

# MC14070B, MC14077B

## CMOS SSI

### Quad Exclusive “OR” and “NOR” Gates

The MC14070B quad exclusive OR gate and the MC14077B quad exclusive NOR gate are constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. These complementary MOS logic gates find primary use where low power dissipation and/or high noise immunity is desired.

#### Features

- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- All Outputs Buffered
- Capable of Driving Two Low-Power TTL Loads or One Low-Power Schottky TTL Load Over the Rated Temperature Range
- Double Diode Protection on All Inputs
- MC14070B – Replacement for CD4030B and CD4070B Types
- MC14077B – Replacement for CD4077B Type
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant

#### MAXIMUM RATINGS (Voltages Referenced to $V_{SS}$ )

Symbol	Parameter	Value	Unit
$V_{DD}$	DC Supply Voltage Range	-0.5 to +18.0	V
$V_{in}, V_{out}$	Input or Output Voltage Range (DC or Transient)	-0.5 to $V_{DD} + 0.5$	V
$I_{in}, I_{out}$	Input or Output Current (DC or Transient) per Pin	$\pm 10$	mA
$P_D$	Power Dissipation, per Package (Note 1)	500	mW
$T_A$	Ambient Temperature Range	-55 to +125	°C
$T_{stg}$	Storage Temperature Range	-65 to +150	°C
$T_L$	Lead Temperature (8-Second Soldering)	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Temperature Derating: “D/DW” Packages: -7.0 mW/°C From 65°C To 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$ .

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either  $V_{SS}$  or  $V_{DD}$ ). Unused outputs must be left open.



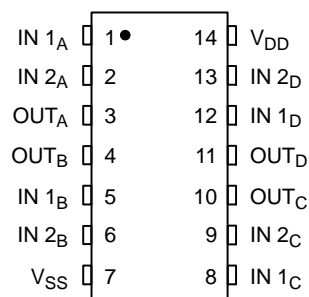
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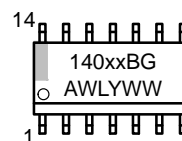


SOIC-14  
D SUFFIX  
CASE 751A

#### PIN ASSIGNMENT



#### MARKING DIAGRAM

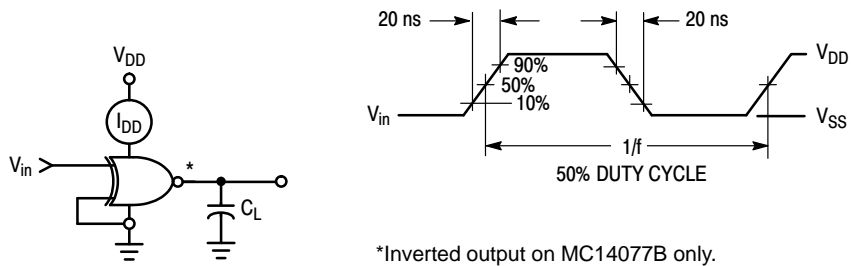
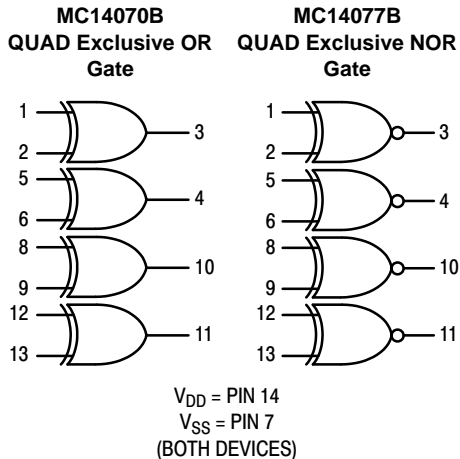


xx = Specific Device Code  
A = Assembly Location  
WL, L = Wafer Lot  
YY, Y = Year  
WW, W = Work Week  
G = Pb-Free Package

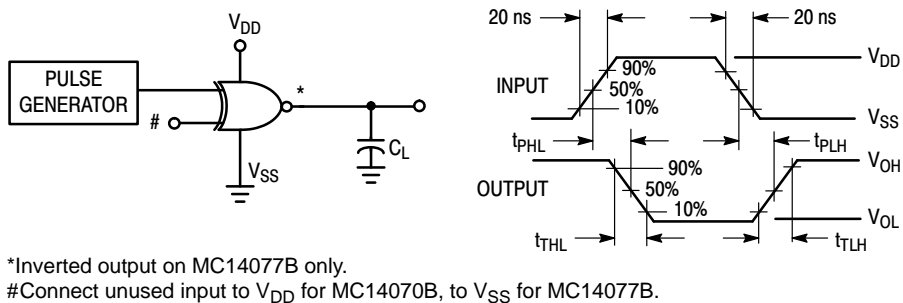
#### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 4 of this data sheet.

# MC14070B, MC14077B



**Figure 1. Power Dissipation Test Circuit and Waveform**



**Figure 2. Switching Time Test Circuit and Waveforms**

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## ELECTRICAL CHARACTERISTICS (Voltages Referenced to $V_{SS}$ )

Characteristic	Symbol	$V_{DD}$ Vdc	-55°C		25°C			125°C		Unit		
			Min	Max	Min	Typ (Note 2)	Max	Min	Max			
Output Voltage $V_{in} = V_{DD}$ or 0	"0" Level	$V_{OL}$	5.0	–	0.05	–	0	0.05	–	0.05	Vdc	
			10	–	0.05	–	0	0.05	–	0.05		
			15	–	0.05	–	0	0.05	–	0.05		
	$V_{in} = 0$ or $V_{DD}$	"1" Level	$V_{OH}$	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
				10	9.95	–	9.95	10	–	9.95	–	
				15	14.95	–	14.95	15	–	14.95	–	
Input Voltage ( $V_O = 4.5$ or $0.5$ Vdc) ( $V_O = 9.0$ or $1.0$ Vdc) ( $V_O = 13.5$ or $1.5$ Vdc)	"0" Level	$V_{IL}$	5.0	–	1.5	–	2.25	1.5	–	1.5	Vdc	
			10	–	3.0	–	4.50	3.0	–	3.0		
			15	–	4.0	–	6.75	4.0	–	4.0		
	$V_O = 0.5$ or $4.5$ Vdc) ( $V_O = 1.0$ or $9.0$ Vdc) ( $V_O = 1.5$ or $13.5$ Vdc)	"1" Level	$V_{IH}$	5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
				10	7.0	–	7.0	5.50	–	7.0	–	
				15	11	–	11	8.25	–	11	–	
Output Drive Current ( $V_{OH} = 2.5$ Vdc) ( $V_{OH} = 4.6$ Vdc) ( $V_{OH} = 9.5$ Vdc) ( $V_{OH} = 13.5$ Vdc)	Source	$I_{OH}$	5.0	–3.0	–	–2.4	–4.2	–	–1.7	–	mAdc	
			5.0	–0.64	–	–0.51	–0.88	–	–0.36	–		
			10	–1.6	–	–1.3	–2.25	–	–0.9	–		
			15	–4.2	–	–3.4	–8.8	–	–2.4	–		
	$V_{OL} = 0.4$ Vdc) ( $V_{OL} = 0.5$ Vdc) ( $V_{OL} = 1.5$ Vdc)	Sink	$I_{OL}$	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
				10	1.6	–	1.3	2.25	–	0.9	–	
15	4.2	–	3.4	8.8	–	2.4	–	–				
Input Current	$I_{in}$	15	–	$\pm 0.1$	–	$\pm 0.00001$	$\pm 0.1$	–	$\pm 1.0$	$\mu$ Adc		
Input Capacitance ( $V_{in} = 0$ )	$C_{in}$	–	–	–	–	5.0	7.5	–	–	pF		
Quiescent Current (Per Package)	$I_{DD}$	5.0	–	0.25	–	0.0005	0.25	–	7.5	$\mu$ Adc		
		10	–	0.5	–	0.0010	0.5	–	15			
		15	–	1.0	–	0.0015	1.0	–	30			
Total Supply Current (Notes 3 & 4) (Dynamic plus Quiescent, Per Package) ( $C_L = 50$ pF on all outputs, all buffers switching)	$I_T$	5.0	$I_T = (0.3 \mu A/kHz) f + I_{DD}$							$\mu$ Adc		
		10	$I_T = (0.6 \mu A/kHz) f + I_{DD}$									
		15	$I_T = (0.9 \mu A/kHz) f + I_{DD}$									
Output Rise and Fall Times (Note 3) ( $C_L = 50$ pF) $t_{TLH}, t_{THL} = (1.35 \text{ ns/pF}) C_L + 33 \text{ ns}$ $t_{TLH}, t_{THL} = (0.60 \text{ ns/pF}) C_L + 20 \text{ ns}$ $t_{TLH}, t_{THL} = (0.40 \text{ ns/pF}) C_L + 20 \text{ ns}$	$t_{TLH},$ $t_{THL}$	5.0	–	–	–	100	200	–	–	ns		
		10	–	–	–	50	100	–	–			
		15	–	–	–	40	80	–	–			
		–	–	–	–	–	–	–	–			
Propagation Delay Times (Note 3) ( $C_L = 50$ pF) $t_{PLH}, t_{PHL} = (0.90 \text{ ns/pF}) C_L + 130 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.36 \text{ ns/pF}) C_L + 57 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.26 \text{ ns/pF}) C_L + 37 \text{ ns}$	$t_{PLH},$ $t_{PHL}$	5.0	–	–	–	175	350	–	–	ns		
		10	–	–	–	75	150	–	–			
		15	–	–	–	55	110	–	–			
		–	–	–	–	–	–	–	–			

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

3. The formulas given are for the typical characteristics only at 25°C.

4. To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) Vfk$$

where:  $I_T$  is in  $\mu$ A (per package),  $C_L$  in pF,  $V = (V_{DD} - V_{SS})$  in volts,  $f$  in kHz is input frequency, and  $k = 0.002$ .

## MC14070B, MC14077B

### ORDERING INFORMATION

Device	Package	Shipping†
MC14070BDG	SOIC-14 (Pb-Free)	55 Units / Rail
MC14070BDR2G	SOIC-14 (Pb-Free)	2500 / Tape & Reel
NLV14070BDR2G*	SOIC-14 (Pb-Free)	2500 / Tape & Reel

MC14077BDG	SOIC-14 (Pb-Free)	55 Units / Rail
MC14077BDR2G	SOIC-14 (Pb-Free)	2500 / Tape & Reel
NLV14077BDR2G*	SOIC-14 (Pb-Free)	2500 / Tape & Reel

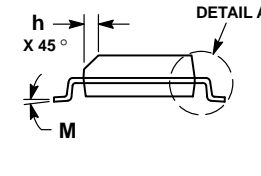
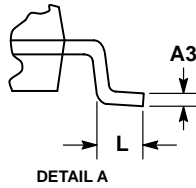
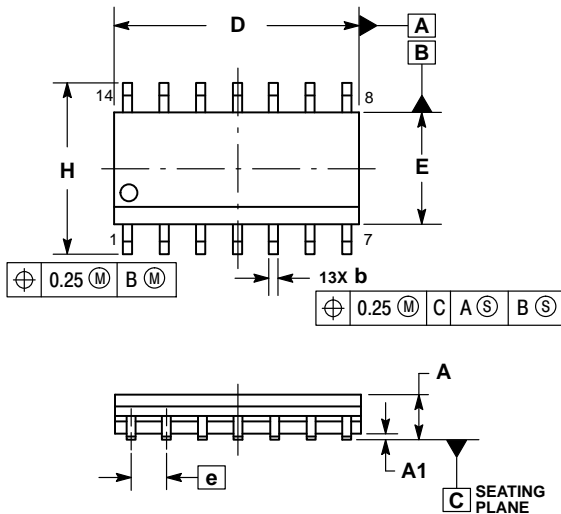
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

\*NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable.

# MC14070B, MC14077B

## PACKAGE DIMENSIONS

### SOIC-14 NB CASE 751A-03 ISSUE K

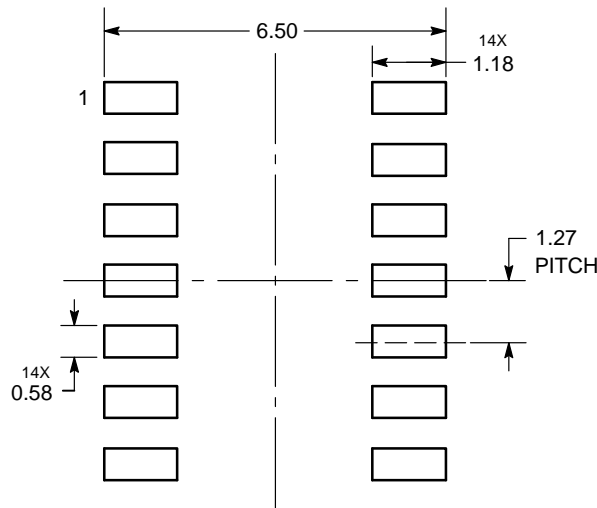


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	1.35	1.75	0.054	0.068
A1	0.10	0.25	0.004	0.010
A3	0.19	0.25	0.008	0.010
b	0.35	0.49	0.014	0.019
D	8.55	8.75	0.337	0.344
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.019
L	0.40	1.25	0.016	0.049
M	0°	7°	0°	7°

### SOLDERING FOOTPRINT\*



DIMENSIONS: MILLIMETERS

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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