

NCP81295, NCP81296

Hot Swap Smart Fuse

The NCP81295 and NCP81296 are 50 A, electronically re-settable, in-line fuses for use in 12 V, high current applications such as servers, storage and base stations. The NCP81295/6 offers a very low 0.65 mΩ integrated MOSFET to reduce solution size and minimize power loss. It also integrates a highly accurate current sensor for monitoring and overload protection.

Power Features

- Co-packaged Power Switch, Hotswap Controller and Current Sense
- Up to 60 A Peak Current Output, 50 A Continuous
- Vin Range: 4.5 V to 18 V
- 0.65 mΩ, no R_{SENSE} Required

Control Features

- Enable Input
- Optional Enable-controlled Output Pulldown when Disabled
- Programmable Soft-Start
- Programmable, Multi-level Current Limit

Reporting Features

- Accurate Analog Load Current Monitor
- Programmable Over Current Alert Output
- Analog Temperature Output
- Status Fault OK Output

Other Features

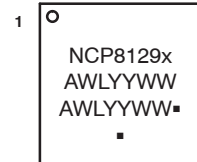
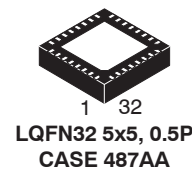
- 5 mm x 5 mm QFN32 Package
- Operating Temperature: -40°C to 125°C
- Can be Paralleled for Higher Current Applications
- Built-in Insertion Delay for Hotswap Applications
- NCP81295: Latch off for Following Protection Features
- NCP81296: Auto-Retry Mode for Following Protection Features
 - ◆ Current-limit after Delay
 - ◆ Fast Short-circuit Protection
 - ◆ Over-Temperature Shutdown
 - ◆ Excessive Soft-start Duration
- Internal Switch Fault Diagnostics
- Low-power Auxiliary Output Voltage



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MARKING DIAGRAM



NCP8129x = Specific Device Code

x = 5 or 6

A = Assembly Location

WL = Wafer Lot

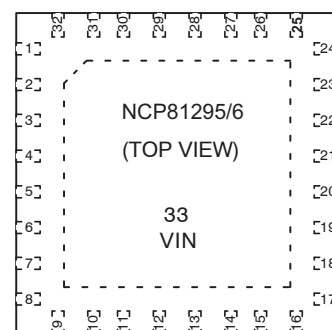
YY = Year

WW = Work Week

▪ = Pb-Free Package
(may or may not be present)

(Note: Microdot may be in either location)

PINOUT



For more details see Figure 1.

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

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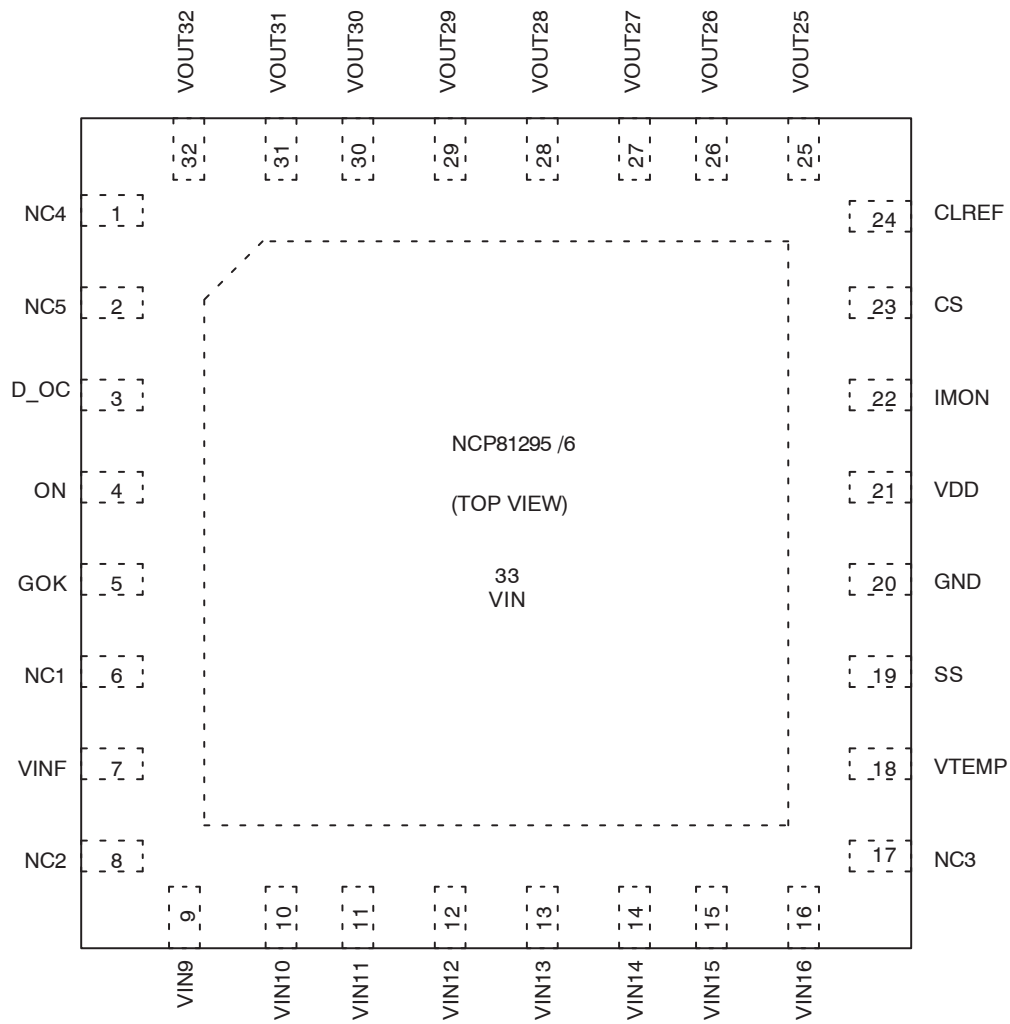


Figure 1. Pin Configuration

Ordering Information

Table 1. AVAILABLE DEVICES

| Device | Package | Shipping [†] |
|---------------|---------|-----------------------|
| NCP81295MNTXG | QFN32 | 2500/Tape & Reel |
| NCP81296MNTXG | QFN32 | 2500/Tape & Reel |

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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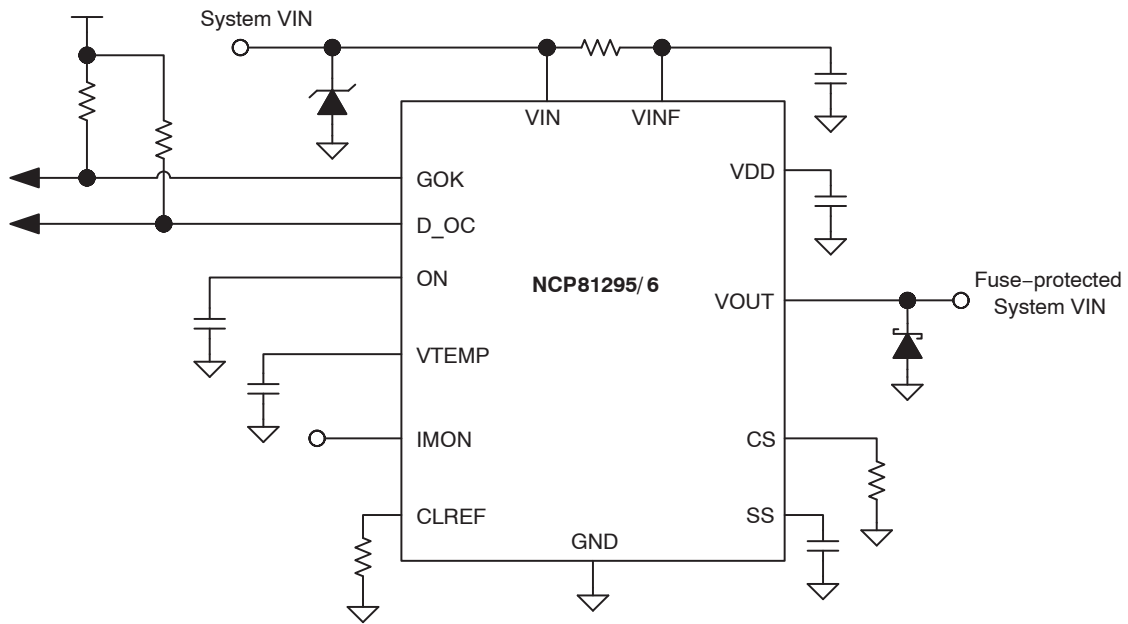


Figure 2. Typical Application

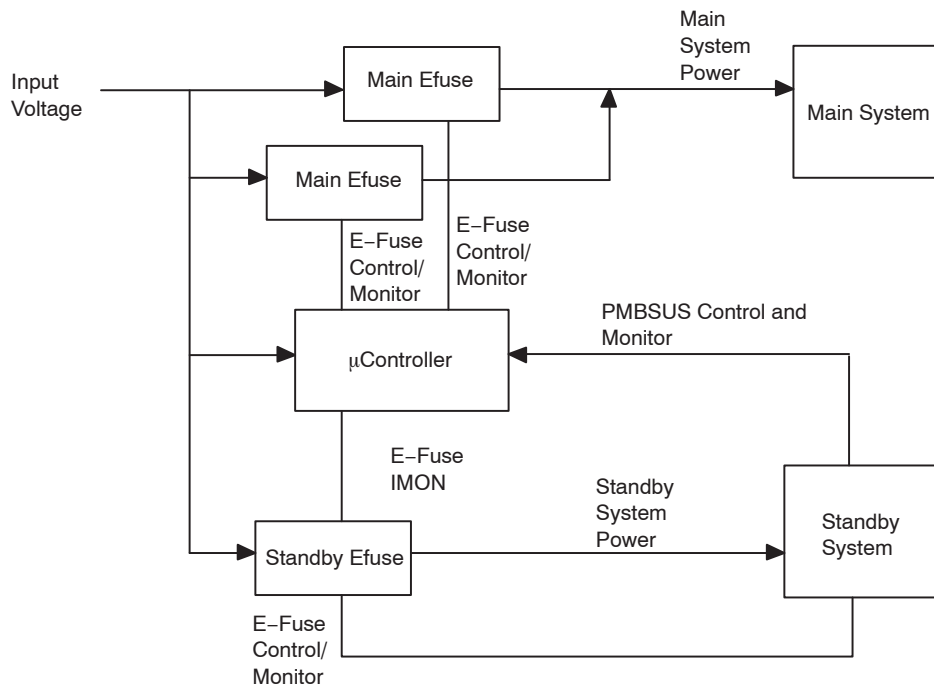


Figure 3. Typical Application Diagram

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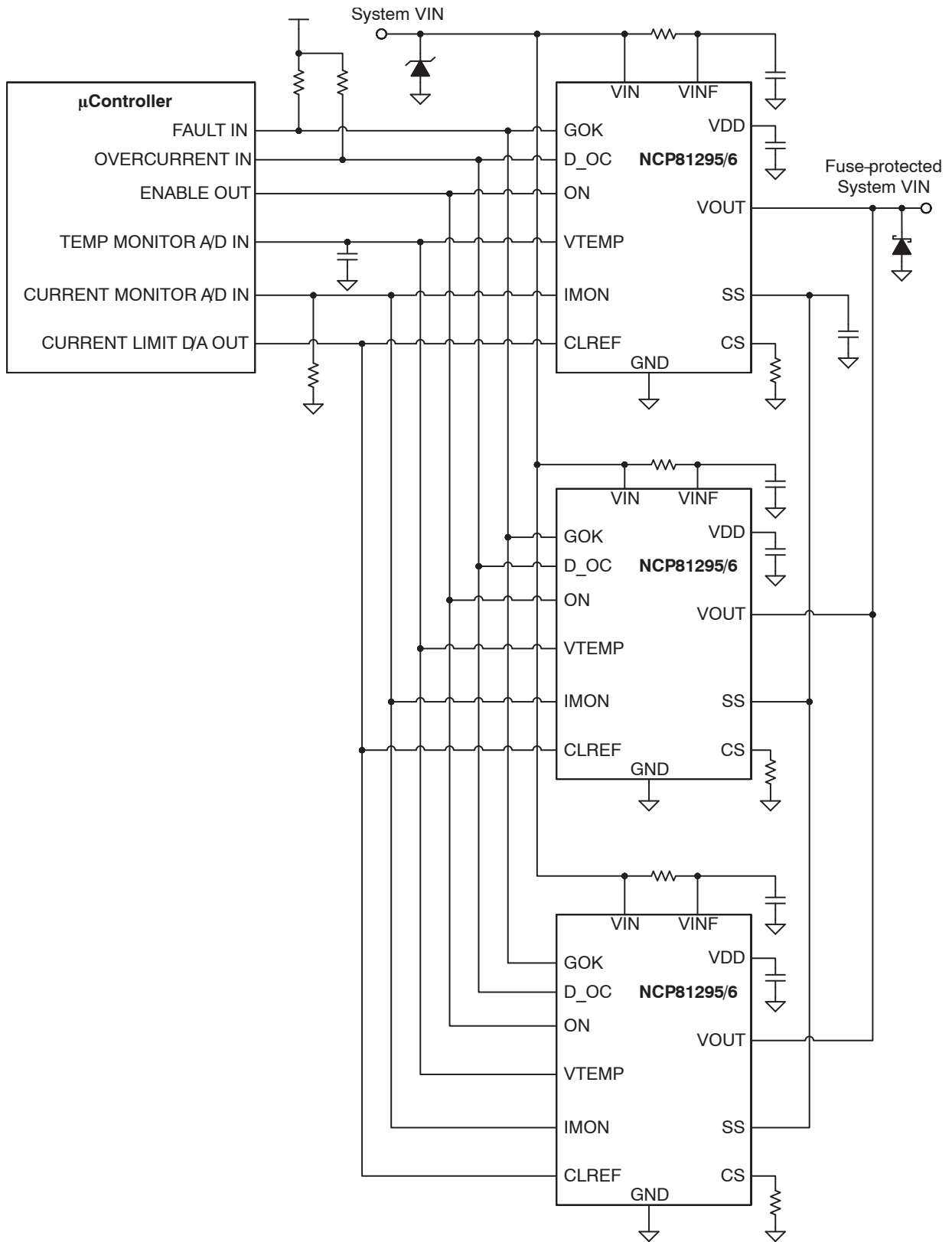


Figure 4. Application Schematic – Parallel Fuse Operation with Controller

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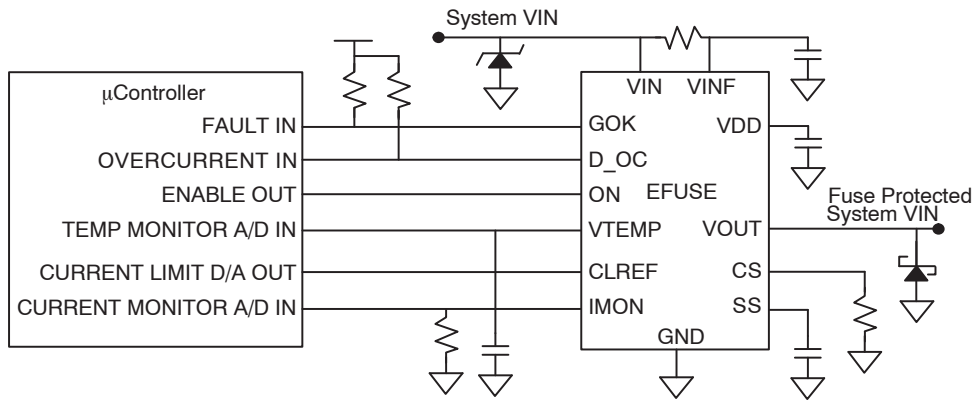


Figure 5. Application Schematic – Single EFuse with Controller

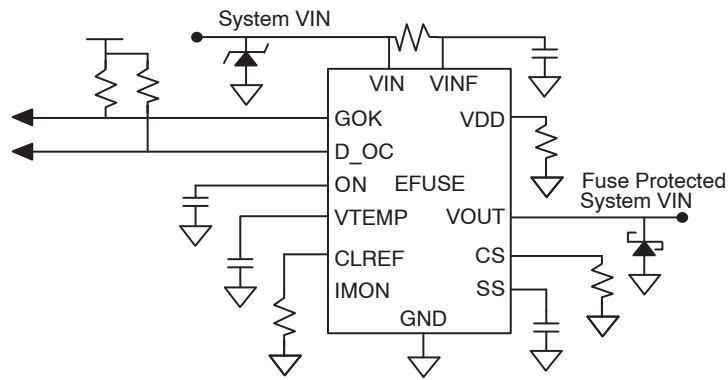


Figure 6. Application Schematic – Stand-alone Operation

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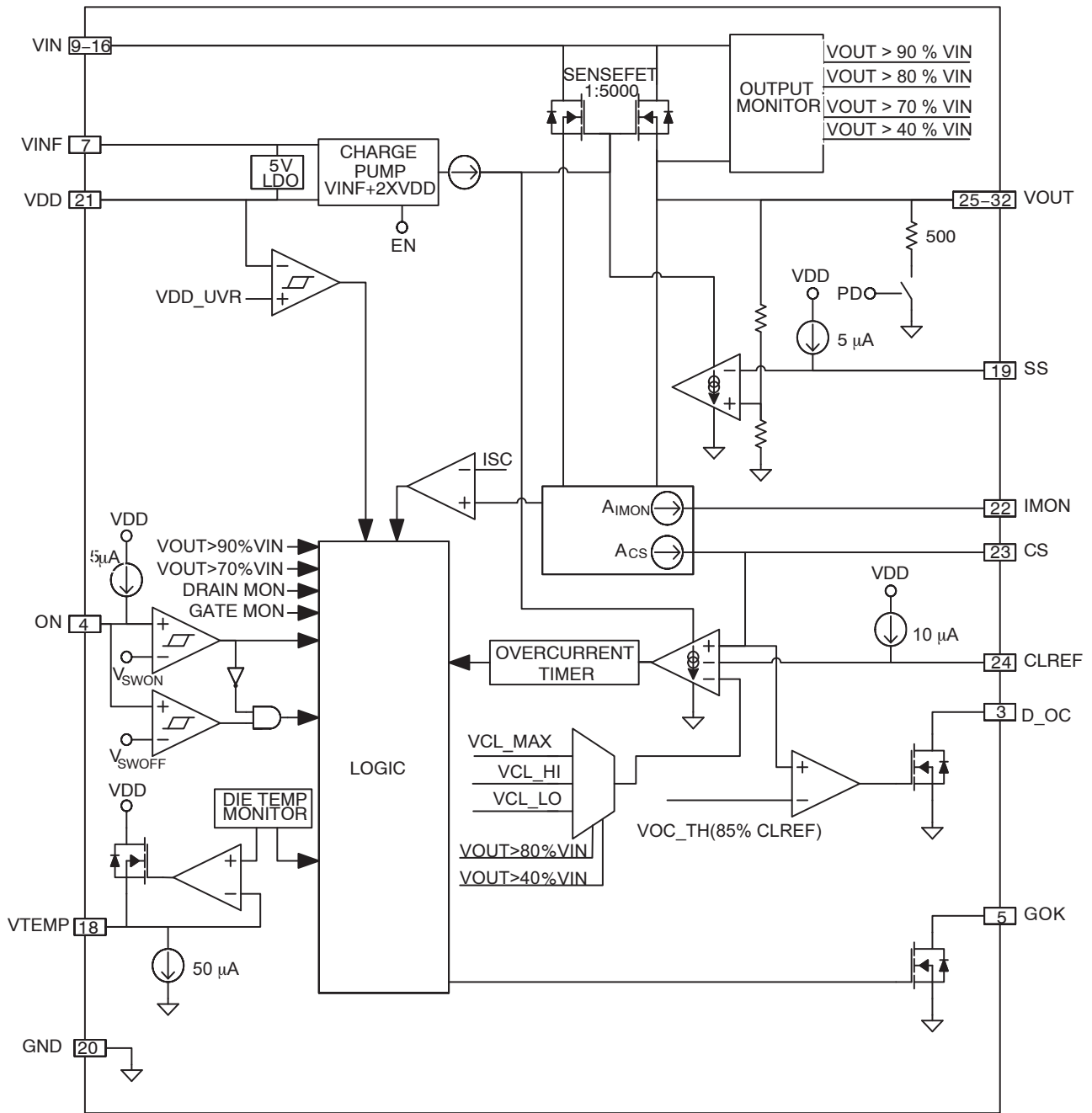


Figure 7. Block Diagram

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Table 2. PIN DESCRIPTION

| Pin No. | Symbol | Description |
|---------|--------|--|
| 1 | NC4 | No electrical connection internally. May connect to any potential |
| 2 | NC5 | No electrical connection internally. May connect to any potential |
| 3 | D_OC | Overcurrent indicator output (open drain). Low indicates the NCP81295 is limiting current. The D_OC output does not report current limiting during soft-start. |
| 4 | ON | Enable input and output pulldown resistance control. |
| 5 | GOK | OK status indicator output (open drain). Low indicates that the NCP81295 was turned off by a fault. |
| 6 | NC1 | Test pin. Do not connect to this pin. Leave floating |
| 7 | VINF | Control circuit power supply input. Connect to VIN pins through an RC filter. |
| 8 | NC2 | Internal FET sense pin. Do not connect to this pin. Leave floating |
| 9 | VIN09 | Input of high current output switch |
| 10 | VIN10 | Input of high current output switch |
| 11 | VIN11 | Input of high current output switch |
| 12 | VIN12 | Input of high current output switch |
| 13 | VIN13 | Input of high current output switch |
| 14 | VIN14 | Input of high current output switch |
| 15 | VIN15 | Input of high current output switch |
| 16 | VIN16 | Input of high current output switch |
| 17 | NC3 | Internal FET gate pin. Do not connect to this pin. Leave floating |
| 18 | VTEMP | Analog temperature monitor output. |
| 19 | SS | Soft Start time programming pin. Connect a capacitor to this pin to set the softstart time. |
| 20 | GND | Ground |
| 21 | VDD | Linear regulator output |
| 22 | IMON | Analog current monitor output |
| 23 | CS | Current sense feedback output (current). Scaling the voltage developed at this pin with a resistor to ground makes this also an input for several current limiting functions and overcurrent indicator D_OC. |
| 24 | CLREF | Current limit setpoint input for normal operation (after soft-start). |
| 25 | VOUT25 | Output of high current output switch |
| 26 | VOUT26 | Output of high current output switch |
| 27 | VOUT27 | Output of high current output switch |
| 28 | VOUT28 | Output of high current output switch |
| 29 | VOUT29 | Output of high current output switch |
| 30 | VOUT30 | Output of high current output switch |
| 31 | VOUT31 | Output of high current output switch |
| 32 | VOUT32 | Output of high current output switch |
| 33 | VIN33 | Input of high current output switch |

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Table 3. MAXIMUM RATINGS

| Rating | Symbol | Min | Max | Unit |
|---|---------------------|---------------------|-----------|------|
| Pin Voltage Range (Note 2) | VINx, VINf | -0.3 | 20 | V |
| Pin Voltage Range (Note 2) | VOUTx | -0.3 -1(<500 ms) | 20 | V |
| Pin Voltage Range (Note 2) | VDD | -0.3 | 6.0 | V |
| Pin Voltage Range (Note 2) | All Other Pins | -0.3 | VDD + 0.3 | V |
| Operating Junction Temperature | T _{J(max)} | | 150 | °C |
| Storage Temperature Range | TSTG | -55 | 150 | °C |
| Lead Temperature Soldering Reflow (SMD Styles Only), Pb-Free Versions (Note 3) | T _{SLD} | | 260 | °C |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. All signals referenced to GND unless noted otherwise.
2. Pin ratings referenced to VDD apply with VDD at any voltage within the VDD Pin Voltage Range.
3. For information, please refer to our Soldering and Mounting Techniques Reference Manual, SOLDERRM/D

Table 4. THERMAL CHARACTERISTICS

| Rating | Symbol | Value | Unit |
|--|-------------------|-------|------|
| Thermal Resistance, Junction-to-Ambient (Note 4) | R _{θJA} | 30 | °C/W |
| Thermal Resistance, Junction-to-Top-Case | R _{θJCT} | 50 | °C/W |
| Thermal Resistance, Junction-to-Bottom-Case | R _{θJCB} | 1.5 | °C/W |
| Thermal Resistance, Junction-to-Board (Note 5) | R _{θJB} | 1.5 | °C/W |
| Thermal Resistance, Junction-to-Case (Note 6) | R _{θJC} | 1.5 | °C/W |

4. Obtained by simulating the device mounted on a 500 mm², 1-oz Cu pad on a 80 mm x 80 mm, 1.6 mm thick 8-layer FR4 board.
5. R_{θJB} value based on hottest board temperature within 1 mm of the package.
6. R_{θJC} ≈ R_{θJCT} // R_{θJCB} (Two-Resistor Compact Thermal Model, JEDEC15-3).

Table 5. RECOMMENDED OPERATING RANGES

| Parameter | Symbol | Min | Max | Unit |
|-------------------------------------|--------------------|-----|-----|------|
| VIN, VINf Pin Voltage Range | | 4.5 | 18 | V |
| Maximum Continuous Output Current | I _{AVE} | | 50 | A |
| Peak Output Current | I _{PEAK} | | 60 | A |
| VDD Output Load Capacitance Range | C _{VDD} | 2.2 | 10 | μF |
| VTEMP Output Load Capacitance Range | C _{VTEMP} | 0.1 | | μF |
| Softstart Duration | T _{SS} | 10 | 100 | ms |
| CS Load Resistance Range | R _{CS} | 1.8 | 4 | kΩ |
| CLREF Voltage Range | V _{CLREF} | 0.2 | 1.4 | V |
| Operating Junction Temperature | T _{J(OP)} | -40 | 125 | °C |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

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Table 6. ELECTRICAL CHARACTERISTICS ($V_{INx} = V_{INF} = 12.0\text{ V}$, $V_{ON} = 3.3\text{ V}$, $C_{VINf} = 0.1\ \mu\text{F}$, $C_{VDD} = 4.7\ \mu\text{F}$, $C_{VTEMP} = 0.1\ \mu\text{F}$, $R_{VTEMP} = 1\ \text{k}\Omega$, $C_{SS} = 100\ \text{nF}$ (unless specified otherwise) Min/Max values are valid for the temperature range $-40^{\circ}\text{C} \leq T_A = T_J \leq 125^{\circ}\text{C}$ unless noted otherwise, and are guaranteed by design and characterization through statistical correlation.

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Units |
|-----------|--------|-----------------|-----|-----|-----|-------|
|-----------|--------|-----------------|-----|-----|-----|-------|

VINF INPUT

| | | | | | | |
|-------------------|--|---|--|------|-----|----|
| Quiescent Current | | $V_{ON} > 1.4\text{ V}$, no load | | 3.23 | 5.0 | mA |
| | | $V_{ON} > 1.4\text{ V}$, fault | | | 5.0 | mA |
| | | $V_{ON} < 0.8\text{ V}$ | | 2.38 | 4.0 | mA |
| | | $V_{ON} < 0.8\text{ V}$, $V_{INF} = 16\text{ V}$ | | | 4.0 | mA |

VDD REGULATOR

| | | | | | | |
|--------------------------|---------------|---|-----|------|-----|----|
| VDD Output Voltage | V_{DD_NL} | $I_{VDD} = 0\text{ mA}$, $V_{INF} = 6\text{ V}$ | 4.7 | 5.09 | 5.3 | V |
| VDD Load Capability | I_{DDLOAD} | $V_{INF} = 5.5\text{ V}$ | | | 30 | mA |
| VDD Current Limit | I_{DD_CL} | $V_{INF} = 12\text{ V}$ and $V_{INF} = 6\text{ V}$ | 50 | 70 | | mA |
| VDD Dropout Voltage | | $I_{VDD} = 25\text{ mA}$, $V_{INF} = 4.5\text{ V}$ | | 85 | 200 | mV |
| UVLO threshold – rising | V_{DD_UVR} | | 4.1 | 4.3 | 4.5 | V |
| UVLO threshold – falling | V_{DD_UVF} | | 3.8 | 4.0 | 4.2 | V |

ON INPUT

| | | | | | | |
|--------------------------------------|----------------|--|-----|------|-----|------------------|
| Bias Current | I_{ON} | From pin into a 0 V or 1.5 V source | 4.0 | 5.0 | 6.0 | μA |
| Switch ON Threshold | V_{SWON} | | 1.3 | 1.4 | 1.5 | V |
| Switch OFF/ Pulldown Upper Threshold | V_{SWOFF} | | | 1.2 | | V |
| Pulldown Lower Threshold | V_{PDOFF} | | | 0.8 | | V |
| Switch ON Delay Timer | t_{ON} | From ON transitioning above V_{SWON} to SS start | 0.6 | 1.0 | 2.5 | ms |
| Switch OFF Delay Time (Note 7) | t_{OFF} | From ON transitioning below V_{SWOFF} to GATE pulldown | | 1.7 | | μs |
| ON Current Source Clamp Voltage | V_{ON_CLMP} | Max pullup voltage of current source | | 3.0 | | V |
| Load Pulldown Delay Timer | t_{PD_DEL} | From ON transitioning into the range between V_{SWOFF} and V_{PDOFF} | | 2.0 | | ms |
| Output Pulldown Resistance | R_{PD} | $V_{OUT} = 12\text{ V}$, PD mode = 1 | | 0.77 | | $\text{k}\Omega$ |

SS PIN

| | | | | | | |
|---------------------|--------------|-----------------------------------|------|------|------|---------------|
| Bias Current | I_{SS} | From pin into a 0 V or 1 V source | 4.62 | 5.15 | 5.62 | μA |
| Gain to VOUT | A_{VSS} | | 9.6 | 10 | 10.4 | V/V |
| SS Pulldown Voltage | V_{OL_SS} | 0.1 mA into pin during ON delay | | 22 | | mV |

GOK OUTPUT

| | | | | | | |
|---------------------------|---------------|-------------------------|--|--|-----|---------------|
| Output Low Voltage | V_{OL_GOK} | $I_{GOK} = 1\text{ mA}$ | | | 0.1 | V |
| Off-state Leakage Current | I_{LK_GOK} | $V_{GOK} = 5\text{ V}$ | | | 1.0 | μA |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

7. Guaranteed by design or characterization data. Not tested in production.

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Table 6. ELECTRICAL CHARACTERISTICS ($V_{INx} = V_{INF} = 12.0\text{ V}$, $V_{ON} = 3.3\text{ V}$, $C_{VINf} = 0.1\ \mu\text{F}$, $C_{VDD} = 4.7\ \mu\text{F}$, $C_{VTEMP} = 0.1\ \mu\text{F}$, $R_{VTEMP} = 1\ \text{k}\Omega$, $C_{SS} = 100\ \text{nF}$ (unless specified otherwise) Min/Max values are valid for the temperature range $-40^\circ\text{C} \leq T_A = T_J \leq 125^\circ\text{C}$ unless noted otherwise, and are guaranteed by design and characterization through statistical correlation.

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Units |
|---|-----------------------------|--------------------------------------|----------------------|-----|-----|---------------|
| IMON/CS OUTPUT | | | | | | |
| IMON or CS Current (single EFuse) Based on $10\ \mu\text{A}/\text{A} + 5\ \mu\text{A}$ | I_{IMON}/I_{CS} | $T_J = 0\text{ to }85^\circ\text{C}$ | IOUT = 5 A (Note 7) | | 55 | μA |
| | | | IOUT = 10 A (Note 7) | | 105 | μA |
| | | | IOUT = 25 A (Note 7) | | 255 | μA |
| | | | IOUT = 50 A (Note 7) | | 505 | μA |
| Accuracy (single EFuse) | | $T_J = 0\text{ to }85^\circ\text{C}$ | IOUT = 5 A (Note 7) | -6 | +6 | % |
| | | | IOUT = 10 A (Note 7) | -4 | +4 | % |
| | | | IOUT = 25 A (Note 7) | -4 | +4 | % |
| | | | IOUT = 50 A (Note 7) | -4 | +4 | % |
| IMON or CS Current Source Clamp Voltage | V_{IM_CLMP}/V_{CS_CLMP} | Max pullup voltage of current source | | 3.0 | | V |
| Pre-Biased Offset Current Load for Auto-Zero Op-Amp | I_{AZ_BIAS} | | | 5.0 | | μA |

CURRENT LIMIT & CLREF PIN

| | | | | | | |
|-------------------------------------|----------------|--|------|-----|------|---------------|
| Current Limit Voltage | V_{CL_TH} | If $V_{CS} > V_{CL_TH}$ current limiting regulation occurs via gate | 95 | 98 | 101 | $\%V_{CLREF}$ |
| Current Limit Clamp Voltage | V_{CL_LO} | $V_{OUT} < 40\%$, $V_{IN} V_{CLREF} > 0.15\text{ V}$ | 135 | 152 | 165 | mV |
| | V_{CL_HI} | $40\% V_{IN} < V_{OUT} < 80\% V_{IN}$ $V_{CLREF} > 0.5\text{ V}$ | 480 | 504 | 520 | mV |
| Max Current Limit Reference Voltage | V_{CL_MX} | $V_{OUT} > 80\% V_{IN}$, $V_{CLREF} > 1.6\text{ V}$ | 1.55 | 1.6 | 1.65 | V |
| Response Time (Note 7) | t_{CL_REG} | $V_{CS} > V_{CLREF}$ until current limiting | | 200 | | μs |
| CLREF Bias Current | I_{CL} | From pin into a 1.2 V source | 9.6 | 10 | 10.4 | μA |
| CLREF Current Source Clamp Voltage | V_{CL_CLMP} | Max pullup voltage of current source | | 3.0 | | V |
| FET Turn-off Timer | t_{CL_LA} | Delay between current limit detection and FET turn-off (GOK = 0) | | 250 | | μs |

D_OC OUTPUT

| | | | | | | |
|---------------------------|---------------|---|----|-----|-----|---------------|
| Overcurrent Threshold | V_{OC_TH} | If $V_{CS} > V_{OC_TH}$ D_OC pin pulls low | 83 | 86 | 90 | $\%V_{CLREF}$ |
| Output Low Voltage | V_{OL_DOC} | $I_{DOC} = 1\ \text{mA}$ | | | 0.1 | V |
| Off-state Leakage Current | I_{LK_DOC} | $V_{DOC} = 5\text{ V}$ | - | | 1.0 | μA |
| Delay (rising) (Note 7) | | $V_{CS} < \text{limit}$ until D_OC rising | - | 1.0 | | μs |
| Delay (falling) (Note 7) | | $V_{CS} > \text{limit}$ until D_OC falling | - | 1.0 | | μs |

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| Parameter | Symbol | Test Conditions | Min | Typ | Max | Units |
|---------------------------------|------------------|---|-----|------|-----|----------------------------|
| SHORT CIRCUIT PROTECTION | | | | | | |
| Current Threshold (Note 7) | I_{SC} | NCP81295 | | 100 | | A |
| | | NCP81296 | | 80 | | A |
| Response Time (Note 7) | t_{SC} | From $I_{OUT} > I_{LIMSC}$ until gate pulldown | | 500 | | ns |
| VTEMP OUTPUT | | | | | | |
| Bias Voltage | $V_{VTEMP25}$ | At 25°C | | 450 | | mV |
| Gain (Note 7) | A_{VTEMP} | $0^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$ | | 10 | | $\text{mV}/^\circ\text{C}$ |
| Load Capability | R_{VTEMP} | At 25°C | | 1 | | $\text{k}\Omega$ |
| Pulldown Current | I_{VTEMP} | At 25°C | | 50 | | μA |
| THERMAL SHUTDOWN | | | | | | |
| Temperature Shutdown (Note 7) | T_{TSD} | GOK pulls dow | | 140 | | $^\circ\text{C}$ |
| OUTPUT SWITCH (FET) | | | | | | |
| On Resistance | R_{DSon} | $T_J = 25^\circ\text{C}$ | | 0.65 | 1.0 | $\text{m}\Omega$ |
| Off-state leakage current | I_{DSoff} | $V_{IN} = 16\text{ V}$, $V_{ON} < 1.2\text{ V}$, $T_J = 25^\circ\text{C}$ | | | 1.0 | μA |
| FAULT detection | | | | | | |
| V_{DS} Short Threshold | V_{DS_TH} | Startup postponed if $V_{OUT} > V_{DS_TH}$ at $V_{ON} > V_{SWON}$ transition | | 88.8 | | $\%V_{IN}$ |
| V_{DS} Short OK Threshold | V_{DS_OK} | Startup resumed if $V_{OUT} < V_{DS_OK}$ anytime after postponed | | 68.6 | | $\%V_{IN}$ |
| V_{GD} Short Threshold | V_{DG_TH} | Startup postponed if $V_G > V_{DG_TH}$ at $V_{ON} > V_{SWON}$ transition | | 3.1 | | V |
| V_{GD} Short OK Threshold | V_{DG_OK} | Startup resumed if $V_G < V_{DG_OK}$ anytime after postponed | | 3.0 | | V |
| V_G Low Threshold | V_G_TH | Latch/Restart if $V_{GD} < V_G_TH$ after t_{SSF_END} or t_{GATE_FLT} | | 5.4 | | V |
| V_{OUT} Low Threshold | V_{OUTL_TH} | Latch/Restart if $V_{OUT} < V_{OUTL_TH}$ after t_{SSF_END} | | 90 | | $\%V_{IN}$ |
| Gate Fault Timer (Note 7) | t_{GATE_FLT} | Time from $V_{GD} < V_G_TH$ transition after t_{SSF_END} completed | | 200 | | ms |
| Startup Timer Failsafe (Note 7) | t_{SSF_END} | Time from $V_{ON} > V_{SWON}$ transition, Max programmable softstart time | | 200 | | ms |
| AUTO-RETRY (NCP81296) | | | | | | |
| Auto-Retry Delay | t_{DLY_RETRY} | Delay from power-down to retry of startup | | 1000 | | ms |

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TYPICAL CHARACTERISTICS

Test Conditions: $V_{in} = 12\text{ V}$, $R_{cs} = 2\text{ k}\Omega$, $C_{ss} = 200\text{ nF}$, $R_{CLREF} = 121\text{ k}\Omega$, $R_{IMON} = 2\text{ k}\Omega$

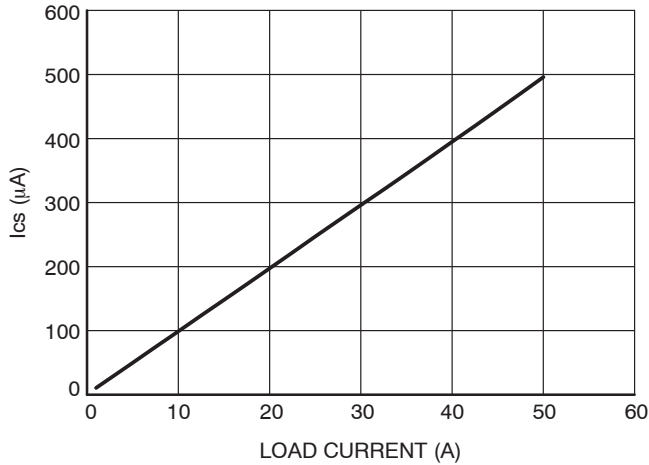


Figure 8. Ics vs. Load Current

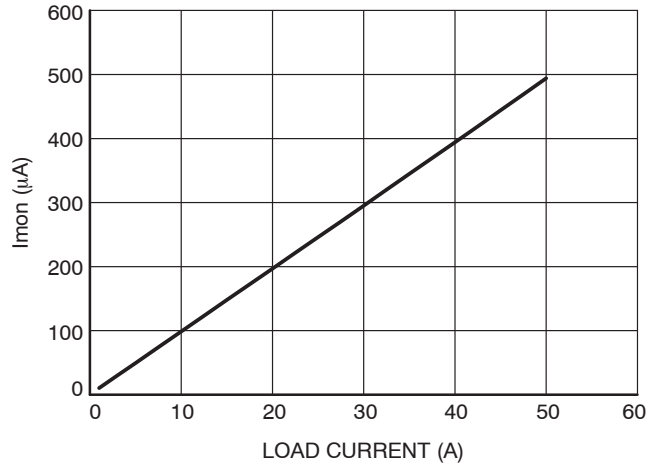


Figure 9. Imon vs. Load Current

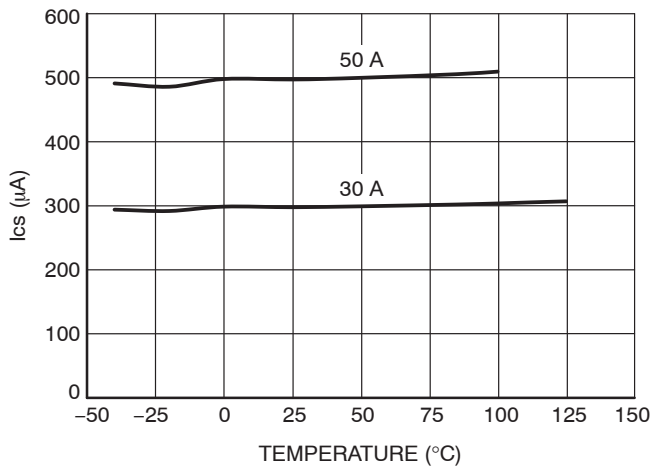


Figure 10. Ics vs. Temperature

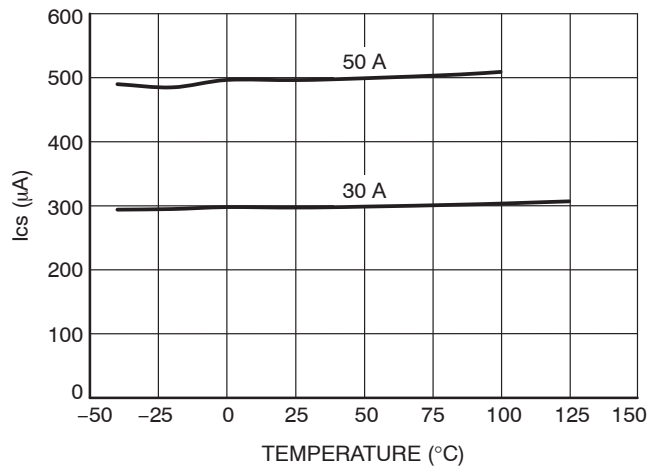


Figure 11. Imon vs. Temperature

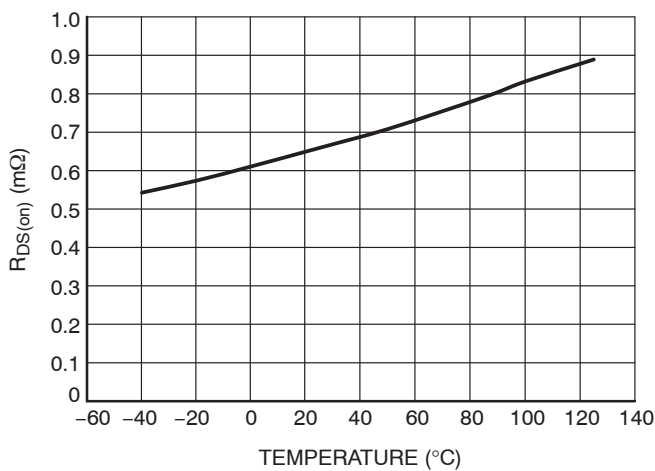


Figure 12. Output Switch $R_{DS(on)}$ @ 22 A vs. Temperature

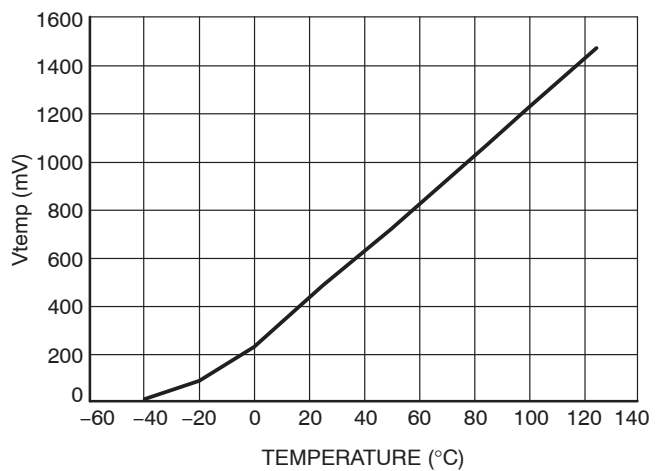


Figure 13. Vtemp vs. Temperature (no load)

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TYPICAL CHARACTERISTICS

Test Conditions: $V_{in} = 12\text{ V}$, $R_{cs} = 2\text{ k}\Omega$, $C_{ss} = 200\text{ nF}$, $R_{CLREF} = 121\text{ k}\Omega$, $R_{IMON} = 2\text{ k}\Omega$

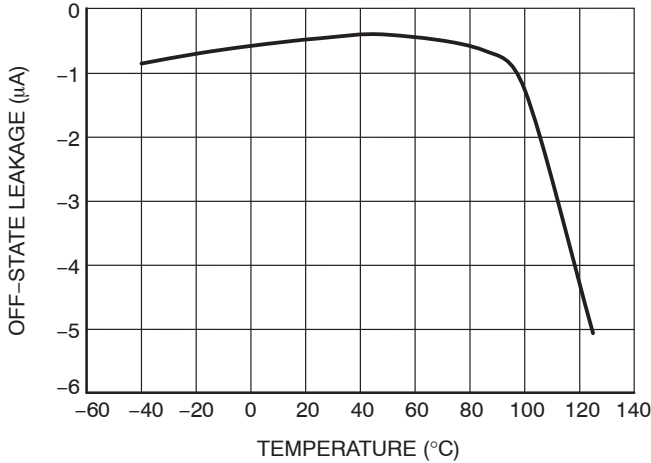


Figure 14. Output Switch Off-state Leakage vs. Temperature

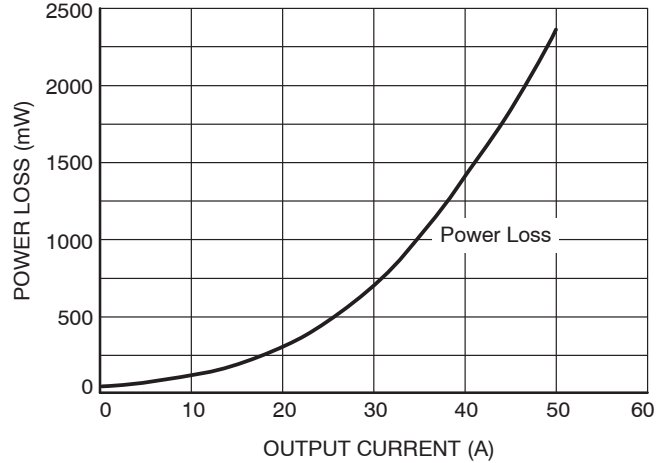


Figure 15. Power Loss vs. Load Current

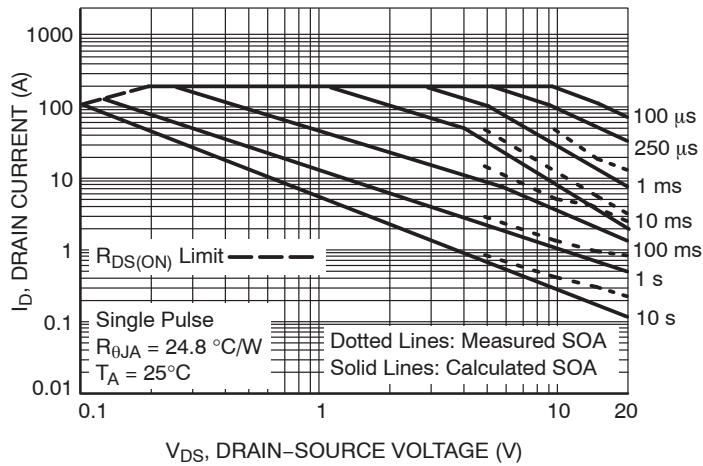


Figure 16. Internal FET's Safe Operating Area (SOA)

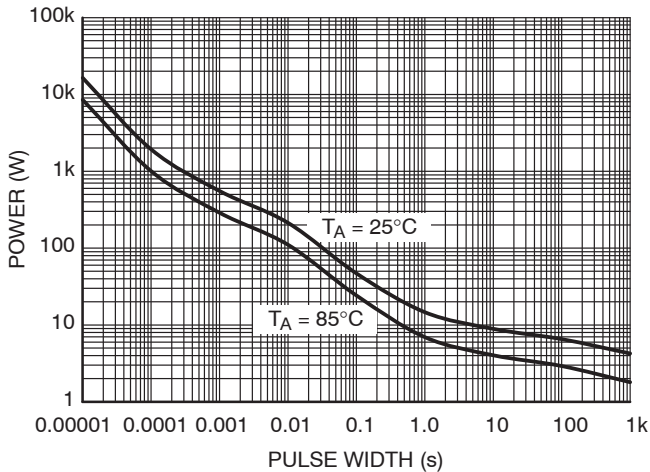


Figure 17. Single Pulse Power Rating (10 µs - 1000 s, Junction-to-Ambient, Note 4)

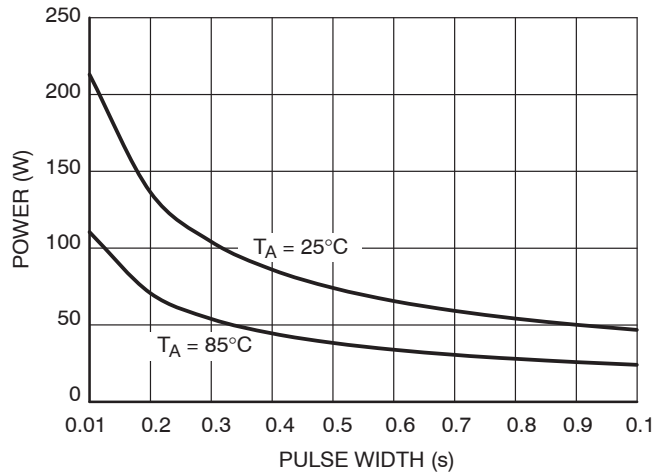


Figure 18. Single Pulse Power Rating (10 ms - 100 ms, Junction-to-Ambient, Note 4)

NCP81295, NCP81296

TYPICAL CHARACTERISTICS

Test Conditions: $V_{in} = 12\text{ V}$, $R_{cs} = 2\text{ k}\Omega$, $C_{ss} = 200\text{ nF}$, $R_{CLREF} = 121\text{ k}\Omega$, $R_{IMON} = 2\text{ k}\Omega$

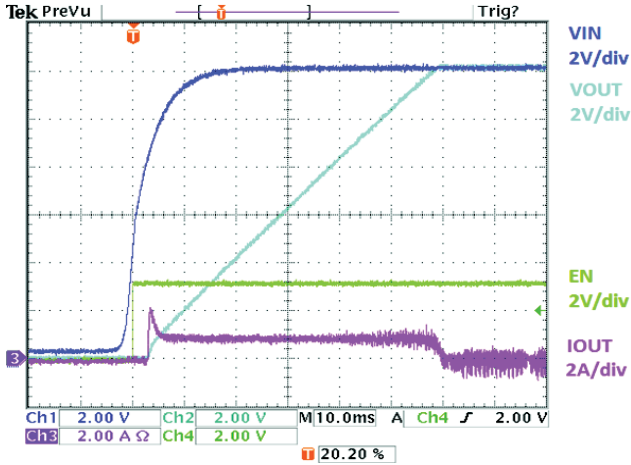


Figure 19. Start Up by VIN (Iout = 0 A)

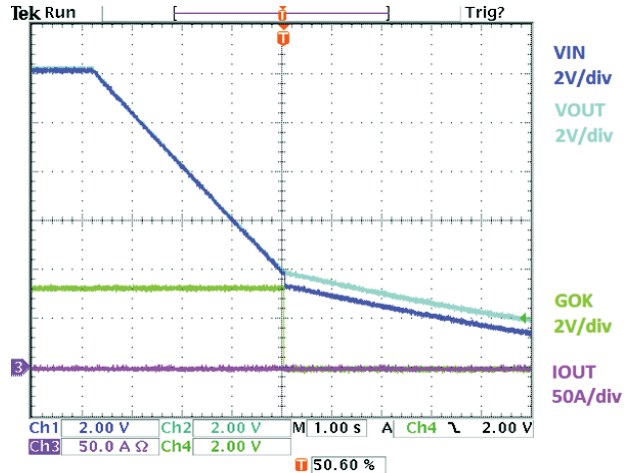


Figure 20. Shut Down by VIN (Iout = 0 A)

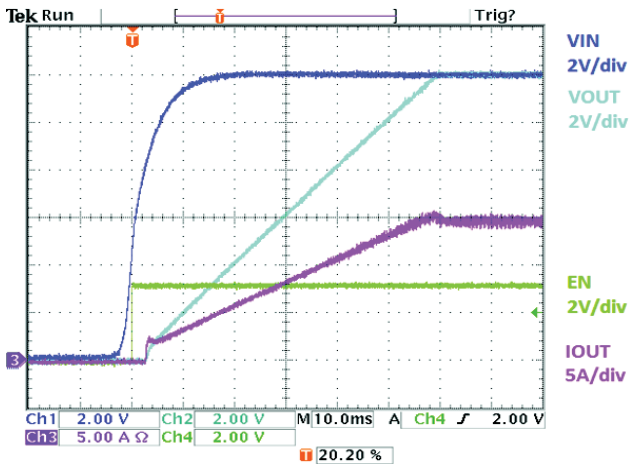


Figure 21. Start Up by VIN (Iout = 15 A)

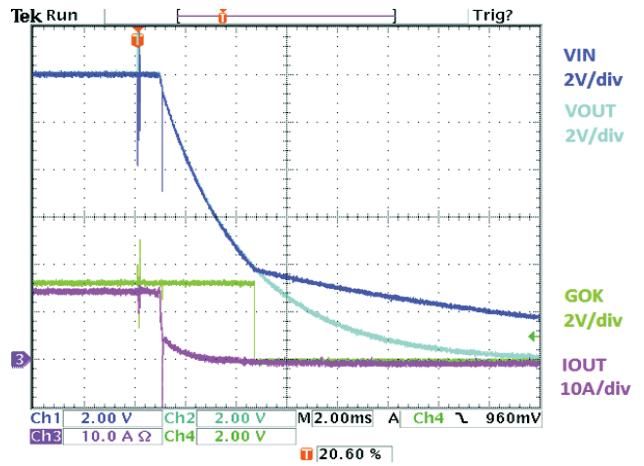


Figure 22. Shut Down by VIN (Iout = 15 A)

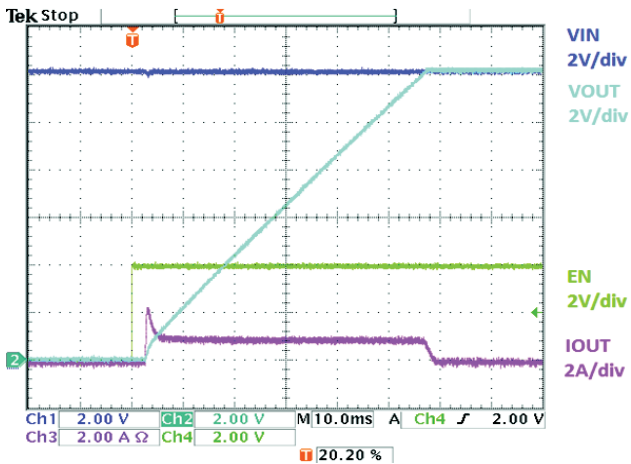


Figure 23. Start Up by EN (Iout = 0 A)

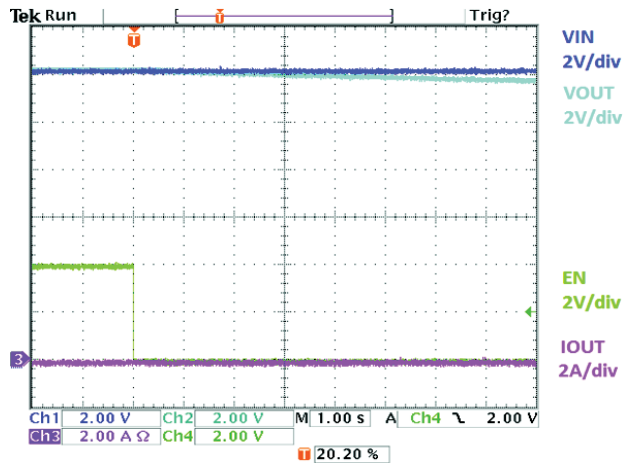


Figure 24. Shut Down by EN (Iout = 0 A)

NCP81295, NCP81296

TYPICAL CHARACTERISTICS

Test Conditions: $V_{in} = 12\text{ V}$, $R_{cs} = 2\text{ k}\Omega$, $C_{ss} = 200\text{ nF}$, $R_{CLREF} = 121\text{ k}\Omega$, $R_{IMON} = 2\text{ k}\Omega$

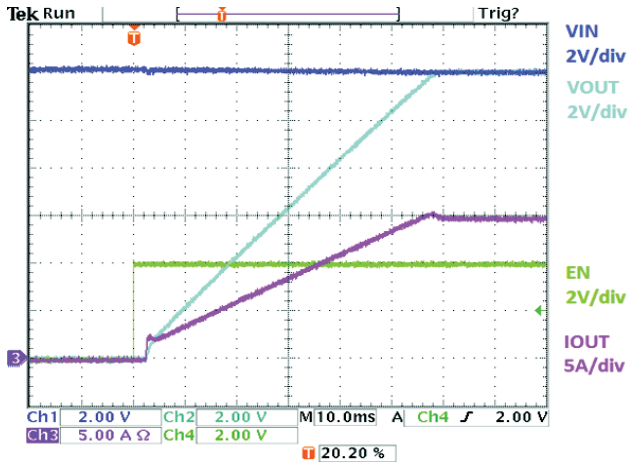


Figure 25. Start Up by EN (Iout = 15 A)

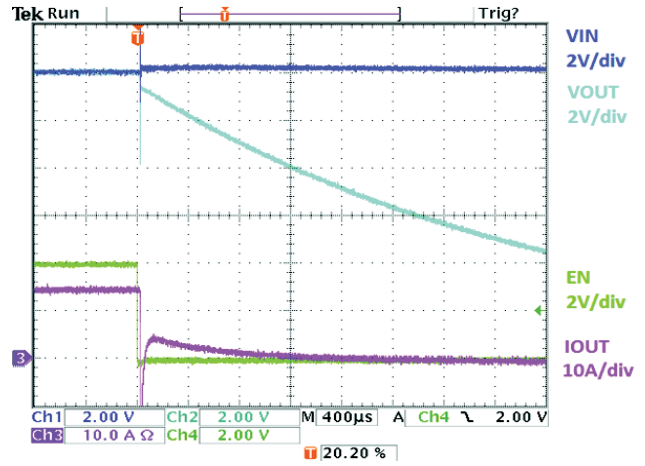


Figure 26. Shut Down by EN (Iout = 15 A)

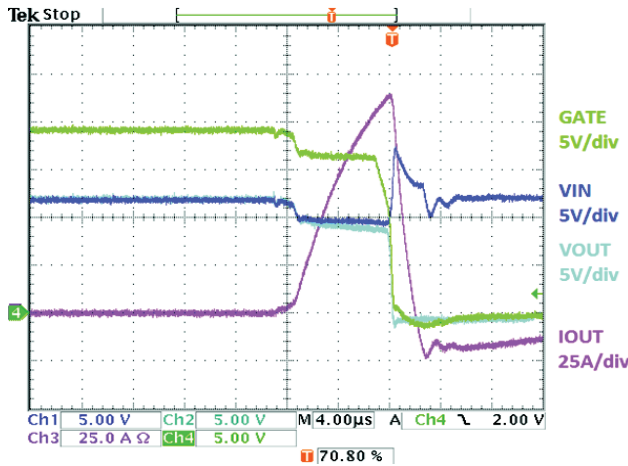


Figure 27. Short Circuit during Normal Operation (Iout = 0 A)

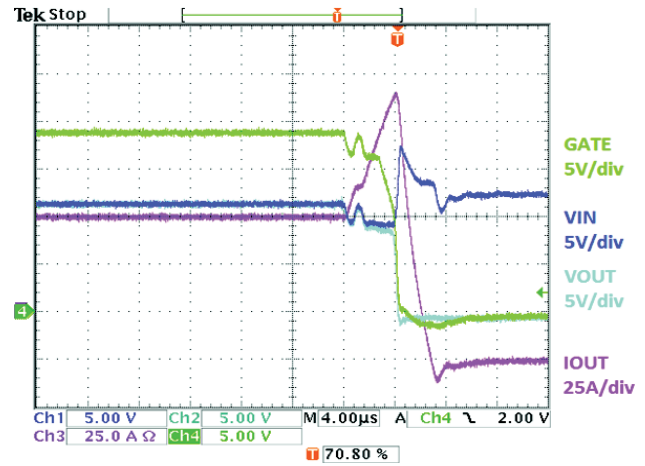


Figure 28. Short Circuit during Normal Operation (Iout = 50 A)

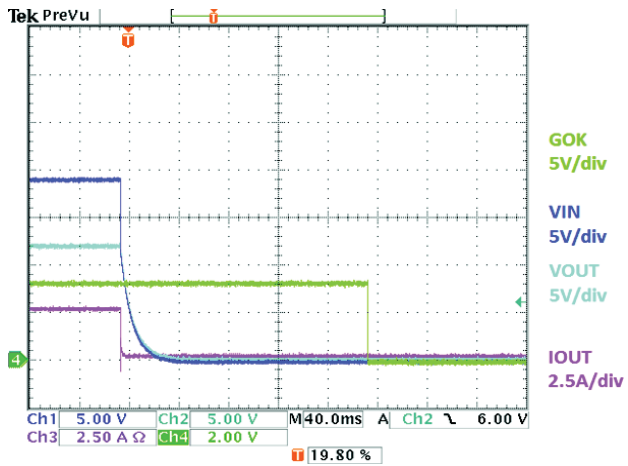


Figure 29. Short FET's Gate During Normal Operation (Iout = 2.5 A)

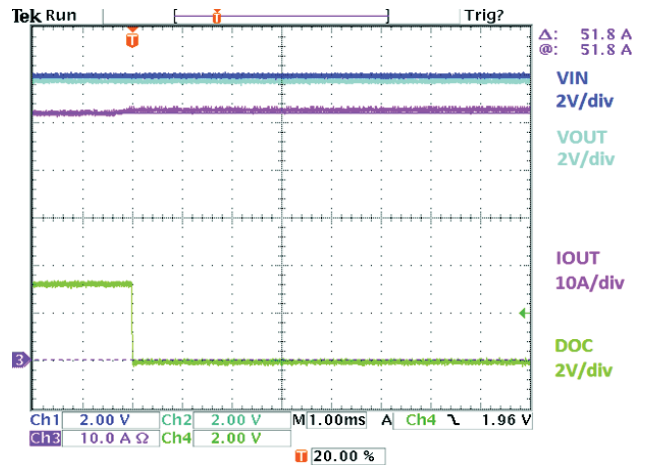


Figure 30. DOC Index for Current Limit during Normal Operation (Iout = 51.8 A)

NCP81295, NCP81296

TYPICAL CHARACTERISTICS

Test Conditions: $V_{in} = 12\text{ V}$, $R_{cs} = 2\text{ k}\Omega$, $C_{ss} = 200\text{ nF}$, $R_{CLREF} = 121\text{ k}\Omega$, $R_{IMON} = 2\text{ k}\Omega$

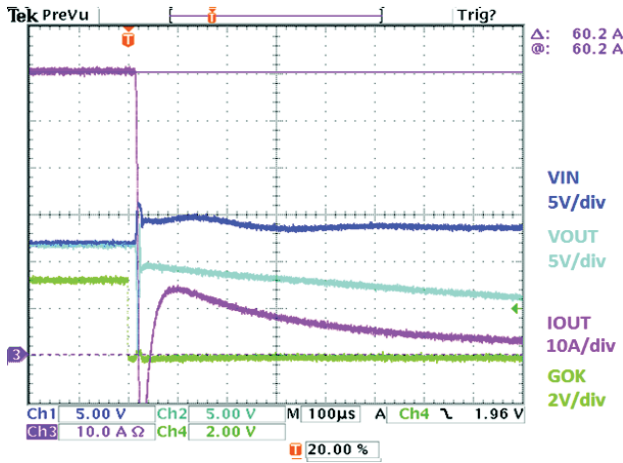


Figure 31. OCP during Normal Operation($I_{out}=60.2\text{A}$)

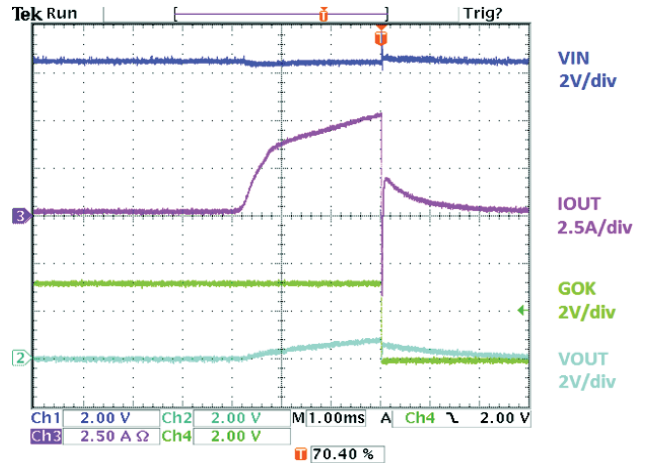


Figure 32. OCP during Power Up by Enable

General Information

The NCP81295/6 is an N-channel MOSFET co-packaged with a smart hotswap controller. It is suited for high-side current limiting and fusing in hot-swap applications. It can be used either alone, or in a parallel configuration for higher current applications.

VDD Output (Auxiliary Regulated Supply)

An internal linear regulator draws current from the VIN pin to produce and regulate voltage at the VDD pin. This auxiliary output supply is current-limited to I_{DD_CL} . A ceramic capacitor in the range of 2.2 μF to 10 μF must be placed between the VDD and GND pins, as close to the NCP81295/6 as possible.

ON Input (Device Enable)

When the ON pin voltage (V_{ON}) is higher than V_{SWON} , and no undervoltage (UVLO) or output switch faults are present, the output switch turns on. When V_{ON} is lower than V_{SWOFF} , the output switch is off. If V_{ON} is between V_{PDOFF} and V_{SWOFF} for longer than t_{PD_DEL} , the output switches off, and a pulldown resistance to ground, of R_{PD} , is applied to VOUT.

For standalone applications, the ON pin sources current I_{ON} , which can be used to delay output switch turn-on for some time after the appearance of input voltage by connecting a capacitor from the ON pin to ground.

A bi-level control signal driving to ground can be biased up with a resistive divider to produce ON input levels between $V_{PDOFF} < V_{ON} < V_{SWON}$ and $V_{ON} > V_{SWON}$ in order to always apply the output pulldown when the output switch is off.

SS Output (Soft-Start)

When the output switch first turns on, it does so in a controlled manner. The output voltage (VOUT) follows the voltage at the SS pin, produced by current I_{SS} into a capacitor from SS to ground. The duration of soft-start can be programmed by selection of the capacitor value. In parallel fuse applications, the SS pins of all fuses should be shorted together to one shared SS capacitor. Internal soft-start load balancing circuitry will ensure the soft-start current is shared between paralleled devices, so as not to stress one device more than another or hit a soft start-current limit.

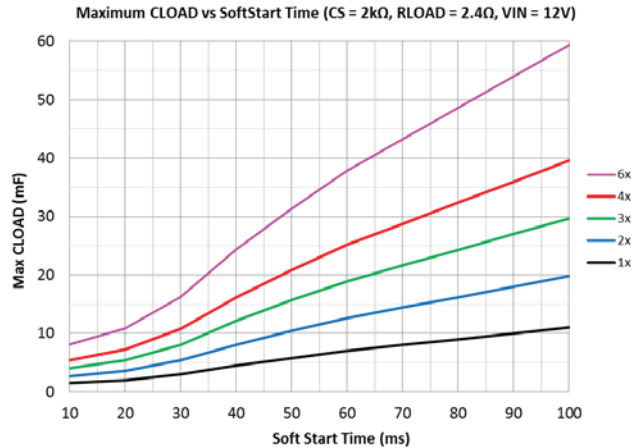
The soft-start capacitor value can be calculated by:

$C_{SS} = (t_{SS} * I_{SS} * AV_{SS})/V_{IN}$ (where t_{SS} is the target soft-start time). The recommended range of t_{SS} is 10 – 100 ms (see Table 5).

The typical C_{SS} values for different t_{SS} are listed below:

| t_{SS} (ms) | C_{SS} (nF) | t_{SS} (ms) | C_{SS} (nF) |
|---------------|---------------|---------------|---------------|
| 10 | 47 | 60 | 270 |
| 20 | 82 | 70 | 330 |
| 30 | 120 | 80 | 330 |
| 40 | 180 | 90 | 470 |
| 50 | 220 | 100 | 470 |

The maximum load capacitor value NCP81295/6 can power up depends on the device soft-start time. When $V_{IN} = 12\text{ V}$, $R_{CS} = 2\text{ k}\Omega$, $R_{LOAD} = 2.4\ \Omega$, their relationship for different paralleled operations are shown as below chart (above line device shuts down safely due to protection, below line device powers up successfully without trigger protection):



GOK Output (Gate OK)

The GOK pin is an open-drain output that is pulled low to report the fault under the following conditions:

- V_{DD} voltage is below UVLO voltage at any time.
- V_{ON} disabled and V_{DS_OK} is false (indicates a short from VIN to VOUT).
- V_{ON} disabled and V_{DG_OK} is false (indicates a short from GATE to VIN).
- V_{ON} enabled and V_{SS_OK} is false at t_{SSF_END} (indicates $V_{OUT} < 90\%$ after soft-start completes – FET latches off for NCP81295/auto-retries for NCP81296).
- V_{ON} enabled and V_G is below V_{G_TH} at t_{SSF_END} (indicates leakage on GATE in startup – FET latches off for NCP81295/auto-retries for NCP81296).
- V_{ON} enabled and V_G is below V_{G_TH} after t_{GATE_FLT} (indicates leakage on GATE during normal operation – FET latches off for NCP81295/auto-retries for NCP81296).
- V_{ON} enabled and a current-limiting condition lasts longer than t_{OC_LA} (FET latches off for NCP81295/auto-retries for NCP81296).
- V_{ON} enabled and device temperature is above T_{TSD} (indicates an over-temperature is detected – FET latches off for NCP81295/auto-retries for NCP81296).

Usually GOK can't be used as power good to indicate the output voltage is in the normal range. Bringing VDD below the UVLO voltage is required to release a latching condition.

IMON Output (Current Monitor)

The IMON pin sources a current that is A_{IMON} times the VOUT output current. A resistor connected from the IMON pin to ground can be used to monitor current information as a voltage up to V_{IM_CLMP} . A capacitor of any value in parallel with the IMON resistor can be used to low-pass filter the IMON signal without affecting any internal operation of the device.

CLREF Pin (Current Limit and Over-Current Reference)

The CLREF pin voltage determines the current-limit regulation point and over-current indication point via its interaction with the CS pin voltage. The CLREF voltage can be applied by an external source, such as a hot-swap controller or D-to-A converter, or developed across a programming resistor to ground by the CLREF bias current, I_{CL} . The recommended range of CLREF voltage is 0.2 – 1.4 V (see Table 5).

CS Input/Output (Current Set)

The CS pin is both an input and an output. The CS pin sources a current that is A_{CS} times the VOUT current. This produces a voltage on the CS pin that is the product of the CS pin current and an external CS pin resistance to ground.

The voltage generated on V_{CS} determines the D_OC over-current indicator trip point and the current-limit regulation point, via its interaction with the voltage on CLREF pin.

When the voltage on the CS pin is higher than V_{OC_TH} , D_OC is pulled low. If the CS pin voltage drops below V_{OC_TH} , the D_OC pin is released and gets pulled high by the external pullup resistor. D_OC transitions based on the following formula: $I_{OUT} = V_{OC_TH} / (R_{CS} * A_{CS})$.

The V_{OC_TH} trip point is based on a percentage of V_{CLREF} (85%).

During normal operation ($V_{ON} > V_{SWON}$ for longer than t_{SS_END}), if the voltage on the CS pin is above V_{CL_TH} (V_{CL_TH} is clamped at V_{CL_MX} if $V_{CL_TH} > V_{CL_MX}$), then the gate voltage of the FET is modulated to limit current into the output based on the following formula:

$I_{OUT} = V_{CL_TH} / (R_{CS} * A_{CS})$. The V_{CL_TH} regulation point is equal to V_{CLREF} .

During startup ($V_{ON} > V_{SWON}$ for less than t_{SS_END}), the current limit reference voltage is clamped according to the following:

- When $V_{OUT} < 40\%$ of V_{IN} , $V_{CL_TH} = V_{CL_LO}$ or V_{CLREF} (whichever is lower).
- When V_{OUT} is between 40% and 80% of V_{IN} , $V_{CL_TH} = V_{CL_HI}$ or V_{CLREF} (whichever is lower).
- When V_{OUT} exceeds 80% of V_{IN} , $V_{CL_TH} = V_{CL_MX}$ or V_{CLREF} (whichever is lower).

If a current limiting condition exists anytime for a continuous duration $> t_{CL_LA}$, then the device latches off (NCP81295) or restarts (NCP81296).

The CS pin must have no capacitive loading other than parasitic device/board capacitance to function correctly. The recommended range of R_{CS} is 1.8 – 4 k Ω (see Table 5).

CS AMP OFFSET BIAS

NCP81295/6 use an auto-zero Op-Amp with low input offset to sense current in FET with high-accuracy, and an pre-biased offset current load, I_{AZ_BIAS} is need for this Op-Amp to always keep it to maintain this low input offset (<100 μ V). The internal IMON and CS current source follow below relationship:

$$I_{OUT} = \frac{I_{CS} - I_{AZ_BIAS}}{10 \mu} \quad (\text{eq. 1})$$

and

$$I_{OUT} = \frac{I_{MON} - I_{AZ_BIAS}}{10 \mu} \quad (\text{eq. 2})$$

For typical 5 μ A I_{AZ_BIAS} , there has 0.5 A positive off-set in I_{OUT} sense.

D_OC Output (Over-current Indicator)

The D_OC pin is an open-drain output that indicates when an over-current condition exists after soft-start is complete. When the voltage on the CS pin is higher than V_{OC_TH} , D_OC is pulled low. If output current drops below V_{OC_TH} , the D_OC pin is released and gets pulled high by an external pullup resistor.

VTEMP Output (Temperature Indicator)

VTEMP is a voltage output proportional to device temperature, with an offset voltage. The VTEMP output can source much more current than it can sink, so that if multiple VTEMP outputs are connected together, the voltage of all VTEMP outputs will be driven to the voltage produced by the hottest NCP81295/6. A 100 nF capacitor or greater must be connected from the VTEMP pin to ground.

Auto-Retry Restart (NCP81296)

Under certain fault conditions, the FET is turned off and another soft-start procedure takes place. Between the fault and the new soft-start, there is a delay of t_{DLY_RETRY} . The protection features that use this hiccup mode restart are:

- Over-Current
- Short-Circuit Detection
- Over-Temperature
- Excessive Soft-Start Duration
- Gate Leakage

Protection Features

For the following protection features, the FET either latches off (NCP81295) or the FET turns off and initiates a restart (NCP81296), unless noted otherwise.

NCP81295, NCP81296

Excessive Current Limiting

If a current limiting condition exists anytime for a continuous duration $> t_{CL_LA}$, then the FET latches/restarts.

Excessive Soft-Start Duration

If $V_{OUT} < V_{OUTL_TH}$ when t_{SSF_END} expires, then the FET latches/restarts.

Short Circuit Detection

If switch current exceeds I_{SC} , the device reacts within t_{SC} , and the FET latches/restarts. The short-circuit current monitor is independent of CS, CLREF, IMON and current limit setting (cannot be changed externally).

Over-Temperature Shutdown

If the FET controller temperature $> T_{TSD}$, then the FET latches/restarts.

FET Fault Detection

The device contains various FET monitoring circuits:

- VIN to VOUT short, non-latching/non-auto-retry condition. If the device is disabled and $V_{OUT} > V_{DS_TH}$ then GOK is pulled low and the device is prevented from powering up. The device is allowed to power up once $V_{OUT} < V_{DS_OK}$.
- GATE to VIN short, non-latching/non-auto-retry condition. If the device is disabled and

$GATE (Pin 8) > V_{DG_TH}$, then GOK is pulled low and device is prevented from powering up. The device allowed to power up once $GATE < V_{DG_OK}$.

- GATE leakage – startup.
If $(GATE - V_{INF}) < V_{G_TH}$ at t_{SSF_END} , then GOK is pulled low and FET latches/restarts.
- GATE leakage – normal operation.
If $(GATE - V_{INF}) < V_{G_TH}$ for t_{GATE_FLT} time after the soft-start timer completes, then GOK is pulled low and device latches/restarts.

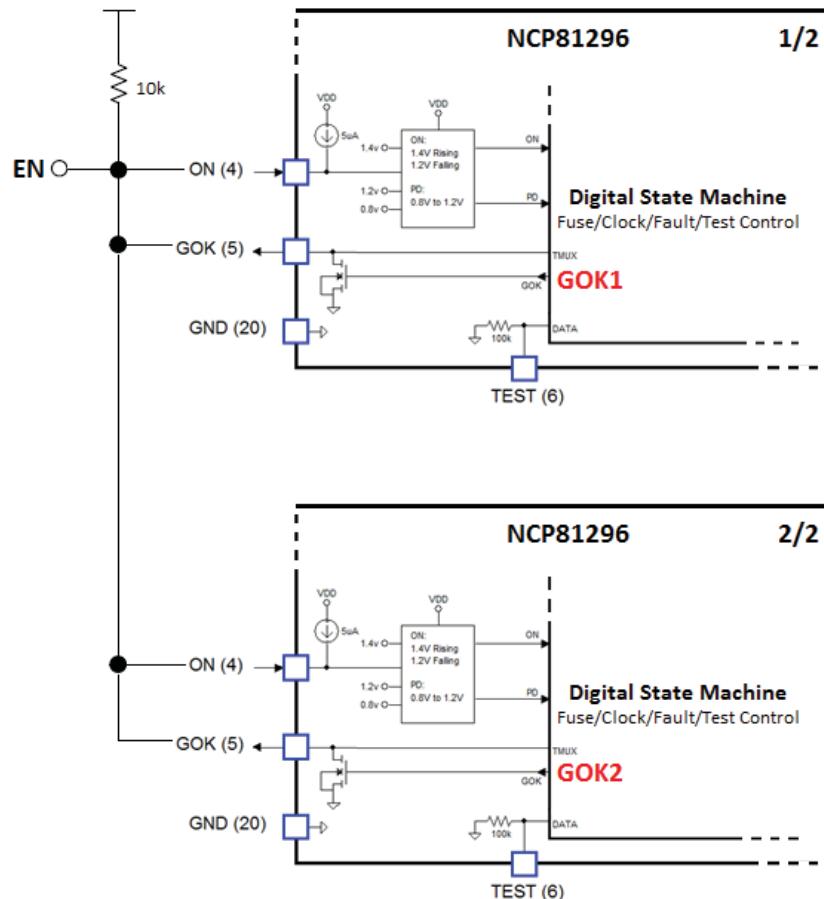
FET SOA Limits

In-built timed current limits and fault-monitoring circuits ensure the copackaged FET is always kept within SOA limits.

Multiple Fuse Power Up

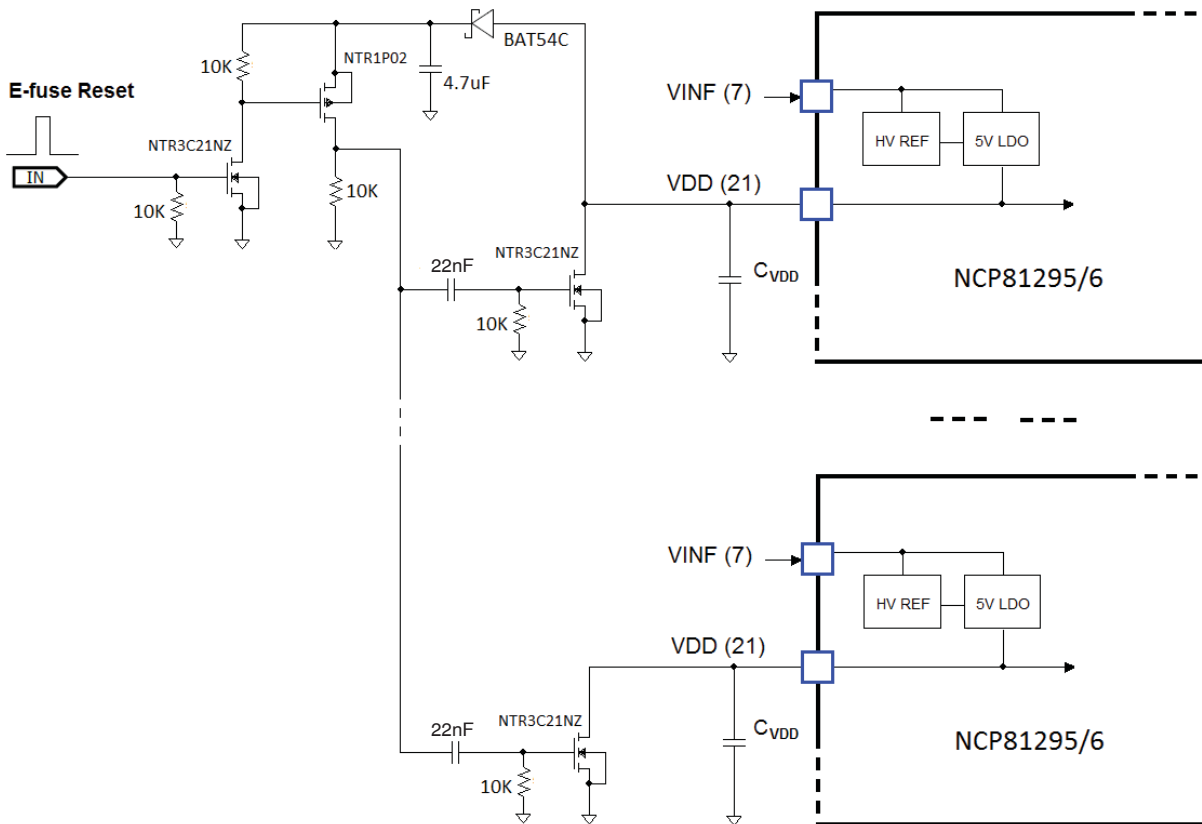
When multiple NPC81295 are paralleled together as shown in Figure 4, the NPC81295s will turn on together. Keeping the current through each switch within 1 A (typical) helps to prevent overstress on each switching during soft-start.

Due to NCP81296 is featured by Auto-Retry Mode protection, please follow the below reference schematic of NCP81296 for paralleled operation.



NCP81295, NCP81296

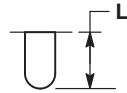
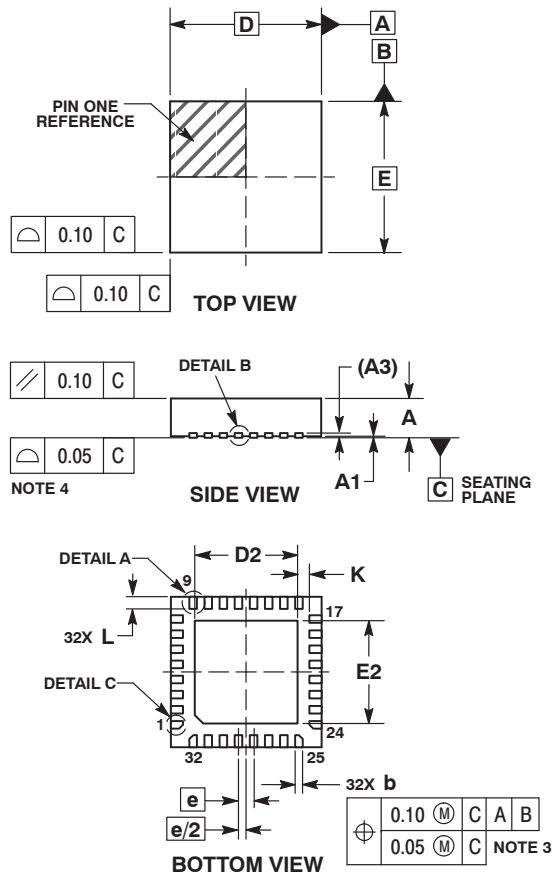
When paralleled multiple NCP81295 encounter fault, the system can recover the E-fuse by resetting their VDD with below buffer and reset circuit.



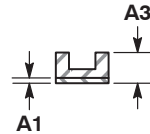
NCP81295, NCP81296

PACKAGE DIMENSIONS

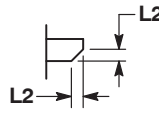
LQFN32 5x5, 0.5P
CASE 487AA
ISSUE A



DETAIL A
ALTERNATE
CONSTRUCTION



DETAIL B
ALTERNATE
CONSTRUCTION



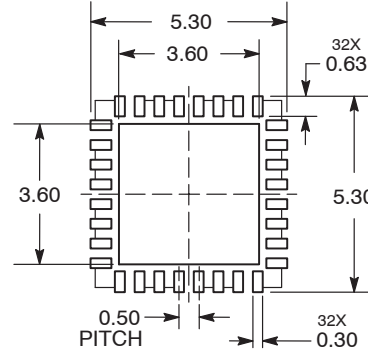
DETAIL C
4 PLACES

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

| MILLIMETERS | | |
|-------------|------|------|
| DIM | MIN | MAX |
| A | 1.20 | 1.40 |
| A1 | --- | 0.05 |
| A3 | 0.20 | REF |
| b | 0.18 | 0.30 |
| D | 5.00 | BSC |
| D2 | 3.30 | 3.50 |
| E | 5.00 | BSC |
| E2 | 3.30 | 3.50 |
| e | 0.50 | BSC |
| L | 0.30 | 0.50 |
| L2 | 0.13 | REF |

**RECOMMENDED
SOLDERING FOOTPRINT***



DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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