

# MOSFET – Power, Single N-Channel

100 V, 5.1 mΩ, 108 A

## NVMFS005N10MCL

### Features

- Small Footprint (5x6 mm) for Compact Design
- Low  $R_{DS(on)}$  to Minimize Conduction Losses
- Low  $Q_G$  and Capacitance to Minimize Driver Losses
- AEC-Q101 Qualified and PPAP Capable
- NVMFWS005N10MCL – Wettable Flank Products
- These Devices are Pb-Free, Halogen Free/BFR Free, Beryllium Free and are RoHS Compliant

### MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Value	Unit	
Drain-to-Source Voltage	$V_{DSS}$	100	V	
Gate-to-Source Voltage	$V_{GS}$	$\pm 20$	V	
Continuous Drain Current $R_{\theta JC}$ (Note 1)	Steady State	$T_C = 25^\circ\text{C}$	$I_D$ 108	A
		$T_C = 100^\circ\text{C}$	76	
Power Dissipation $R_{\theta JC}$ (Note 1)	Steady State	$T_C = 25^\circ\text{C}$	$P_D$ 131	W
		$T_C = 100^\circ\text{C}$	65	
Continuous Drain Current $R_{\theta JA}$ (Notes 1, 2)	Steady State	$T_A = 25^\circ\text{C}$	$I_D$ 18.4	A
		$T_A = 100^\circ\text{C}$	13.0	
Power Dissipation $R_{\theta JA}$ (Notes 1, 2)	Steady State	$T_A = 25^\circ\text{C}$	$P_D$ 3.8	W
		$T_A = 100^\circ\text{C}$	1.9	
Pulsed Drain Current	$T_A = 25^\circ\text{C}, t_p = 10 \mu\text{s}$	$I_{DM}$ 695	A	
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	-55 to +175	$^\circ\text{C}$	
Source Current (Body Diode)	$I_S$	109	A	
Single Pulse Drain-to-Source Avalanche Energy ( $I_{L(pk)} = 6.5 \text{ A}$ )	$E_{AS}$	365	mJ	
Lead Temperature Soldering Reflow for Soldering Purposes (1/8" from case for 10 s)	$T_L$	260	$^\circ\text{C}$	

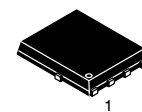
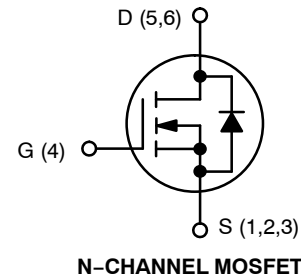
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

### THERMAL RESISTANCE RATINGS

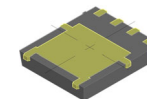
Parameter	Symbol	Value	Unit
Junction-to-Case – Steady State (Note 1)	$R_{\theta JC}$	1.15	$^\circ\text{C}/\text{W}$
Junction-to-Ambient – Steady State (Note 2)	$R_{\theta JA}$	40	

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Surface-mounted on FR4 board using 1 in<sup>2</sup> pad size, 1 oz. Cu pad.

$V_{(BR)DSS}$	$R_{DS(ON)} \text{ MAX}$	$I_D \text{ MAX}$
100 V	5.1 mΩ @ 10 V	108 A
	7.1 mΩ @ 4.5 V	

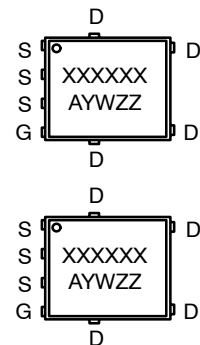


DFN5  
CASE 488AA  
STYLE 1



DFNW5  
(for WF Version)  
CASE 507BA

### MARKING DIAGRAM



XXXXXX = Specific Device Code  
A = Assembly Location  
Y = Year  
W = Work Week  
ZZ = Lot Traceability

### ORDERING INFORMATION

See detailed ordering, marking and shipping information on page 5 of this data sheet.

# NVMFS005N10MCL

## ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = 25°C unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
<b>OFF CHARACTERISTICS</b>						
Drain-to-Source Breakdown Voltage	V <sub>(BR)DSS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA	100			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	V <sub>(BR)DSS</sub> /T <sub>J</sub>	I <sub>D</sub> = 250 μA, ref to 25°C		52		mV/°C
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 100 V	T <sub>J</sub> = 25°C		1	μA
			T <sub>J</sub> = 125°C		100	
Gate-to-Source Leakage Current	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = 20 V			100	nA

## ON CHARACTERISTICS

Gate Threshold Voltage	V <sub>GS(TH)</sub>	V <sub>GS</sub> = V <sub>DS</sub> , I <sub>D</sub> = 192 μA	1		3	V
Threshold Temperature Coefficient	V <sub>GS(TH)</sub> /T <sub>J</sub>	I <sub>D</sub> = 250 μA, ref to 25°C		-5.6		mV/°C
Drain-to-Source On Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 34 A		4.2	5.1	mΩ
		V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 27 A		5.6	7.1	
Forward Transconductance	g <sub>FS</sub>	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 50 A		155		S
Gate-Resistance	R <sub>G</sub>	T <sub>A</sub> = 25°C		0.85		Ω

## CHARGES & CAPACITANCES

Input Capacitance	C <sub>ISS</sub>	V <sub>GS</sub> = 0 V, f = 1 MHz, V <sub>DS</sub> = 50 V		4100		pF
Output Capacitance	C <sub>OSS</sub>			1350		
Reverse Transfer Capacitance	C <sub>RSS</sub>			22		
Total Gate Charge	Q <sub>G(TOT)</sub>	V <sub>GS</sub> = 4.5 V, V <sub>DS</sub> = 50 V, I <sub>D</sub> = 34 A		26		nC
Total Gate Charge	Q <sub>G(TOT)</sub>	V <sub>GS</sub> = 10 V, V <sub>DS</sub> = 50 V, I <sub>D</sub> = 34 A		55		nC
				11		
				5		
				3		
Plateau Voltage	V <sub>GP</sub>			3		V
Threshold Gate Charge	Q <sub>G(TH)</sub>			6		nC

## SWITCHING CHARACTERISTICS (Note 3)

Turn-On Delay Time	t <sub>d(ON)</sub>	V <sub>GS</sub> = 10 V, V <sub>DS</sub> = 50 V, I <sub>D</sub> = 34 A, R <sub>G</sub> = 6 Ω		17		ns
Rise Time	t <sub>r</sub>			6.7		
Turn-Off Delay Time	t <sub>d(OFF)</sub>			57		
Fall Time	t <sub>f</sub>			12.3		

## DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V <sub>SD</sub>	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 34 A	T <sub>J</sub> = 25°C		0.85	1.3	V
			T <sub>J</sub> = 125°C		0.73		
Reverse Recovery Time	t <sub>RR</sub>	V <sub>GS</sub> = 0 V, di/dt = 100 A/μs, I <sub>S</sub> = 17 A		56		ns	
Reverse Recovery Charge	Q <sub>RR</sub>			54		nC	
Charge Time	t <sub>a</sub>			25		ns	
Discharge Time	t <sub>b</sub>			31		ns	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Switching characteristics are independent of operating junction temperatures

TYPICAL CHARACTERISTICS

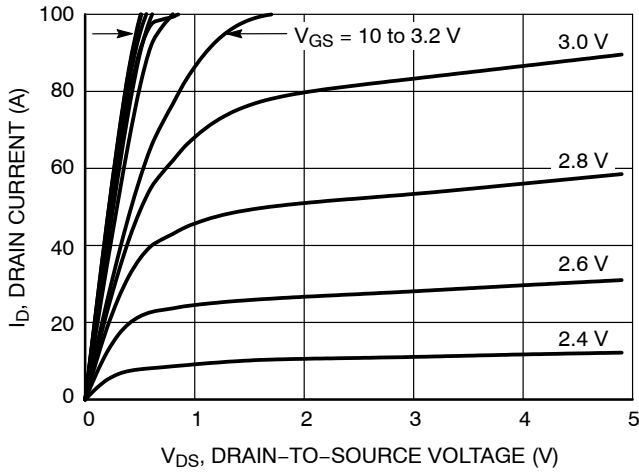


Figure 1. On-Region Characteristics

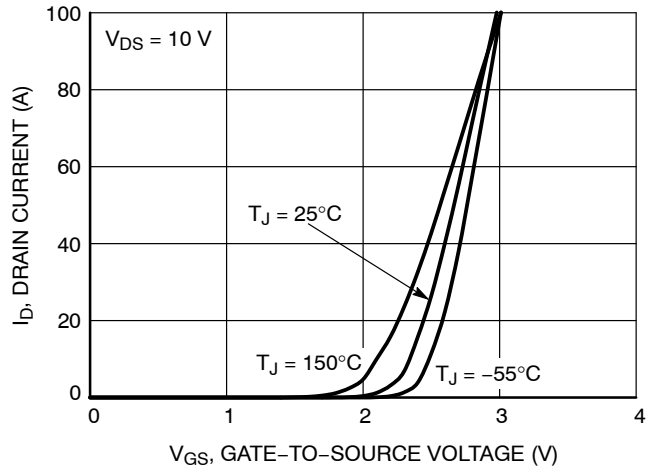


Figure 2. Transfer Characteristics

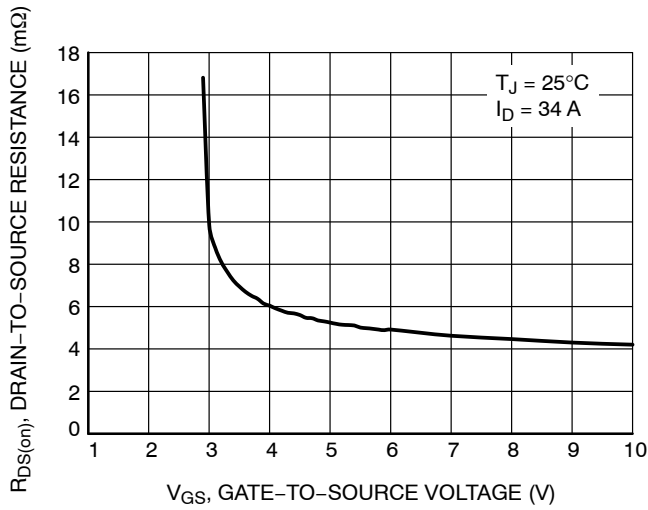


Figure 3. On-Resistance vs. Gate-to-Source Voltage

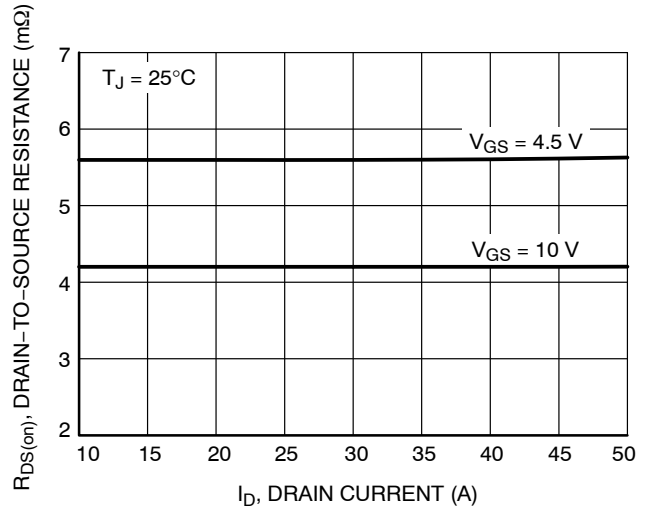


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

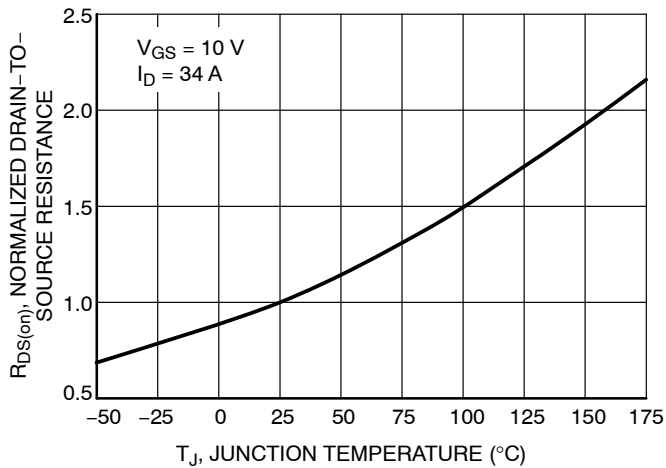


Figure 5. On-Resistance Variation with Temperature

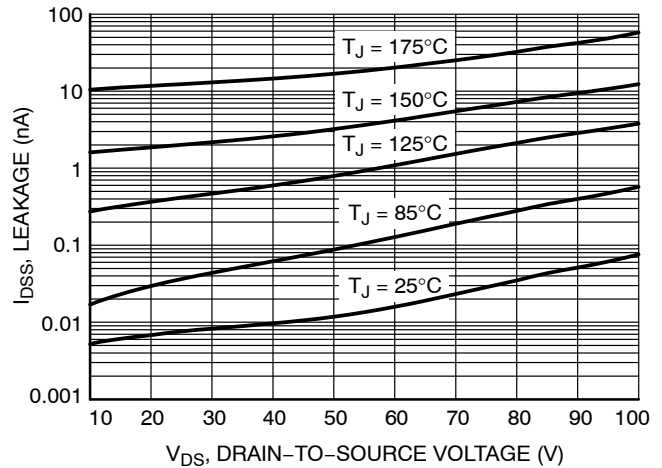


Figure 6. Drain-to-Source Leakage Current vs. Voltage

# NVMFS005N10MCL

## TYPICAL CHARACTERISTICS

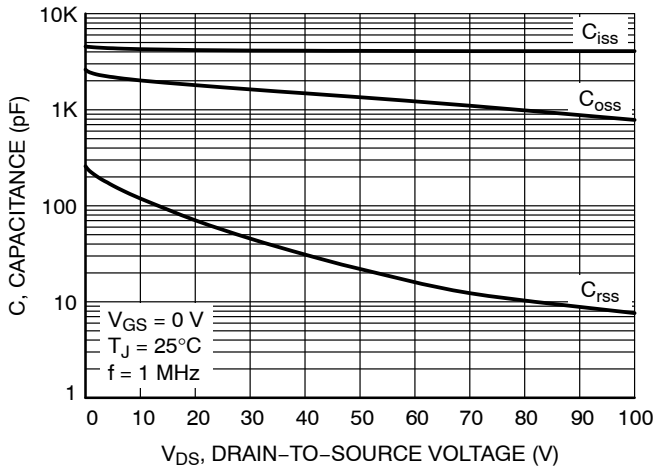


Figure 7. Capacitance Variation

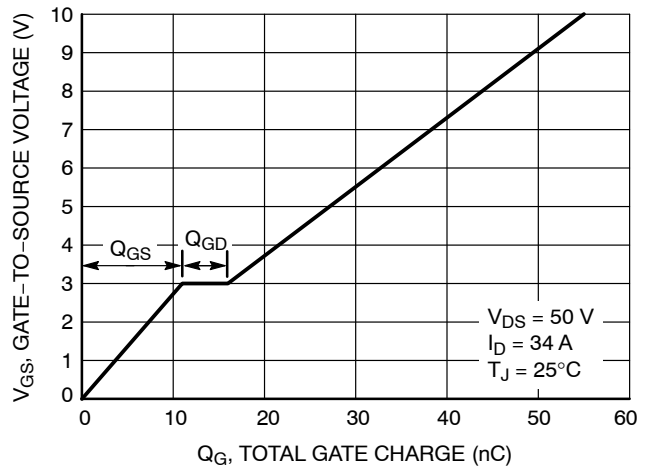


Figure 8. Gate-to-Source vs. Total Charge

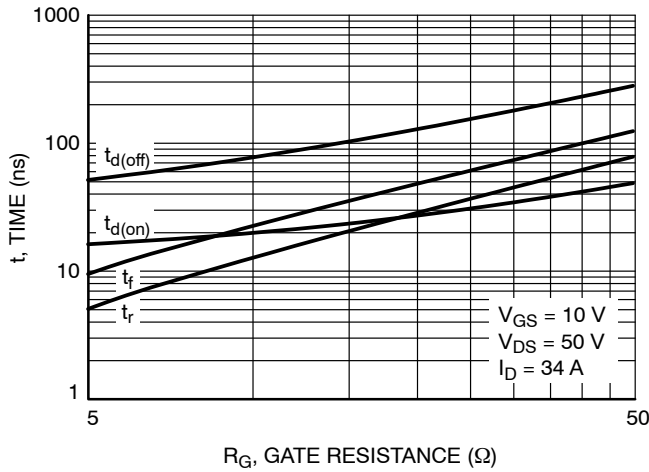


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

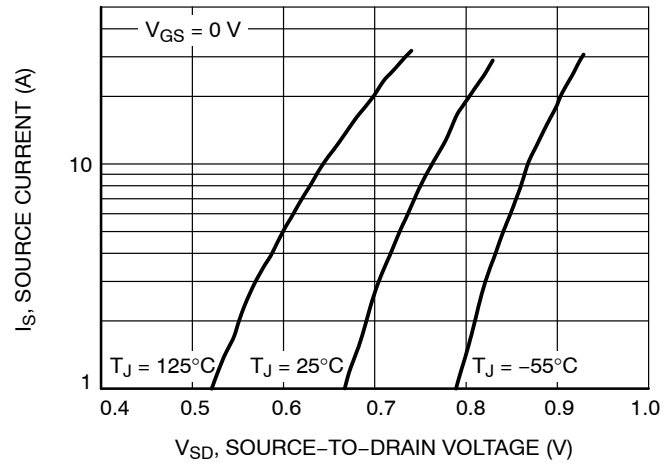


Figure 10. Diode Forward Voltage vs. Current

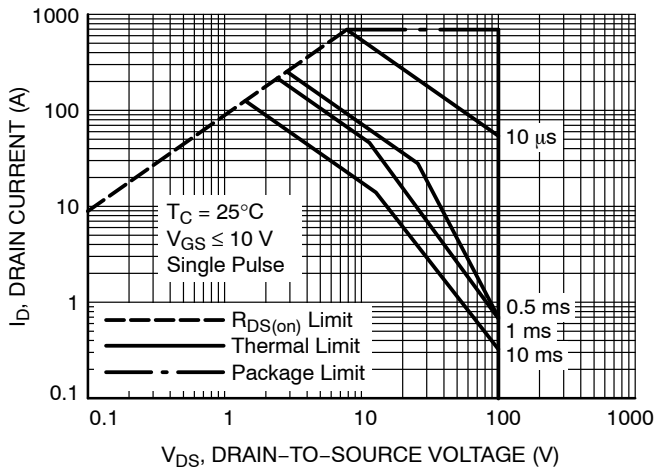


Figure 11. Maximum Rated Forward Biased Safe Operating Area

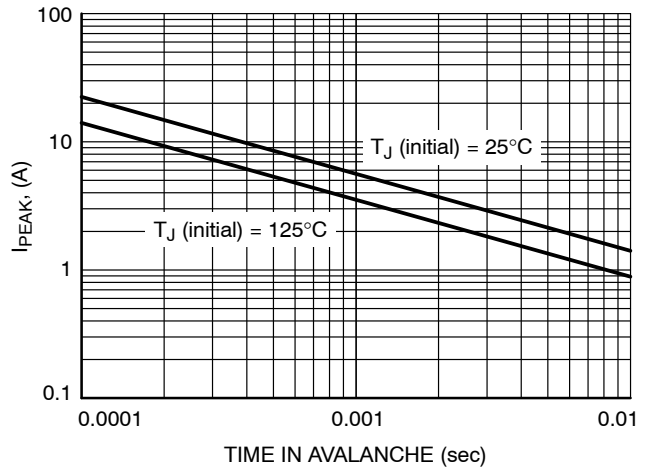


Figure 12. Maximum Drain Current vs. Time in Avalanche

# NVMFS005N10MCL

## TYPICAL CHARACTERISTICS

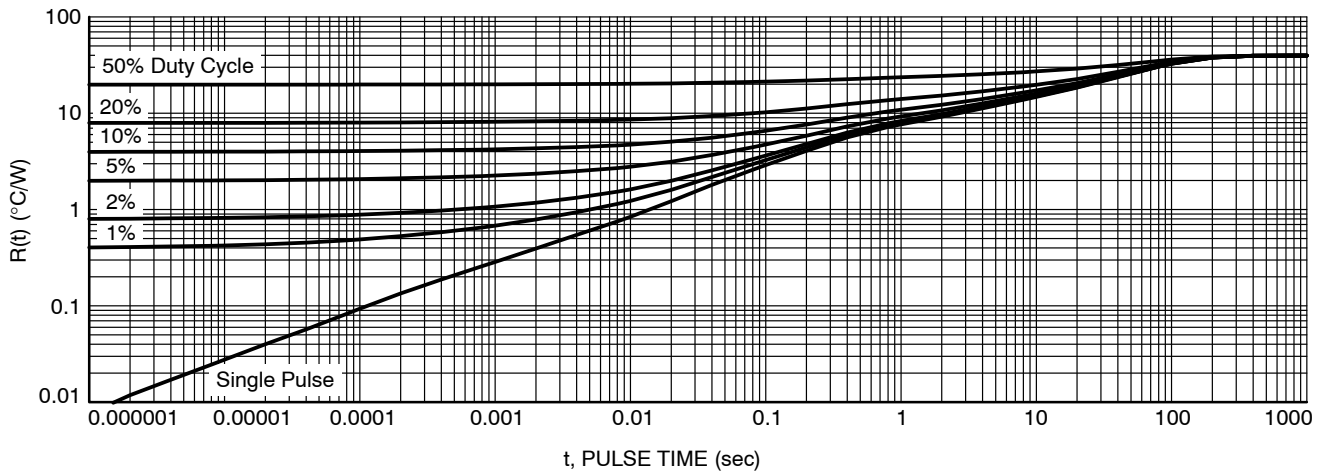


Figure 13. Thermal Response

### DEVICE ORDERING INFORMATION

Device	Marking	Package	Shipping <sup>†</sup>
NVMFS005N10MCLT1G	005L10	DFN5 (Pb-Free)	1500 / Tape & Reel
NVMFWS005N10MCLT1G	005W10	DFN5 (Wettable Flank, Pb-Free)	1500 / Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# NVMFS005N10MCL

## PACKAGE DIMENSIONS

DFN5 5x6, 1.27P  
(SO-8FL)  
CASE 488AA  
ISSUE N

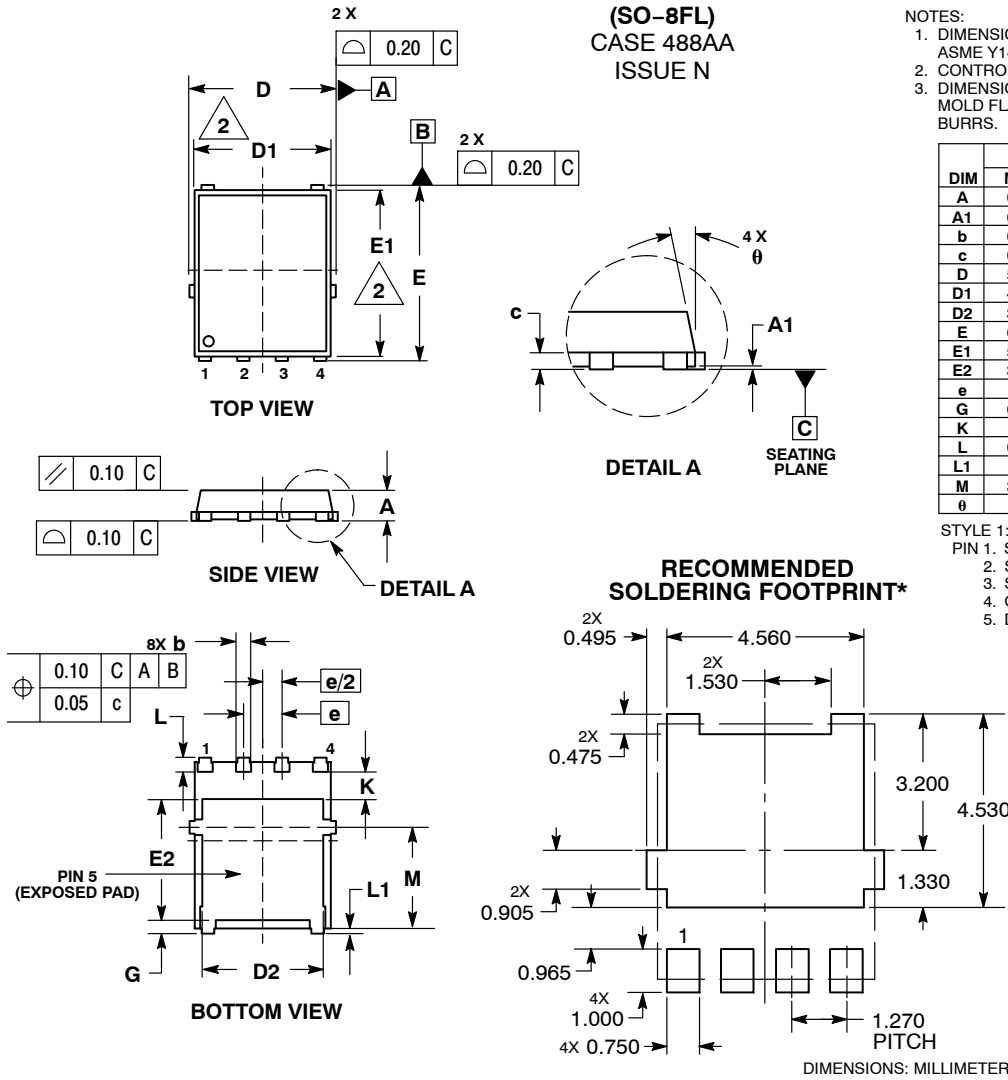
NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD FLASH PROTRUSIONS OR GATE BURRS.

MILLIMETERS			
DIM	MIN	NOM	MAX
A	0.90	1.00	1.10
A1	0.00	---	0.05
b	0.33	0.41	0.51
c	0.23	0.28	0.33
D	5.00	5.15	5.30
D1	4.70	4.90	5.10
D2	3.80	4.00	4.20
E	6.00	6.15	6.30
E1	5.70	5.90	6.10
E2	3.45	3.65	3.85
e	1.27 BSC		
G	0.51	0.575	0.71
K	1.20	1.35	1.50
L	0.51	0.575	0.71
L1	0.125 REF		
M	3.00	3.40	3.80
θ	0°	---	12°

STYLE 1:

1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN



\*For additional information on our Pb-Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

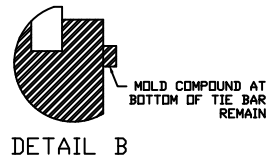
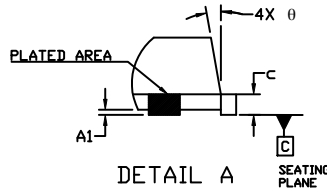
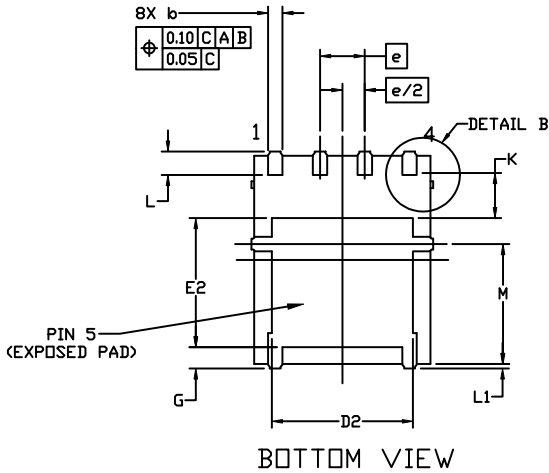
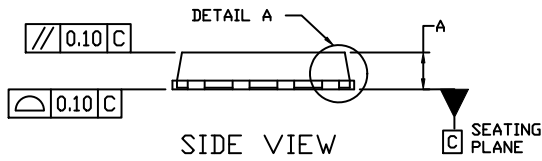
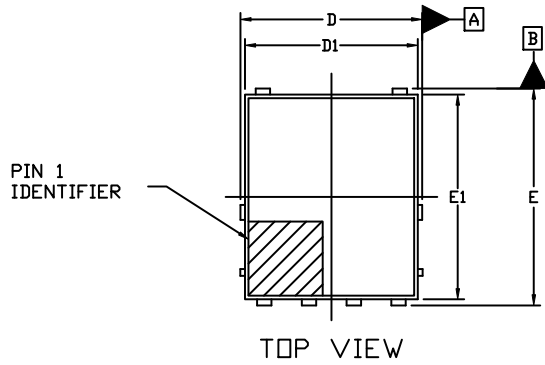
# NVMFS005N10MCL

## PACKAGE DIMENSIONS

### DFNW5 5x6 (FULL-CUT SO8FL WF)

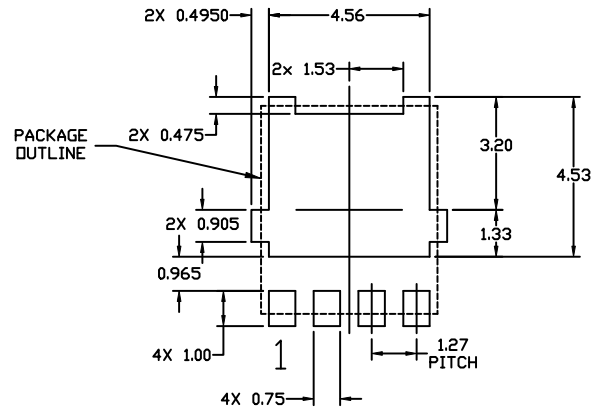
CASE 507BA

ISSUE A



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
  2. CONTROLLING DIMENSION: MILLIMETERS
  3. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
  4. THIS PACKAGE CONTAINS WETTABLE FLANK DESIGN FEATURES TO AID IN FILLET FORMATION ON THE LEADS DURING MOUNTING.

MILLIMETERS			
DIM	MIN.	NOM.	MAX.
A	0.90	1.00	1.10
A1	0.00	---	0.05
b	0.33	0.41	0.51
c	0.23	0.28	0.33
D	5.00	5.15	5.30
D1	4.70	4.90	5.10
D2	3.80	4.00	4.20
E	6.00	6.15	6.30
E1	5.70	5.90	6.10
E2	3.45	3.65	3.85
e	1.27 BSC		
G	0.51	0.575	0.71
K	1.20	1.35	1.50
L	0.51	0.575	0.71
L1	0.150 REF		
M	3.00	3.40	3.80
$\theta$	0°	---	12°



### RECOMMENDED MOUNTING FOOTPRINT

- \* For additional information on our Pb-Free strategy and soldering details, please download the ION Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

# NVMFS005N10MCL

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