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ON Semiconductor®

FDD5N50FTM-WS

N-Channel UniFET™ FRFET® MOSFET

500 V, 3.5 A, 1.55 Ω

Features

- $R_{DS(on)}$ = 1.25Ω (Typ.) @ V_{GS} = 10 V, I_D = 1.75 A
- Low Gate Charge (Typ. 11 nC)
- Low C_{rss} (Typ. 5 pF)
- Fast Switching
- 100% Avalanche Tested
- Improved dv/dt Capability
- RoHS Compliant

Applications

- LCD/LED/PDP TV
- Lighting
- Uninterruptible Power Supply
- AC-DC Power Supply

Description

UniFET™ MOSFET is ON Semiconductor's high voltage MOSFET family based on planar stripe and DMOS technology. This MOSFET is tailored to reduce on-state resistance, and to provide better switching performance and higher avalanche energy strength. The body diode's reverse recovery performance of UniFET FRFET® MOSFET has been enhanced by lifetime control. Its trr is less than 100nsec and the reverse dv/dt immunity is 15V/ns while normal planar MOSFETs have over 200nsec and 4.5V/nsec respectively. Therefore, it can remove additional component and improve system reliability in certain applications in which the performance of MOSFET's body diode is significant. This device family is suitable for switching power converter applications such as power factor correction (PFC), flat panel display (FPD) TV power, ATX and electronic lamp ballasts.

D-PAK
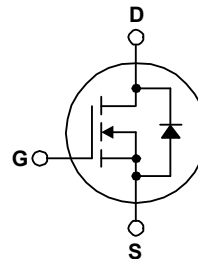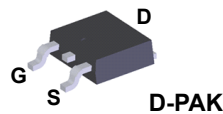
MOSFET Maximum Ratings T_C = 25°C unless otherwise noted.

Symbol	Parameter			Ratings	Units
V_{DSS}	Drain to Source Voltage			500	V
V_{GSS}	Gate to Source Voltage			±30	V
I_D	Drain Current	- Continuous (T_C = 25°C)		3.5	A
		- Continuous (T_C = 100°C)		2.1	
I_{DM}	Drain Current	- Pulsed	(Note 1)	14	A
E_{AS}	Single Pulsed Avalanche Energy		(Note 2)	257	mJ
I_{AR}	Avalanche Current		(Note 1)	3.5	A
E_{AR}	Repetitive Avalanche Energy		(Note 1)	4	mJ
dv/dt	Peak Diode Recovery dv/dt		(Note 3)	4.5	V/ns
P_D	Power Dissipation	(T_C = 25°C)		40	W
		- Derate Above 25°C		0.3	W/°C
T_J, T_{STG}	Operating and Storage Temperature Range			-55 to +150	°C
T_L	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 Seconds			300	°C

Thermal Characteristics

Symbol	Parameter	Ratings	Units
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	1.4	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max.	110	

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Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FDD5N50FTM-WS	FDD5N50F	D-PAK	Tape and Reel	330 mm	16 mm	2500 units

Electrical Characteristics $T_C = 25^oC$ unless otherwise noted.

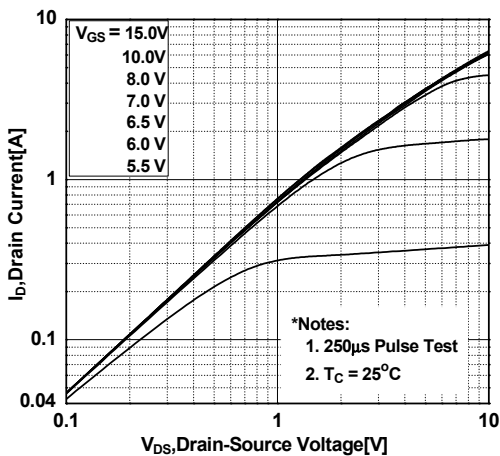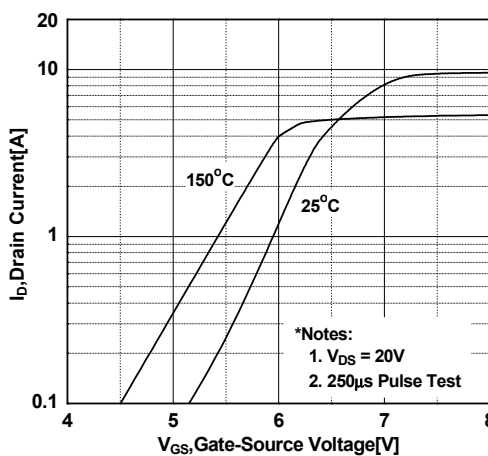| Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
Off Characteristics						
BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250\ \mu A$, $V_{GS} = 0\ V$, $T_J = 25^oC$	500	-	-	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu A$, Referenced to 25^oC	-	0.6	-	V/^oC
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 500\ V$, $V_{GS} = 0\ V$	-	-	10	μA
		$V_{DS} = 400\ V$, $T_C = 125^oC$		-	100	
I_{GSS}	Gate to Body Leakage Current	$V_{GS} = \pm30\ V$, $V_{DS} = 0\ V$	-	-	±100	nA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = 250\ \mu A$	3.0	-	5.0	V
$R_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\ V$, $I_D = 1.75\ A$	-	1.25	1.55	Ω
g_{FS}	Forward Transconductance	$V_{DS} = 20\ V$, $I_D = 1.75\ A$	-	4.3	-	S
Dynamic Characteristics						
C_{iss}	Input Capacitance	$V_{DS} = 25\ V$, $V_{GS} = 0\ V$ f = 1 MHz	-	490	650	pF
C_{oss}	Output Capacitance		-	66	88	pF
C_{rss}	Reverse Transfer Capacitance		-	5	7.5	pF
$Q_{g(tot)}$	Total Gate Charge at 10V	$V_{DS} = 400\ V$, $I_D = 5\ A$, $V_{GS} = 10\ V$ (Note 4)	-	11	15	nC
Q_{gs}	Gate to Source Gate Charge		-	3	-	nC
Q_{gd}	Gate to Drain "Miller" Charge		-	5	-	nC
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 250\ V$, $I_D = 5\ A$ $R_G = 25\ \Omega$ (Note 4)	-	13	36	ns
t_r	Turn-On Rise Time		-	22	54	ns
$t_{d(off)}$	Turn-Off Delay Time		-	28	66	ns
t_f	Turn-Off Fall Time		-	20	50	ns
Drain-Source Diode Characteristics						
I_S	Maximum Continuous Drain to Source Diode Forward Current		-	-	3.5	A
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current		-	-	14	A
V_{SD}	Drain to Source Diode Forward Voltage	$V_{GS} = 0\ V$, $I_{SD} = 3.5\ A$	-	-	1.5	V
t_{rr}	Reverse Recovery Time	$V_{GS} = 0\ V$, $I_{SD} = 5\ A$ $dI_F/dt = 100\ A/\mu s$	-	65	-	ns
Q_{rr}	Reverse Recovery Charge		-	0.120	-	μC

Notes:
1: Repetitive rating: pulse-width limited by maximum junction temperature.
2: L = 42 mH, I_{AS} = 3.5 A, V_{DD} = 50 V, R_G = 25 Ω, starting T_J = 25°C.
3: $I_{SD} \le 3.5\ A$, di/dt ≤ 200 A/μs, $V_{DD} \le BV_{DSS}$, starting T_J = 25°C.
4: Essentially independent of operating temperature typical characteristics.
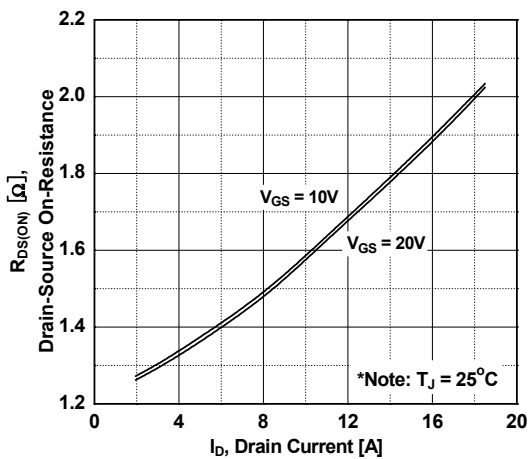
Typical Performance Characteristics
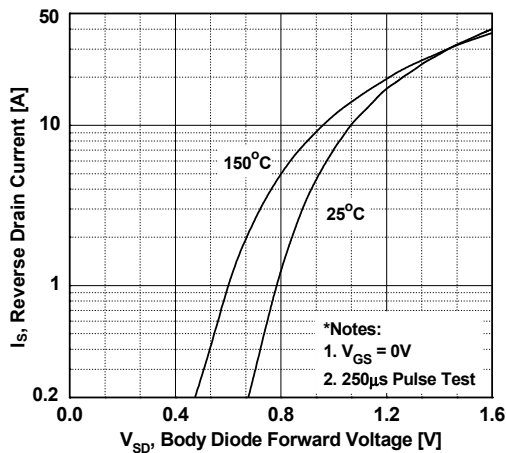
Figure 1. On-Region Characteristics

V_{GS} = 15.0V
10.0V
8.0 V
7.0 V
6.5 V
6.0 V
5.5 V

*Notes:
1. 250µs Pulse Test
2. T_C = 25°C

I_D,Drain Current[A]

V_{DS},Drain-Source Voltage[V]

Figure 2. Transfer Characteristics

150°C
25°C

*Notes:
1. V_{DS} = 20V
2. 250µs Pulse Test

I_D,Drain Current[A]

V_{GS},Gate-Source Voltage[V]

Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

V_{GS} = 10V
V_{GS} = 20V

*Note: T_J = 25°C

$R_{DS(ON)}$ [Ω], Drain-Source On-Resistance

I_D, Drain Current [A]

Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

150°C
25°C

*Notes:
1. V_{GS} = 0V
2. 250µs Pulse Test

I_S, Reverse Drain Current [A]

V_{SD}, Body Diode Forward Voltage [V]

Figure 5. Capacitance Characteristics

C_{iss} = C_{gs} + C_{gd} (C_{ds} = shorted)
C_{oss} = C_{ds} + C_{gd}
C_{rss} = C_{gd}

*Note:
1. V_{GS} = 0V
2. f = 1MHz

C_{iss}
C_{oss}
C_{rss}

Capacitances [pF]

V_{DS}, Drain-Source Voltage [V]
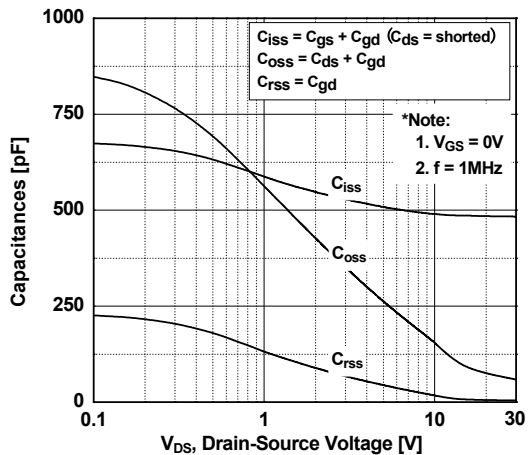
Figure 6. Gate Charge Characteristics

V_{DS} = 100V
V_{DS} = 250V
V_{DS} = 400V

*Note: I_D = 5A

V_{GS}, Gate-Source Voltage [V]

Q_g, Total Gate Charge [nC]
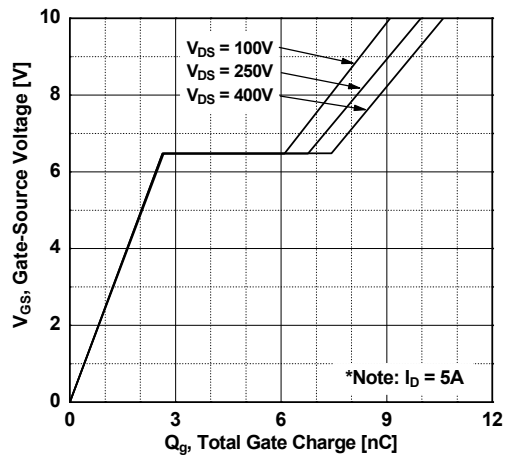
Typical Performance Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

*Notes:
1. $V_{GS} = 0V$
2. $I_D = 250\mu A$
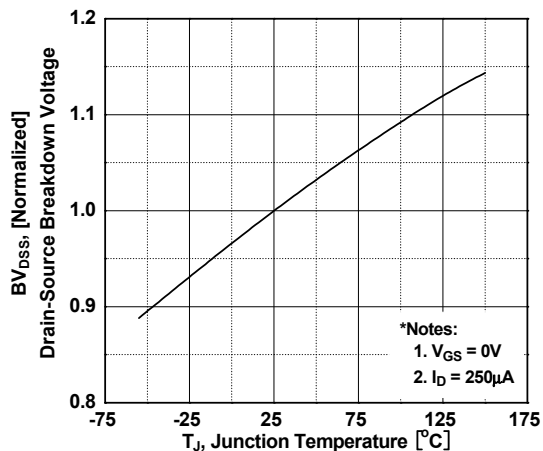
Figure 8. Maximum Safe Operating Area

Operation in This Area is Limited by $R_{DS(on)}$

40μs
100μs
1ms
10ms
DC

*Notes:
1. $T_C = 25^oC$
2. $T_J = 150^oC$
3. Single Pulse
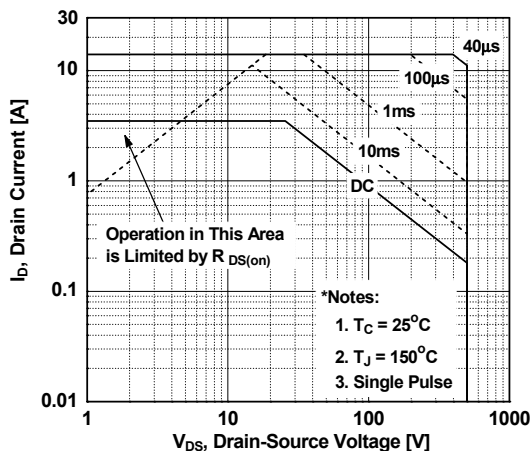
Figure 9. Maximum Drain Current
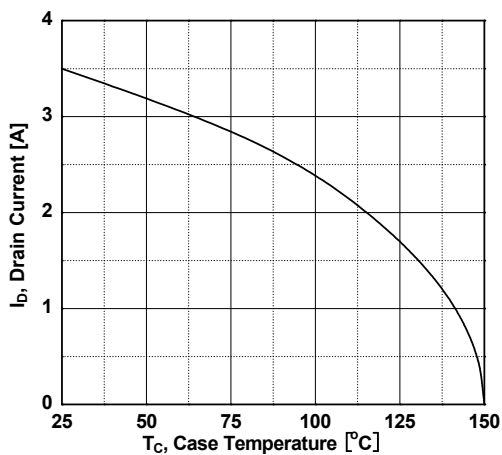
Figure 10. Transient Thermal Response Curve

0.5
0.2
0.1
0.05
0.02
0.01
Single pulse

P_{DM}

t_1
t_2

*Notes:
1. $Z_{\theta JC}(t) = 1.4^oC/W$ Max.
2. Duty Factor, $D = t_1/t_2$
3. $T_{JM} - T_C = P_{DM} * Z_{\theta JC}(t)$
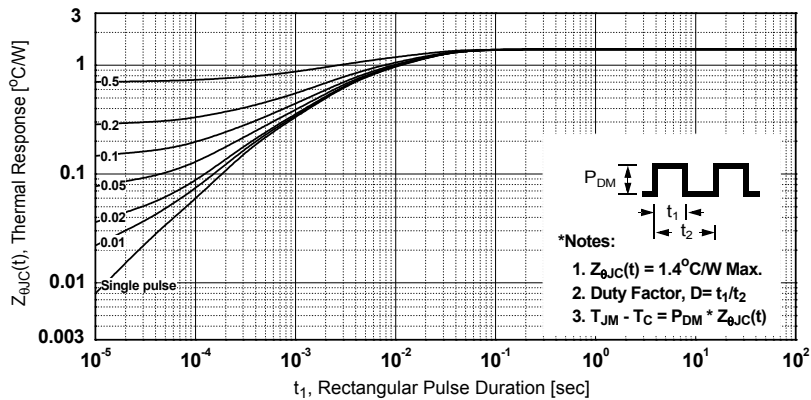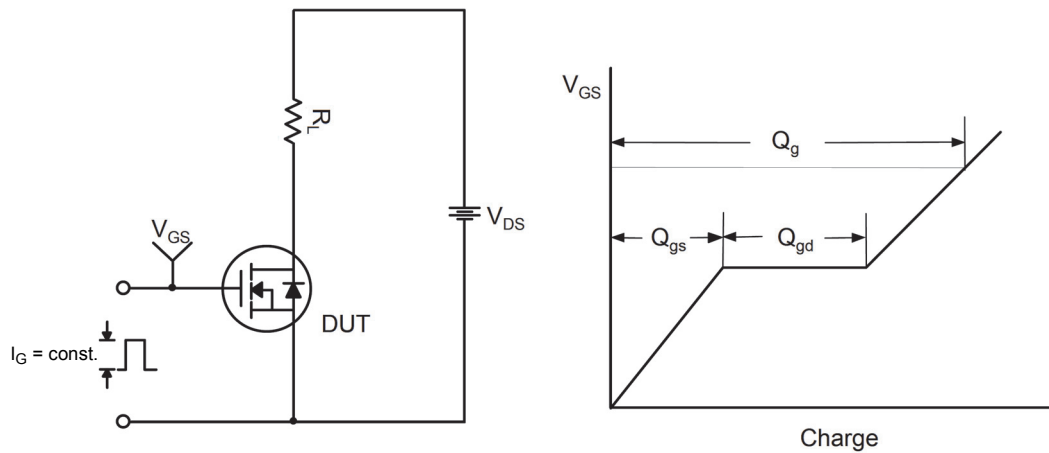
Figure 11. Gate Charge Test Circuit & Waveform
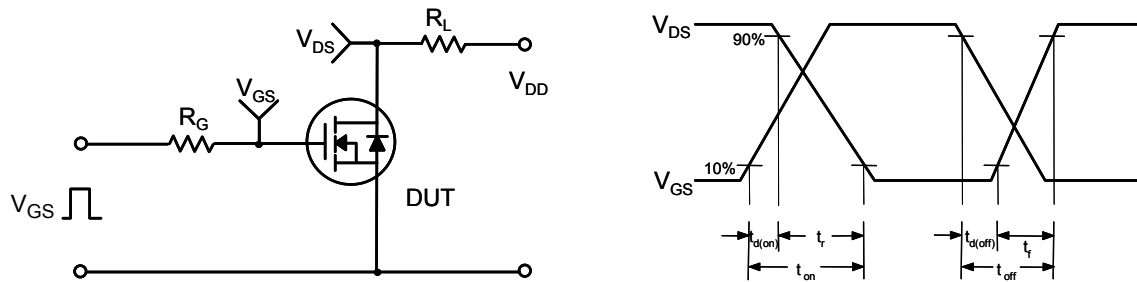
Figure 12. Resistive Switching Test Circuit & Waveforms

$$E_{AS} = \frac{1}{2} L I_{AS}^2$$
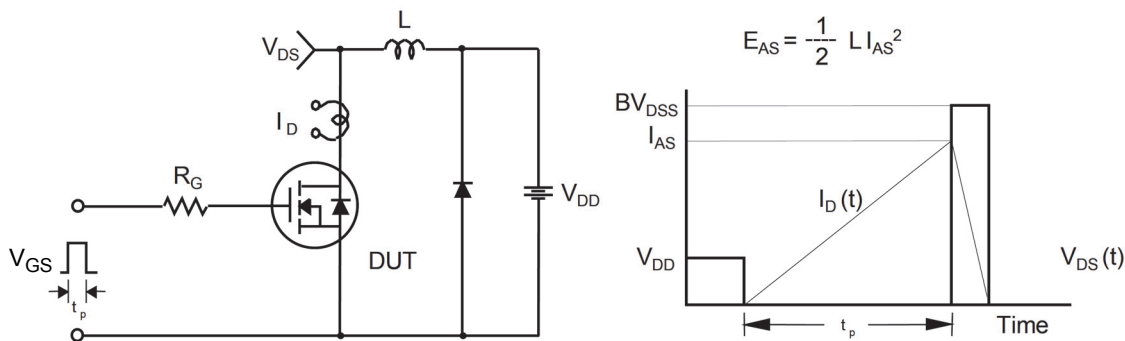
Figure 13. Unclamped Inductive Switching Test Circuit & Waveforms

DUT

V_{DS}

I_{SD}

L

Driver

R_G

Same Type
as DUT

V_{DD}

V_{GS}

• dv/dt controlled by R_G
• I_{SD} controlled by pulse period

V_{GS}
(Driver)

$$D = \frac{\text{Gate Pulse Width}}{\text{Gate Pulse Period}}$$

10V

I_{SD}
(DUT)

I_{FM} , Body Diode Forward Current

di/dt

I_{RM}

Body Diode Reverse Current

V_{DS}
(DUT)

Body Diode Recovery dv/dt

V_{SD}

V_{DD}

Body Diode
Forward Voltage Drop
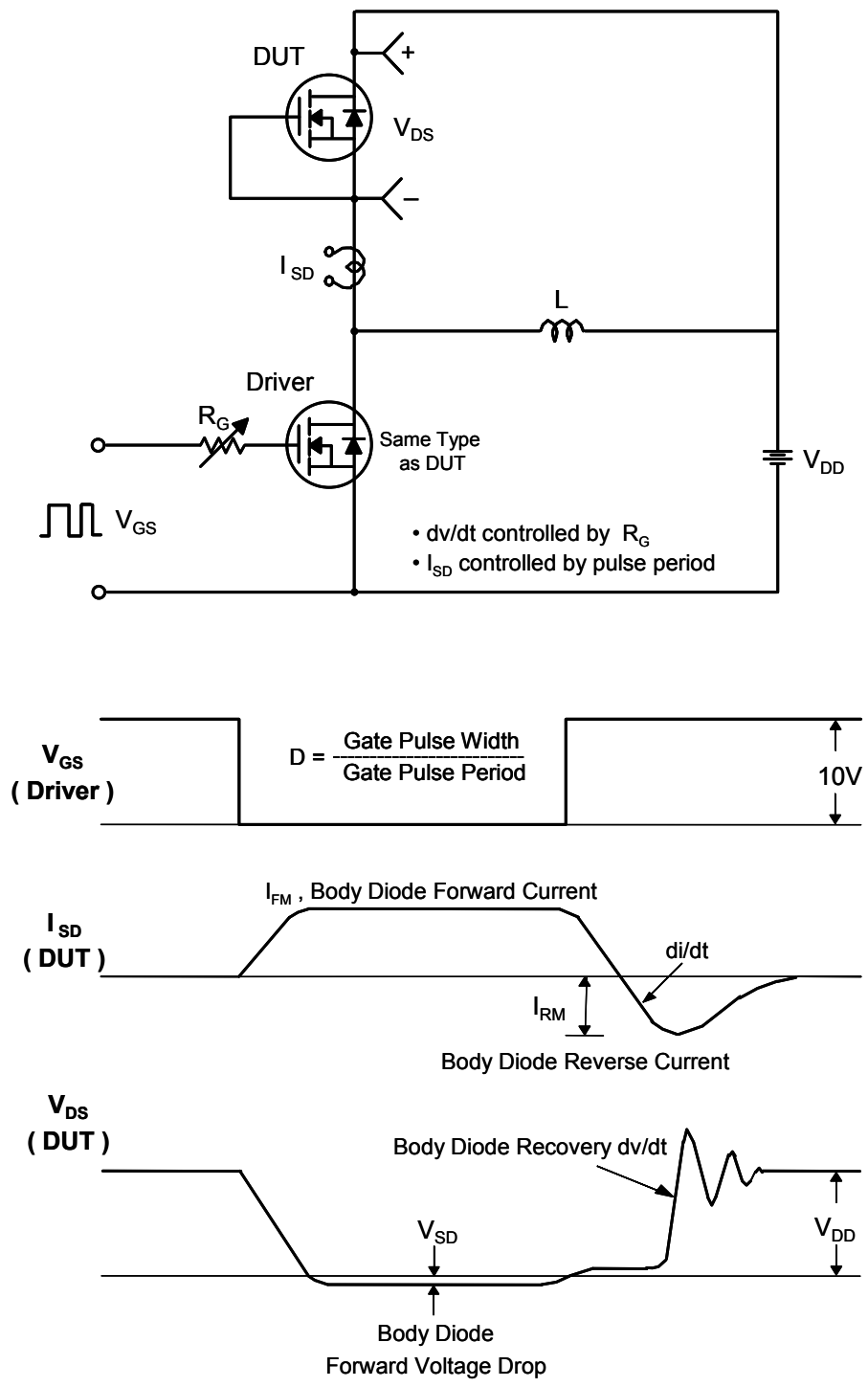
Figure 14. Peak Diode Recovery dv/dt Test Circuit & Waveforms

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