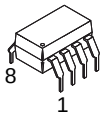
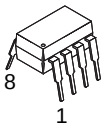
2 A Output Current, High Speed MOSFET Gate Driver Optocoupler

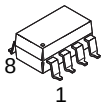
FOD3180



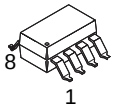
PDIP8 6.6x3.81, 2.54P
CASE 646BW



PDIP8 9.655x6.6, 2.54P
CASE 646CQ



PDIP8 GW
CASE 709AC



PDIP8 GW
CASE 709AD

Description

The FOD3180 is a 2 A Output Current, High Speed MOSFET Gate Drive Optocoupler. It consists of a aluminium gallium arsenide (AlGaAs) light emitting diode optically coupled to a CMOS detector with PMOS and NMOS output power transistors integrated circuit power stage. It is ideally suited for high frequency driving of power MOSFETs used in Plasma Display Panels (PDPs), motor control inverter applications and high performance DC/DC converters.

The device is packaged in an 8−pin dual in−line housing compatible with 260°C reflow processes for lead free solder compliance.

Features

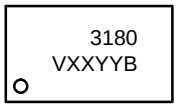
- Guaranteed Operating Temperature Range of −40°C to +100°C
- 2 A Minimum Peak Output Current
- High Speed Response: 200 ns Max Propagation Delay over Temperature Range
- 250 kHz Maximum Switching Speed
- 30 ns Typ Pulse Width Distortion
- Wide V_{CC} Operating Range: 10 V to 20 V
- 5000 Vrms, 1 Minute Isolation
- Under Voltage Lockout Protection (UVLO) with Hysteresis
- Minimum Creepage Distance of 7.0 mm
- Minimum Clearance Distance of 7.0 mm
- C−UL, UL and VDE* Approved
- $R_{DS(ON)}$ of 1.5 Ω (Typ.) Offers Lower Power Dissipation
- 15 kV/μs Minimum Common Mode Rejection
- These are Pb−Free Devices

Applications

- Plasma Display Panel
- High Performance DC/DC Convertor
- High Performance Switch Mode Power Supply
- High Performance Uninterruptible Power Supply
- Isolated Power MOSFET Gate Drive

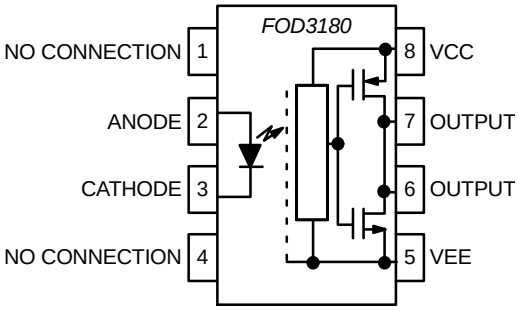
*Requires “V” ordering option

MARKING DIAGRAM



3180 = Device Number
V = VDE Mark (NOTE: Only Appears on Parts Ordered with VDE Option − See Order Table)
XX = Two Digit Year Code, e.g., ‘03’
YY = Two Digit Work Week, Ranging from ‘01’ to ‘53’
B = Assembly Package Code

FUNCTIONAL BLOCK DIAGRAM



NOTE: A 0.1 μF bypass capacitor must be connected between pins 5 and 8.

ORDERING INFORMATION

See detailed ordering and shipping information on page 9 of this data sheet.

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Value	Unit
T_{STG}	Storage Temperature	−40 to +125	°C
T_{OPR}	Operating Temperature	−40 to +100	°C
T_J	Junction Temperature	−40 to +125	°C
TSOL	Lead Solder Temperature	260 for 10 sec.	°C
$I_{F(AVG)}$	Average Input Current (Note 1)	25	mA
$I_{F(tr, tf)}$	LED Current Minimum Rate of Rise/Fall	250	ns
$I_{F(TRAN)}$	Peak Transient Input Current (<1 μs Pulse Width, 300 pps)	1.0	A
V_R	Reverse Input Voltage	5	V
$I_{OH(PEAK)}$	“High” Peak Output Current (Note 2)	2.5	A
$I_{OL(PEAK)}$	“Low” Peak Output Current (Note 2)	2.5	A
$V_{CC} – V_{EE}$	Supply Voltage	−0.5 to 25	V
$V_{O(PEAK)}$	Output Voltage	0 to V_{CC}	V
P_O	Output Power Dissipation (Note 3)	250	mW
P_D	Total Power Dissipation (Note 4)	295	mW

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Derate linearly above +70°C free air temperature at a rate of 0.3 mA/°C.
2. The output currents I_{OH} and I_{OL} are specified with a capacitive current limited load = (3 x 0.01 μF) + 0.5 Ω, frequency = 8 kHz, 50% DF.
3. Derate linearly above +87°C, free air temperature at the rate of 0.77 mW/°C. Refer to Figure 13.
4. No derating required across operating temperature range.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
$V_{CC} – V_{EE}$	Power Supply	10 to 20	V
$I_{F(ON)}$	Input Current (ON)	10 to 16	mA
$V_{F(OFF)}$	Input Voltage (OFF)	−3.0 to 0.8	V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

ELECTRICAL−OPTICAL CHARACTERISTICS (DC) (Over recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Test Conditions	Min	Typ*	Max	Unit
I_{OH}	High Level Output Current (Note 5) (Note 6)	V_{OH} = (V_{CC} – V_{EE} – 1 V)	0.5	–	–	A
		V_{OH} = (V_{CC} – V_{EE} – 3 V)	2.0	–	–	
I_{OL}	Low Level Output Current (Note 5) (Note 6)	V_{OL} = (V_{CC} – V_{EE} – 1 V)	0.5	–	–	A
		V_{OL} = (V_{CC} – V_{EE} – 3 V)	2.0	–	–	
V_{OH}	High Level Output Voltage (Note 7) (Note 8)	I_O = −100 mA	V_{CC} – 0.5	–	–	V
V_{OL}	Low Level Output Voltage (Note 7) (Note 8)	I_O = 100 mA	–	–	V_{EE} + 0.5	V
I_{CCH}	High Level Supply Current	Output Open, I_F = 10 to 16 mA	–	4.8	6.0	mA
I_{CCL}	Low Level Supply Current	Output Open, V_F = −3.0 to 0.8 V	–	5.0	6.0	mA
I_{FLH}	Threshold Input Current Low to High	I_O = 0 mA, V_O > 5 V	–	–	8.0	mA
V_{FHL}	Threshold Input Voltage High to Low	I_O = 0 mA, V_O < 5 V	0.8	–	–	V
V_F	Input Forward Voltage	I_F = 10 mA	1.2	1.43	1.8	V
ΔV_F / T_A	Temperature Coefficient of Forward Voltage	I_F = 10 mA	–	−1.5	–	mV/°C
VU_{VLO+}	UVLO Threshold	V_O > 5 V, I_F = 10 mA	–	8.3	–	V
$V_{UVLO–}$		V_O < 5 V, I_F = 10 mA	–	7.7	–	V
$UVLO_{HYST}$	UVLO Hysteresis		–	0.6	–	V
BV_R	Input Reverse Breakdown Voltage	I_R = 10 μA	5	–	–	V
C_{IN}	Input Capacitance	f = 1 MHz, V_F = 0 V	–	60	–	pF

*Typical values at T_A = 25°C

5. The output currents I_{OH} and I_{OL} are specified with a capacitive current limited load = (3 x 0.01 μF) + 0.5 Ω, frequency = 8 kHz, 50% DF.
6. The output currents I_{OH} and I_{OL} are specified with a capacitive current limited load = (3 x 0.01 μF) + 8.5 Ω, frequency = 8 kHz, 50% DF.
7. In this test, V_{OH} is measured with a dc load current of 100 mA. When driving capacitive load V_{OH} will approach V_{CC} as I_{OH} approaches zero amps.
8. Maximum pulse width = 1 ms, maximum duty cycle = 20%.

SWITCHING CHARACTERISTICS (Over recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Test Conditions	Min	Typ*	Max	Unit
t_{PLH}	Propagation Delay Time to High Output Level (Note 9)	I_F = 10 mA, R_g = 10 Ω, f = 250 kHz, Duty Cycle = 50%, C_g = 10 nF	50	135	200	ns
t_{PHL}	Propagation Delay Time to Low Output Level (Note 9)		50	105	200	ns
P_{WD}	Pulse Width Distortion (Note 10)		–	–	65	ns
P_{DD} (t_{PHL} – t_{PLH})	Propagation Delay Difference Between Any Two Parts (Note 11)		−90	–	90	ns
t_r	Rise Time	C_L = 10nF, R_g = 10 Ω	–	75	–	ns
t_f	Fall Time		–	55	–	ns
$t_{UVLO\ ON}$	UVLO Turn On Delay		–	2.0	–	μs
$t_{UVLO\ OFF}$	UVLO Turn Off Delay		–	0.3	–	μs
| CM_H |	Output High Level Common Mode Transient Immunity (Note 12) (Note 13)	T_A = +25°C, I_f = 10 to 16 mA, V_{CM} = 1.5 kV, V_{CC} = 20 V	15	–	–	kV/μs
| CM_L |	Output Low Level Common Mode Transient Immunity (Note 12) (Note 14)	T_A = +25°C, V_f = 0 V, V_{CM} = 1.5 kV, V_{CC} = 20 V	15	–	–	kV/μs

*Typical values at T_A = 25°C

9. t_{PHL} propagation delay is measured from the 50% level on the falling edge of the input pulse to the 50% level of the falling edge of the V_O signal. t_{PLH} propagation delay is measured from the 50% level on the rising edge of the input pulse to the 50% level of the rising edge of the V_O signal.
10. PWD is defined as | t_{PHL} – t_{PLH} | for any given device.
11. The difference between t_{PHL} and t_{PLH} between any two FOD3180 parts under same test conditions.
12. Pin 1 and 4 need to be connected to LED common.
13. Common mode transient immunity in the high state is the maximum tolerable dV_{CM}/dt of the common mode pulse V_{CM} to assure that the output will remain in the high state (i.e. V_O > 10.0 V).
14. Common mode transient immunity in a low state is the maximum tolerable dV_{CM}/dt of the common mode pulse, V_{CM}, to assure that the output will remain in a low state (i.e. V_O < 1.0 V).

ISOLATION CHARACTERISTICS

Symbol	Parameter	Test Conditions	Min	Typ*	Max	Unit
V_{ISO}	Withstand Isolation Voltage (Note 15) (Note 16)	T_A = 25°C, R.H. < 50%, t = 1 min., $I_{I-O} \leq 20$ μA	5000	−	−	Vrms
R_{I-O}	Resistance (Input to Output) (Note 16)	V_{I-O} = 500 V	−	10^{11}	−	Ω
C_{I-O}	Capacitance (Input to Output)	Freq. = 1 MHz	−	1	−	pF

*Typical values at T_A = 25°C

15. In accordance with UL 1577, each optocoupler is proof tested by applying an insulation test voltage > 6000 Vrms, 60 Hz for 1 second (leakage detection current limit I_{I-O} < 5 μA).
16. Device considered a two−terminal device: pins on input side shorted together and pins on output side shorted together.

TYPICAL PERFORMANCE CURVES

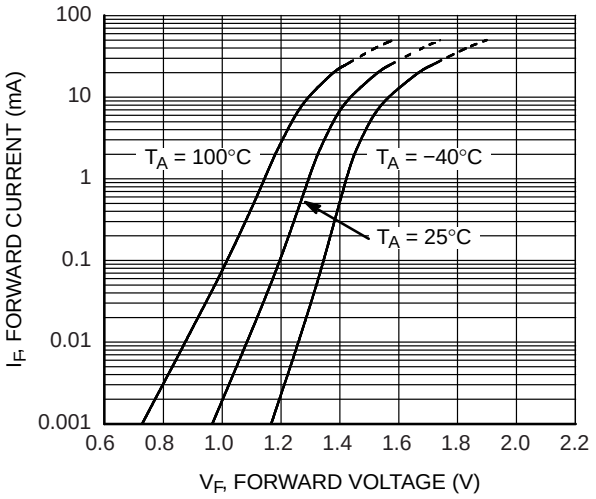


Figure 1. Input Forward Current vs. Forward Voltage

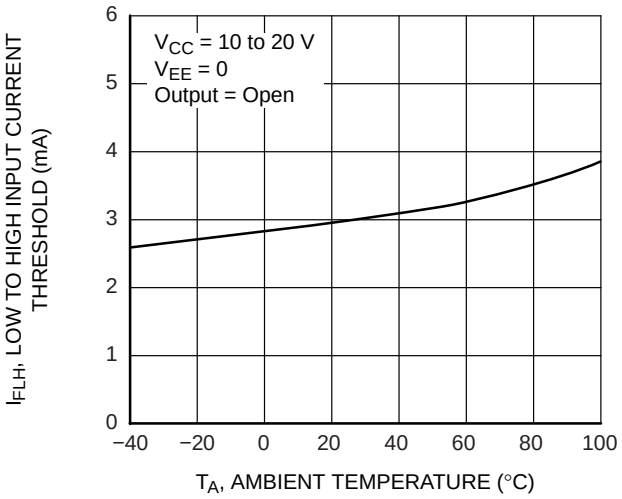


Figure 2. Low To High Input Current Threshold vs. Ambient Temperature

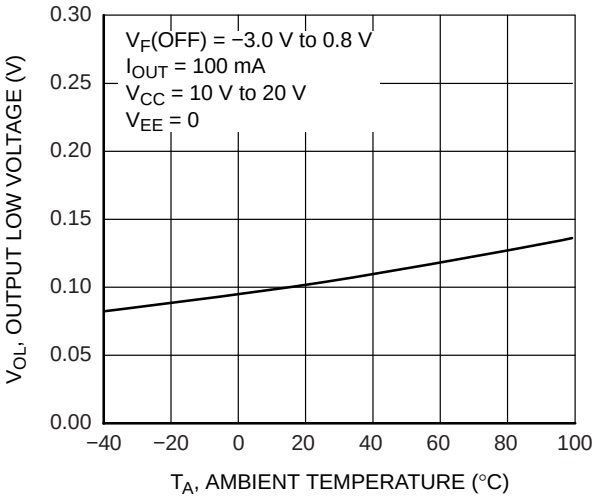


Figure 3. Output Low Voltage vs. Ambient Temperature

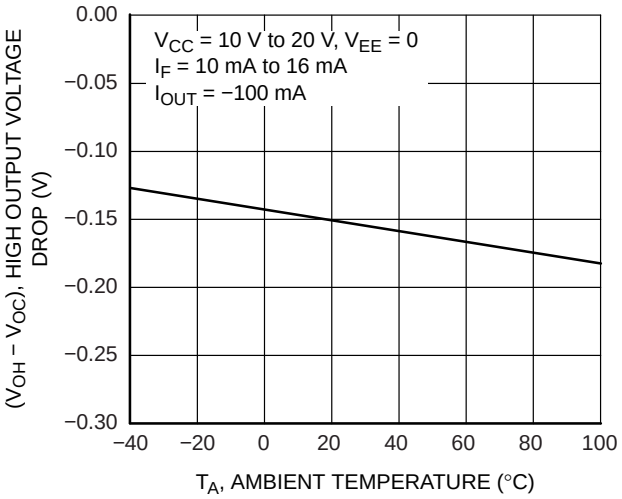


Figure 4. High Output Voltage Drop vs. Ambient Temperature

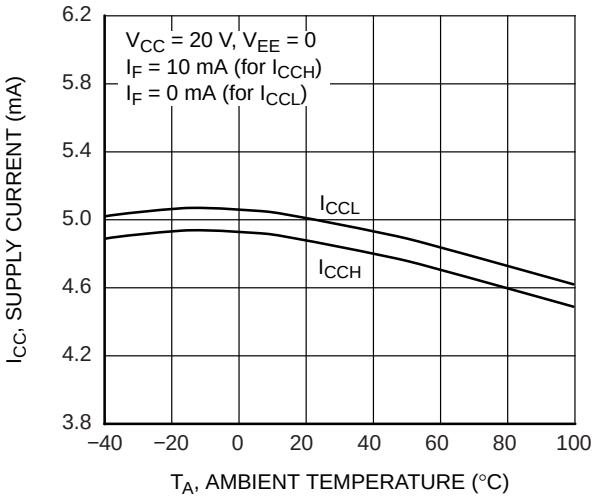


Figure 5. Supply Current vs. Ambient Temperature

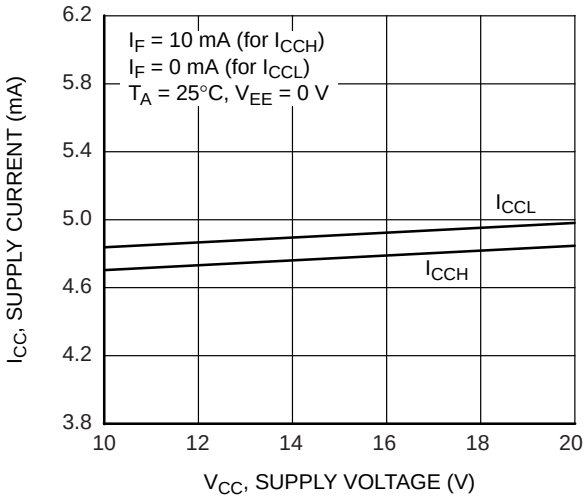


Figure 6. Supply Current vs. Supply Voltage

TYPICAL PERFORMANCE CURVES (continued)

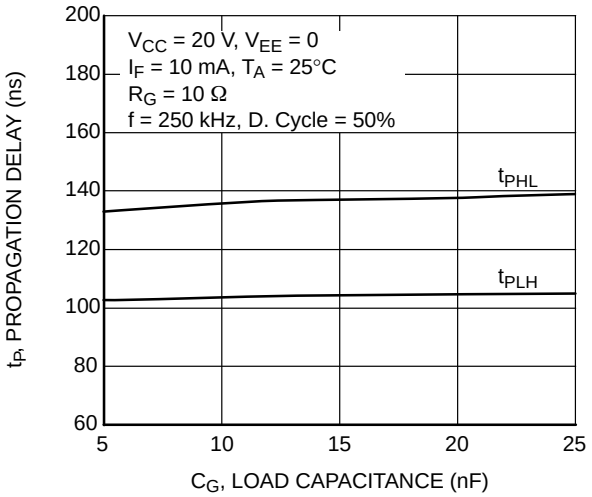


Figure 7. Propagation Delay vs. Load Capacitance

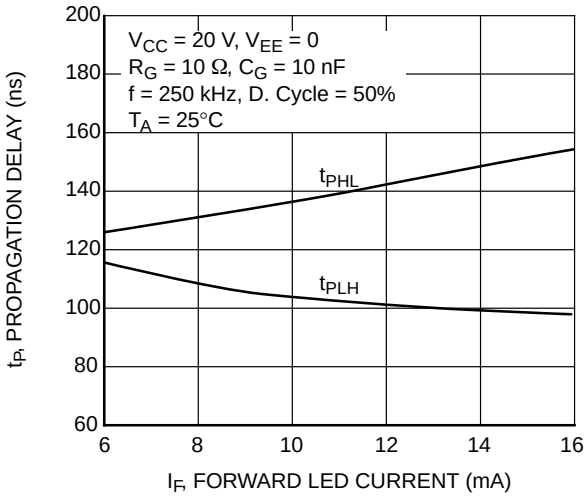


Figure 8. Propagation Delay vs. Forward LED Current

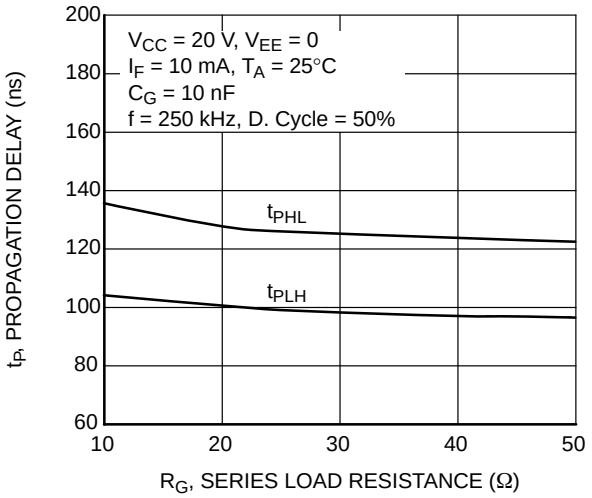


Figure 9. Propagation Delay vs. Series Load Resistance

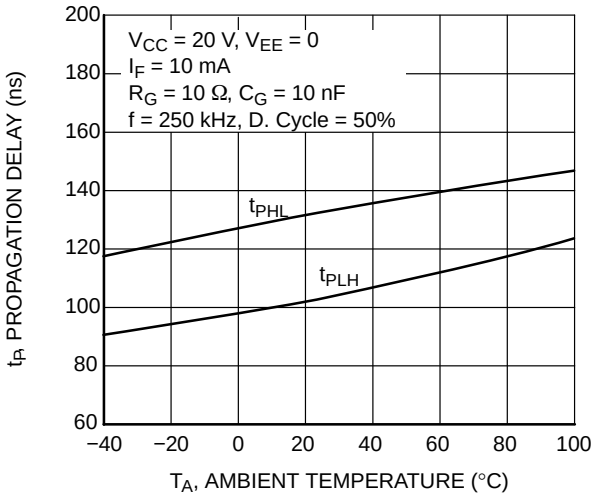


Figure 10. Propagation Delay vs. Ambient Temperature

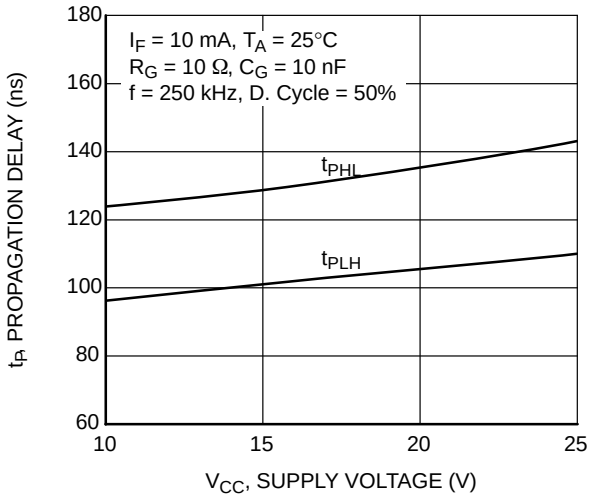
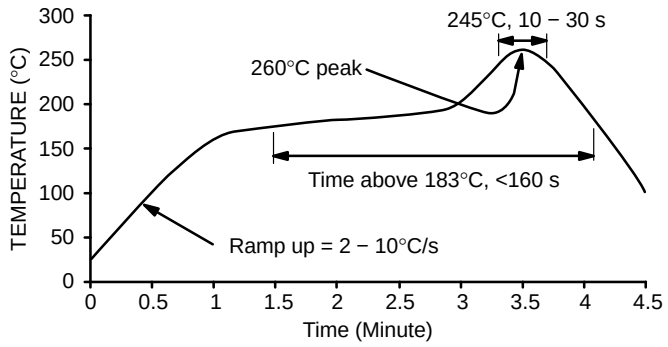


Figure 11. Propagation Delay vs. Supply Current

REFLOW PROFILE



- Peak reflow temperature: 260°C (package surface temperature)
- Time of temperature higher than 183°C for 160 seconds or less
- One time soldering reflow is recommended

Figure 12. Reflow Profile

OUTPUT POWER DERATING

The maximum package power dissipation is 295 mW. The package is limited to this level to ensure that under normal operating conditions and over extended temperature range that the semiconductor junction temperatures do not exceed 125°C. The package power is composed of three elements; the LED, static operating power of the output IC, and the power dissipated in the output power MOSFET transistors. The power rating of the output IC is 250 mW. This power is divided between the static power of the integrated circuit, which is the product of I_{DD} times the power supply voltage (V_{DD} − V_{EE}). The maximum IC static output power is 150 mW, (V_{DD} − V_{EE}) = 25 V, I_{DD} = 6 mA. This maximum condition is valid over the operational temperature range of −40°C to +100°C. Under these maximum operating conditions, the output of the power MOSFET is allowed to dissipate 100 mW of power.

The absolute maximum output power dissipation versus ambient temperature is shown in Figure 13. The output driver is capable of supplying 100 mW of output power over the temperature range from −40°C to 87°C. The output derates to 90 mW at the absolute maximum operating temperature of 100°C.

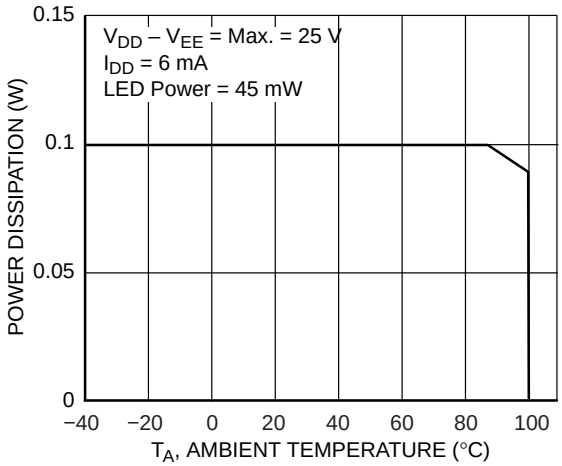


Figure 13. Absolute Maximum Power Dissipation vs. Ambient Temperature

The output power is the product of the average output current squared times the output transistor's $R_{DS(ON)}$:

$$P_{O(AVG)} = I_{O(AVG)}^2 \cdot R_{DS(ON)} \quad \text{(eq. 1)}$$

The $I_{O(AVG)}$ is the product of the duty factor times the peak current flowing in the output. The duty factor is the ratio of the 'on' time of the output load current divided by the period of the operating frequency. An $R_{DS(ON)}$ of 2.0 Ω results in an average output load current of 200 mA. The load duty factor is a ratio of the average output time of the power MOSFET load circuit and period of the driving frequency.

The maximum permissible, operating frequency is determined by the load supplied to the output at its resulting output pulse width. Figure 14 shows an example of a 0.03 μF gate to source capacitance with a series resistance of 8.50 Ω. This reactive load results in a composite average pulse width of 1.5 μs. Under this load condition it is not necessary to derate the absolute maximum output current until the frequency of operation exceeds 63 kHz.

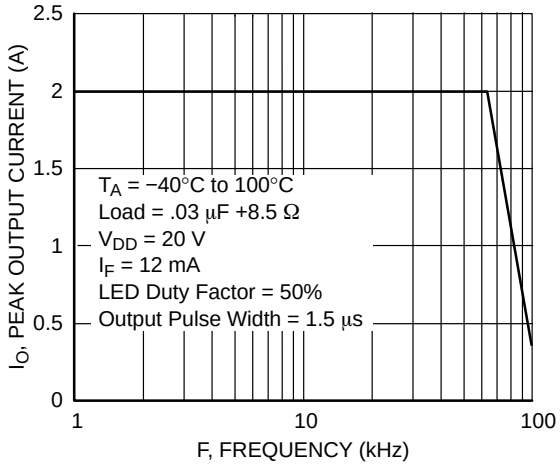


Figure 14. Output Current Derating vs. Frequency

I_{OH} AND I_{OL} TEST CONDITIONS

This device is tested and specified when driving a complex reactive load. The load consists of a capacitor in the series with a current limiting resistor. The capacitor represents the gate to source capacitance of a power MOSFET transistor. The test load is a 0.03 μF capacitor in series with an 8.5 Ω resistor. The LED test frequency is 10.0 kHz with a 50% duty cycle. The combined I_{OH} and I_{OL} output load current duty factor is 0.6% at the test frequency.

Figure 15 illustrates the relationship of the LED input drive current and the device's output voltage and sourcing and sinking currents. The 0.03 μF capacitor load rep

resents the gate to source capacitance of a very large power MOSFET transistor. A single supply voltage of 20 V is used in the evaluation.

Figure 16 shows the test schematic to evaluate the out− put voltage and sourcing and sinking capability of the device. The I_{OH} and I_{OL} are measured at the peak of their respective current pulses.

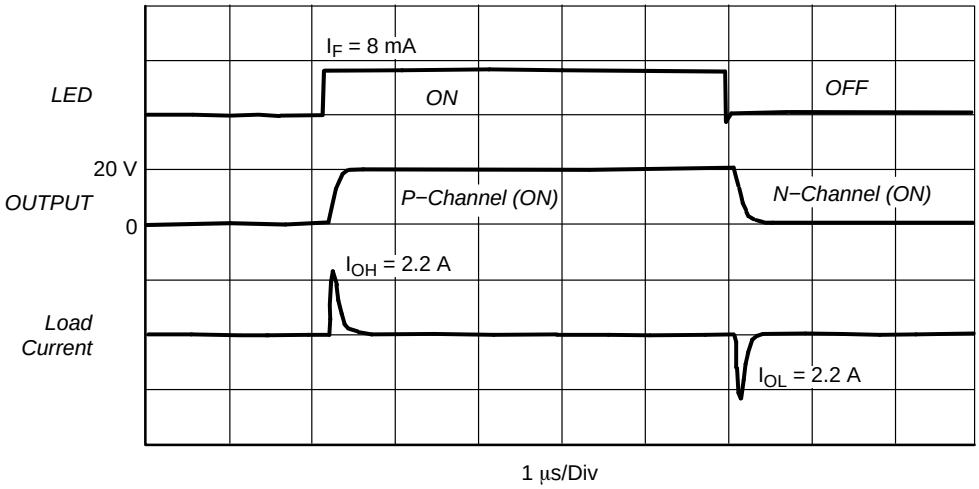


Figure 15. FOD 3180 Output Current and Output Voltage vs. LED Drive

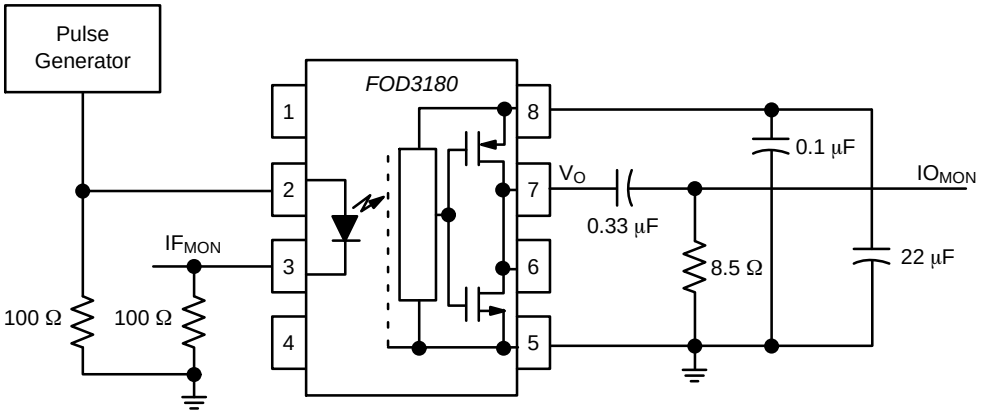


Figure 16. Test Schematic

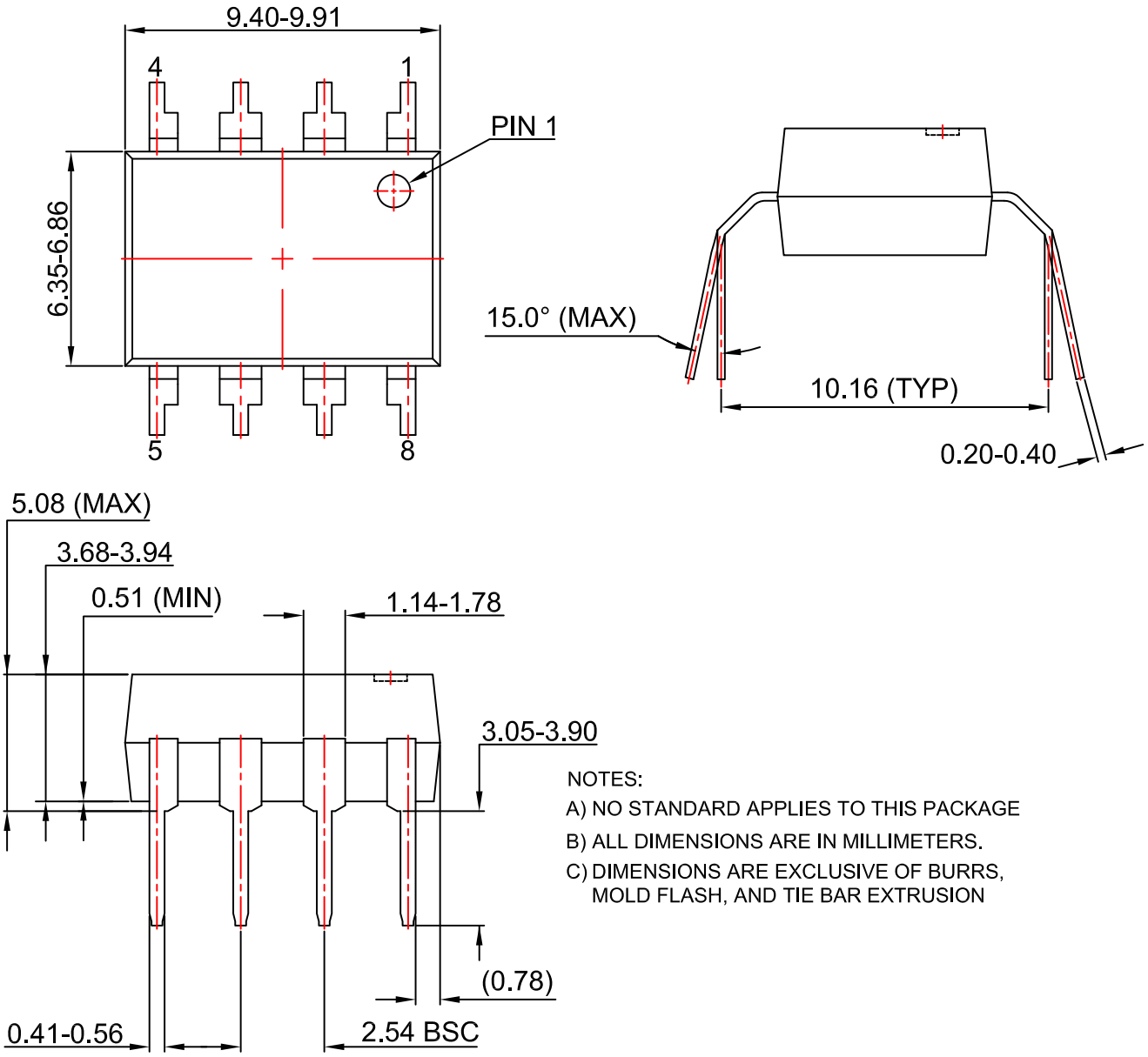
ORDERING INFORMATION

Option	Order Entry Identifier (Example)	Description†
No option	FOD3180	Standard Through Hole Device
S	FOD3180S	Surface Mount, Lead Bend
SD	FOD3180SD	Surface Mount, Tape and Reel
T	FOD3180T	0.4” Lead Spacing
V	FOD3180V	VDE 0884
TV	FOD3180TV	VDE 0884, 0.4” Lead Spacing
SV	FOD3180SV	VDE 0884, Surface Mount
SDV	FOD3180SDV	VDE 0884, Surface Mount, Tape and Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PDIP8 6.6x3.81, 2.54P
CASE 646BW
ISSUE O

DATE 31 JUL 2016



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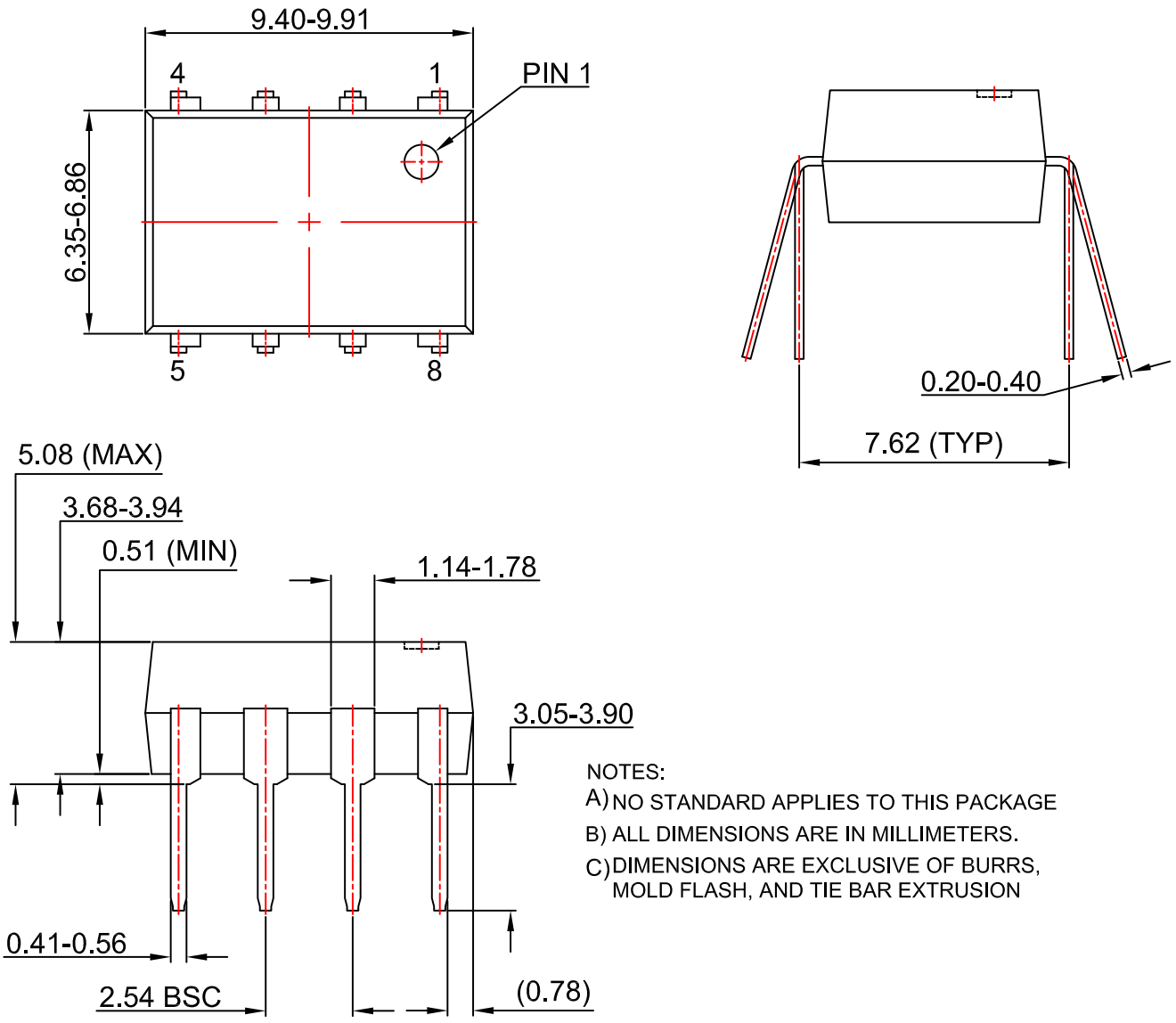
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

PDIP8 9.655x6.6, 2.54P
CASE 646CQ
ISSUE O

DATE 18 SEP 2017



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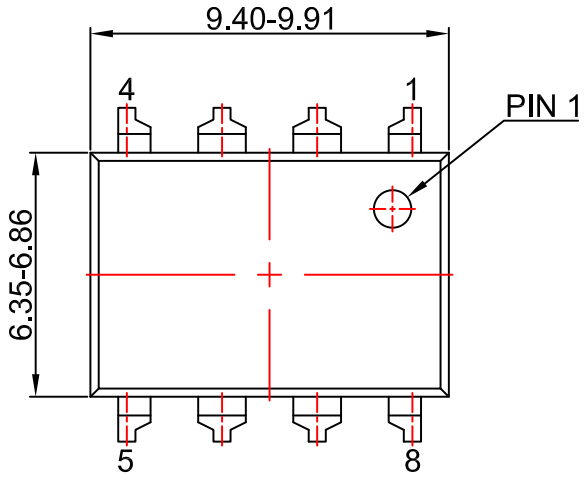
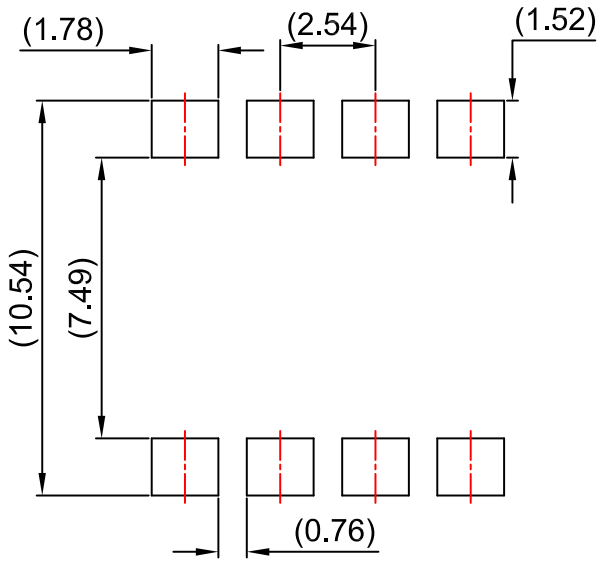
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

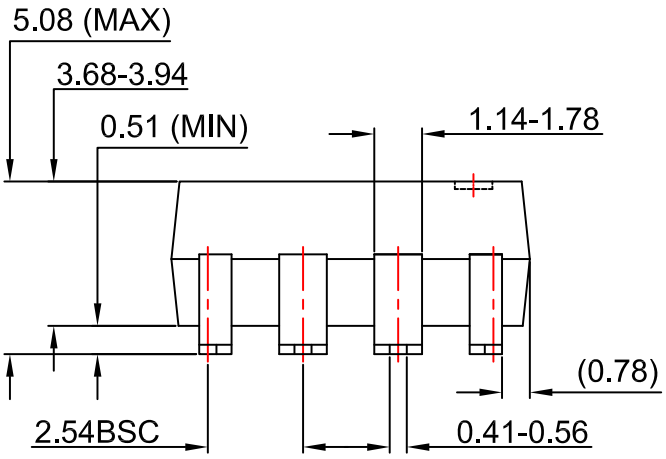
PDIP8 GW
CASE 709AC
ISSUE O

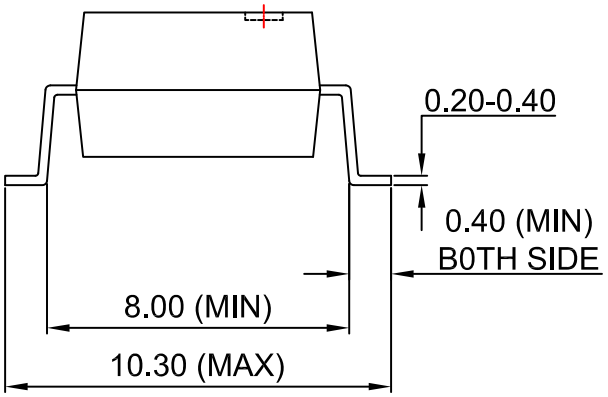
DATE 31 JUL 2016





LAND PATTERN RECOMMENDATION





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MECHANICAL CASE OUTLINE
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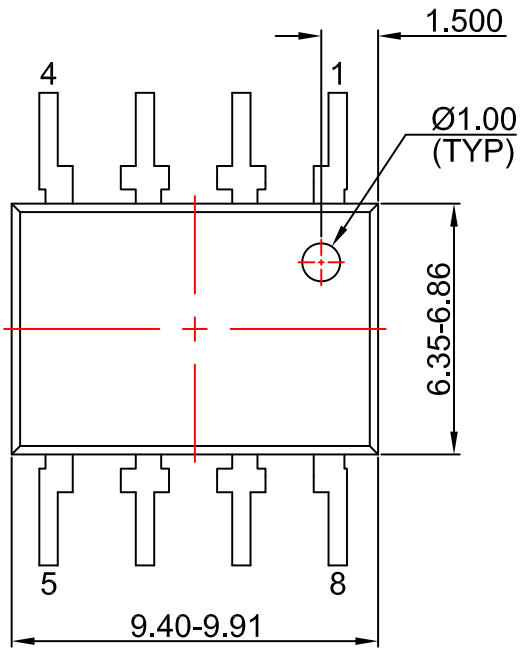

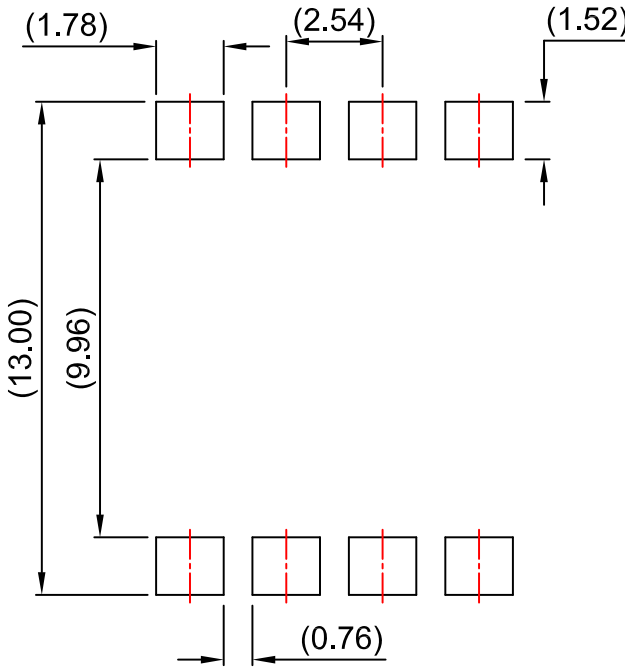

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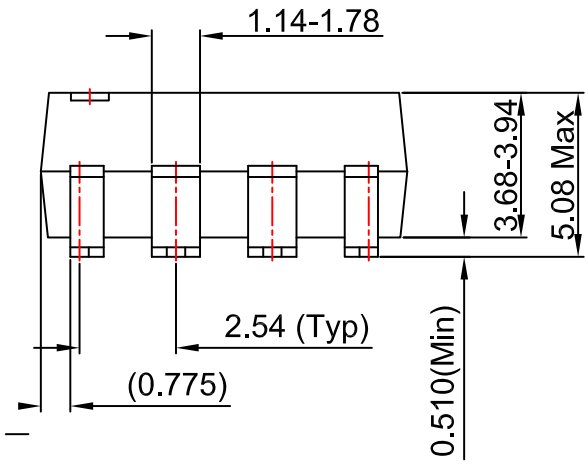

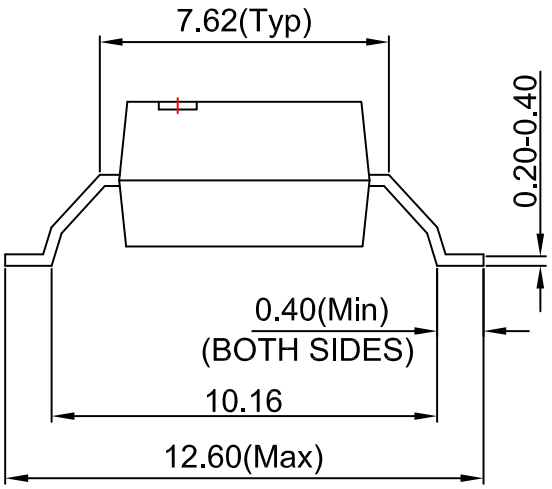

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