

MOSFET - Power, N-Channel, SOT-223

3.0 A, 60 V

NTF3055-100,
NVF3055-100

Designed for low voltage, high speed switching applications in power supplies, converters and power motor controls and bridge circuits.

Features

- NVF Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant

Applications

- Power Supplies
- Converters
- Power Motor Controls
- Bridge Circuits

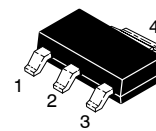
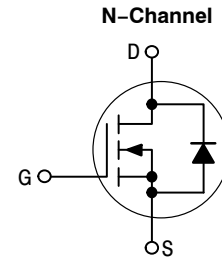
MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-to-Source Voltage	V _{DSS}	60	Vdc
Drain-to-Gate Voltage (R _{GS} = 10 MΩ)	V _{DGR}	60	Vdc
Gate-to-Source Voltage	V _{GS}	± 20 ± 30	Vdc Vpk
Drain Current	I _D	3.0	Adc
– Continuous @ T _A = 25°C	I _D	1.4	
– Continuous @ T _A = 100°C	I _{DM}	9.0	Apk
– Single Pulse (t _p ≤ 10 μs)			
Total Power Dissipation @ T _A = 25°C (Note 1)	P _D	2.1	W
Total Power Dissipation @ T _A = 25°C (Note 2)		1.3	W
Derate above 25°C		0.014	W/°C
Operating and Storage Temperature Range	T _J , T _{stg}	–55 to 175	°C
Single Pulse Drain-to-Source Avalanche Energy – Starting T _J = 25°C (V _{DD} = 25 Vdc, V _{GS} = 10 Vdc, I _{L(pk)} = 7.0 Apk, L = 3.0 mH, V _{DS} = 60 Vdc)	E _{AS}	74	mJ
Thermal Resistance	R _{θJA}	72.3	°C/W
– Junction-to-Ambient (Note 1)	R _{θJA}	114	
– Junction-to-Ambient (Note 2)			
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 10 seconds	T _L	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

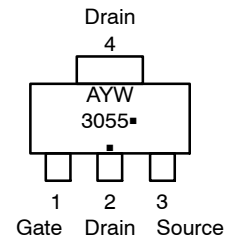
1. When surface mounted to an FR4 board using 1" pad size, 1 oz. (Cu. Area 1.127 sq in).
2. When surface mounted to an FR4 board using minimum recommended pad size, 2–2.4 oz. (Cu. Area 0.272 sq in).

3.0 A, 60 V
R_{DS(on)} = 110 mΩ



SOT-223
CASE 318E
STYLE 3

MARKING DIAGRAM & PIN ASSIGNMENT



A = Assembly Location
Y = Year
W = Work Week
3055 = Specific Device Code
■ = Pb-Free Package
(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping†
NTF3055-100T1G	SOT-223 (Pb-Free)	1000 / Tape & Reel
NTF3055-100T3G	SOT-223 (Pb-Free)	4000 / Tape & Reel
NVF3055-100T1G	SOT-223 (Pb-Free)	1000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

NTF3055-100, NVF3055-100

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage (Note 3) (V _{GS} = 0 Vdc, I _D = 250 μAdc) Temperature Coefficient (Positive)	V _{(BR)DSS}	60 –	68 66	– –	Vdc mV/°C
Zero Gate Voltage Drain Current (V _{DS} = 60 Vdc, V _{GS} = 0 Vdc) (V _{DS} = 60 Vdc, V _{GS} = 0 Vdc, T _J = 150°C)	I _{DSS}	– –	– –	1.0 10	μAdc
Gate-Body Leakage Current (V _{GS} = ± 20 Vdc, V _{DS} = 0 Vdc)	I _{GSS}	–	–	± 100	nAdc

ON CHARACTERISTICS (Note 3)

Gate Threshold Voltage (Note 3) (V _{DS} = V _{GS} , I _D = 250 μAdc) Threshold Temperature Coefficient (Negative)	V _{GS(th)}	2.0 –	3.0 6.6	4.0 –	Vdc mV/°C
Static Drain-to-Source On-Resistance (Note 3) (V _{GS} = 10 Vdc, I _D = 1.5 Adc)	R _{DS(on)}	–	88	110	mΩ
Static Drain-to-Source On-Resistance (Note 3) (V _{GS} = 10 Vdc, I _D = 3.0 Adc) (V _{GS} = 10 Vdc, I _D = 1.5 Adc, T _J = 150°C)	V _{DS(on)}	–	0.27 0.24	0.40 –	Vdc
Forward Transconductance (Note 3) (V _{DS} = 8.0 Vdc, I _D = 1.7 Adc)	g _{fs}	–	3.2	–	Mhos

DYNAMIC CHARACTERISTICS

Input Capacitance	(V _{DS} = 25 Vdc, V _{GS} = 0 V, f = 1.0 MHz)	C _{iss}	–	324	455	pF
Output Capacitance		C _{oss}	–	35	50	
Transfer Capacitance		C _{rss}	–	110	155	

SWITCHING CHARACTERISTICS (Note 4)

Turn-On Delay Time	(V _{DD} = 30 Vdc, I _D = 3.0 Adc, V _{GS} = 10 Vdc, R _G = 9.1 Ω) (Note 3)	t _{d(on)}	–	9.4	20	ns
Rise Time		t _r	–	14	30	
Turn-Off Delay Time		t _{d(off)}	–	21	45	
Fall Time		t _f	–	13	30	
Gate Charge	(V _{DS} = 48 Vdc, I _D = 3.0 Adc, V _{GS} = 10 Vdc) (Note 3)	Q _T	–	10.6	22	nC
		Q ₁	–	1.9	–	
		Q ₂	–	4.2	–	

SOURCE-DRAIN DIODE CHARACTERISTICS

Forward On-Voltage	(I _S = 3.0 Adc, V _{GS} = 0 Vdc) (I _S = 3.0 Adc, V _{GS} = 0 Vdc, T _J = 150°C) (Note 3)	V _{SD}	– –	0.89 0.74	1.0 –	Vdc
Reverse Recovery Time	(I _S = 3.0 Adc, V _{GS} = 0 Vdc, dI _S /dt = 100 A/μs) (Note 3)	t _{rr}	–	30	–	ns
		t _a	–	22	–	
		t _b	–	8.6	–	
Reverse Recovery Stored Charge		Q _{RR}	–	0.04	–	μC

3. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

4. Switching characteristics are independent of operating junction temperatures.

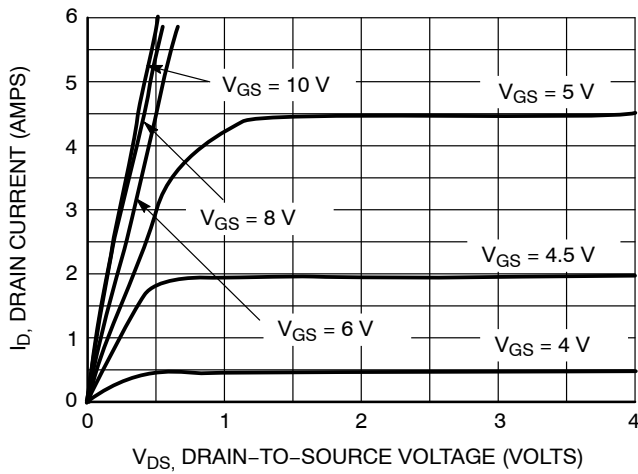


Figure 1. On-Region Characteristics

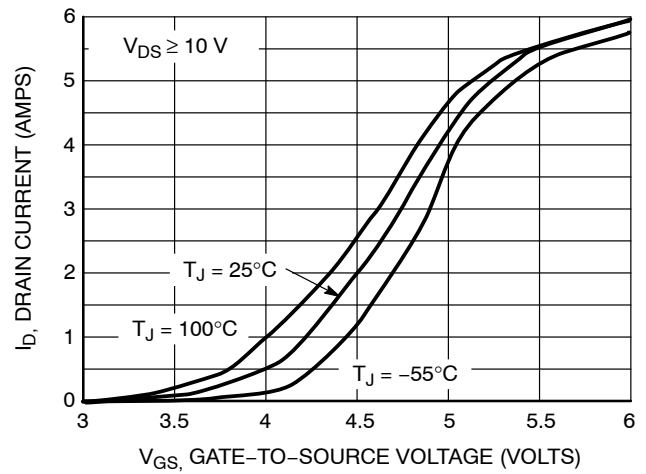


Figure 2. Transfer Characteristics

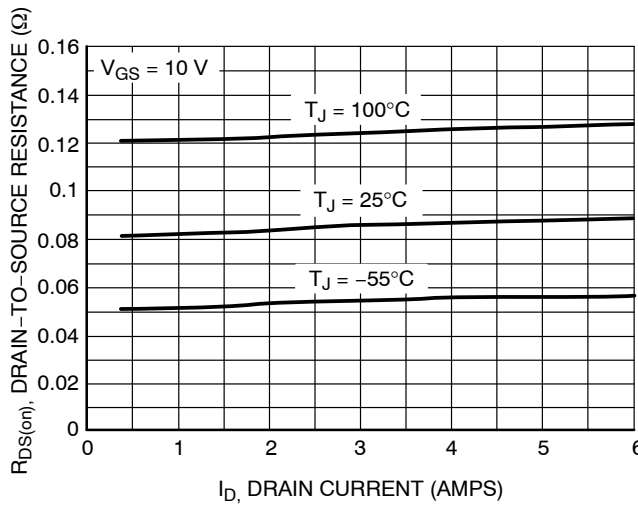


Figure 3. On-Resistance versus Gate-to-Source Voltage

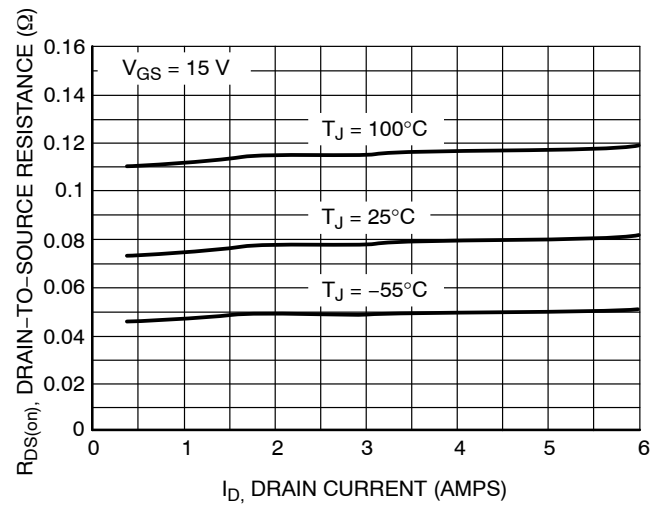


Figure 4. On-Resistance versus Drain Current and Gate Voltage

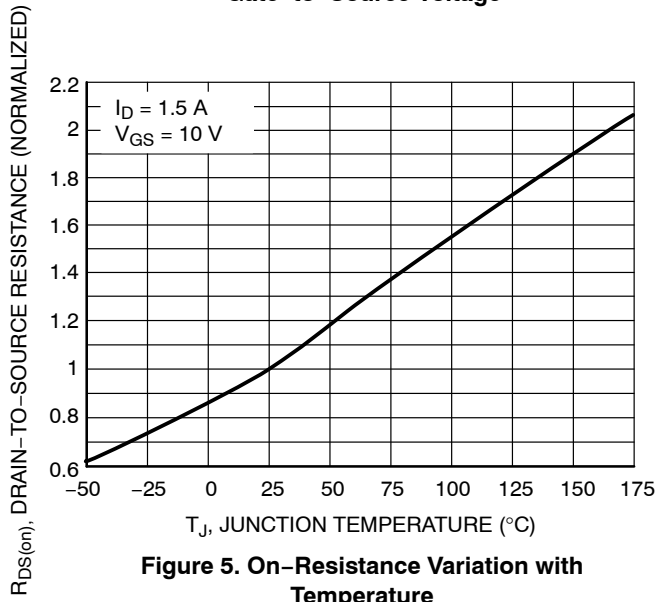


Figure 5. On-Resistance Variation with Temperature

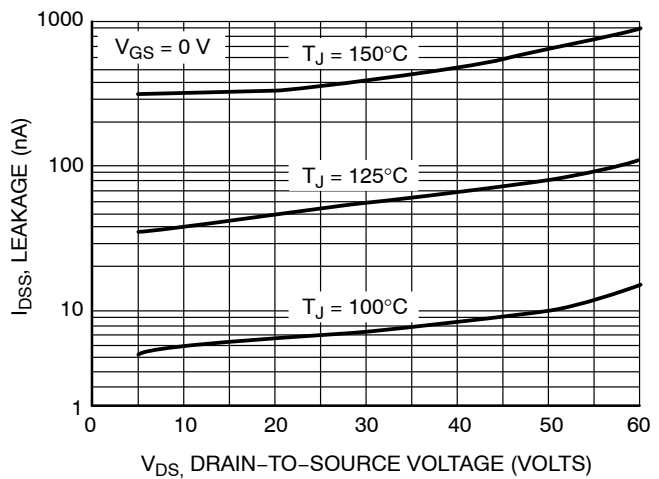


Figure 6. Drain-to-Source Leakage Current versus Voltage

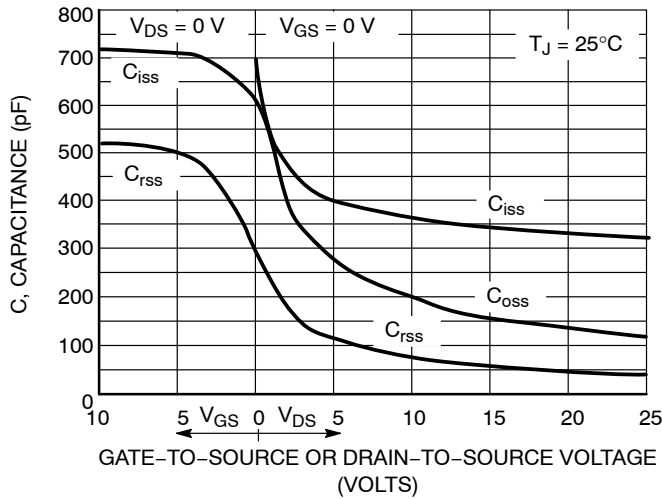


Figure 7. Capacitance Variation

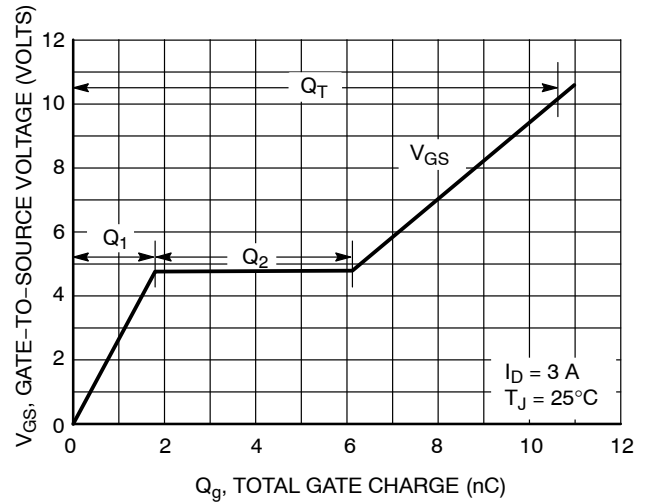


Figure 8. Gate-to-Source and Drain-to-Source Voltage versus Total Charge

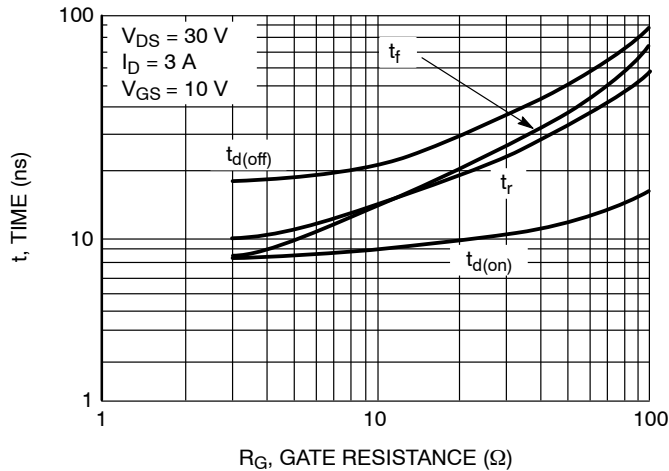


Figure 9. Resistive Switching Time Variation versus Gate Resistance

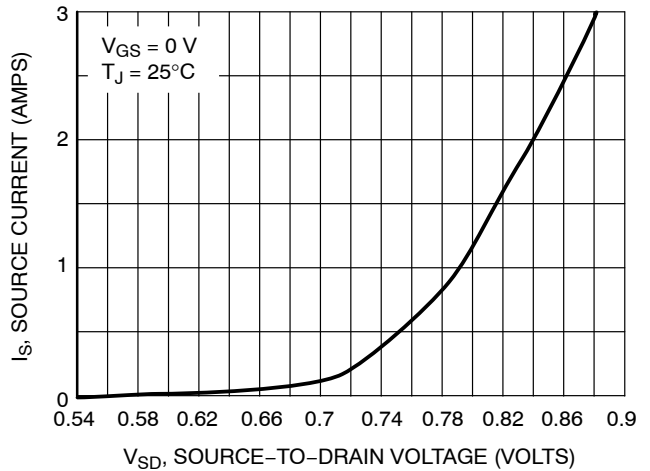


Figure 10. Diode Forward Voltage versus Current

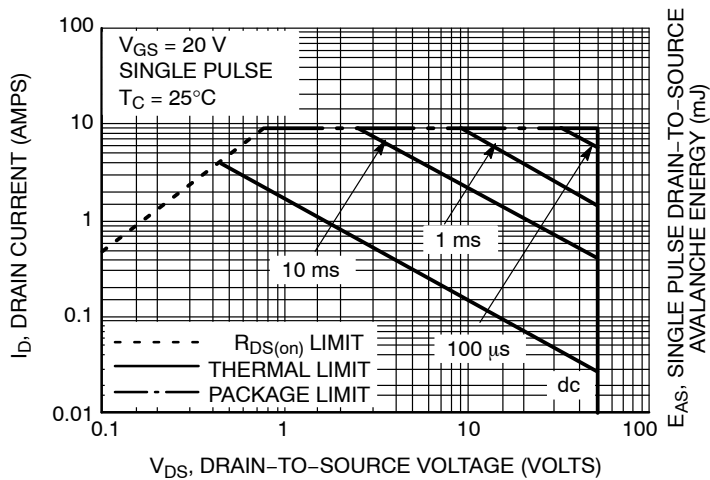


Figure 11. Maximum Rated Forward Biased Safe Operating Area

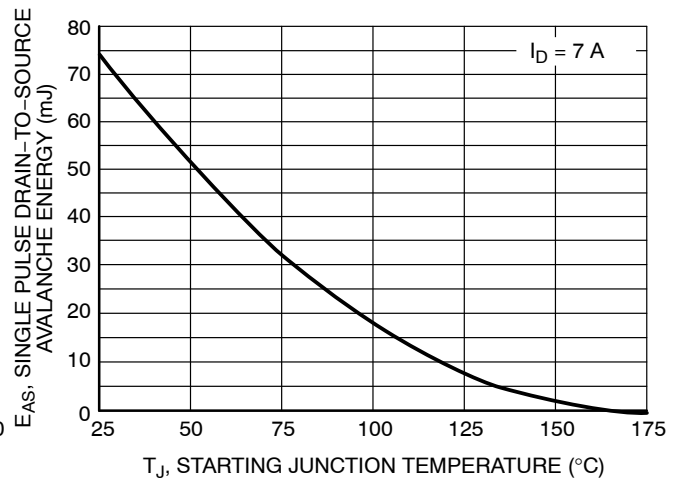


Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature

NTF3055-100, NVF3055-100

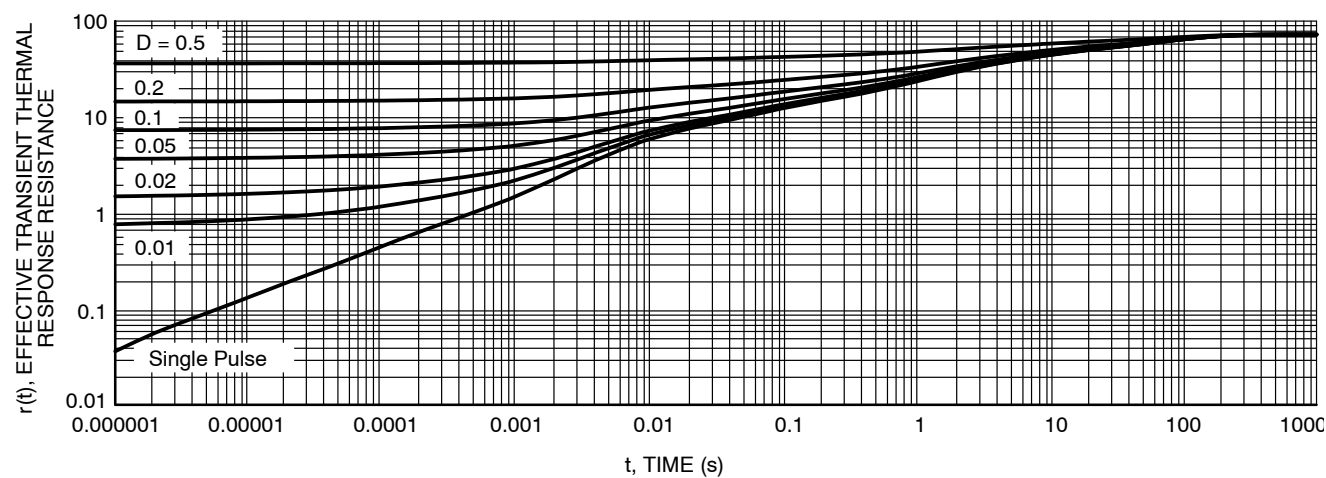


Figure 13. Thermal Response

MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

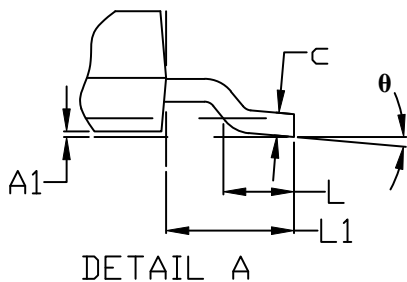
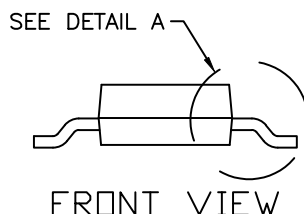
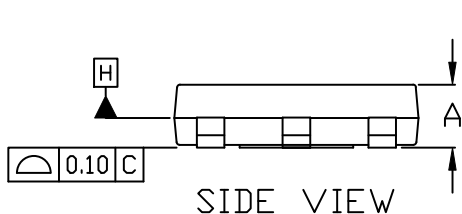
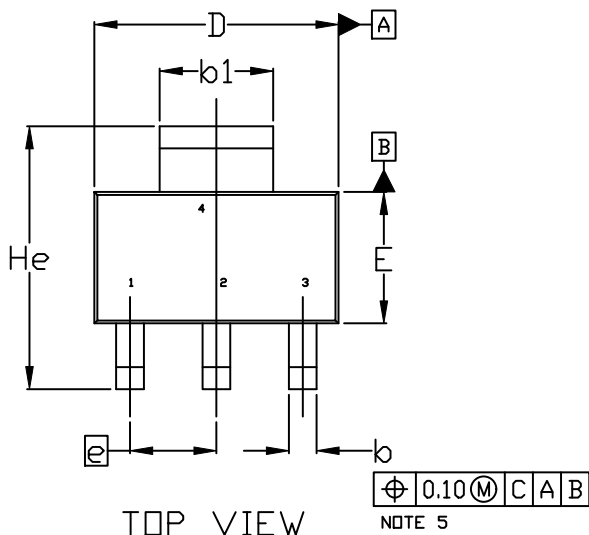
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SCALE 1:1

SOT-223 (TO-261)
CASE 318E-04
ISSUE R

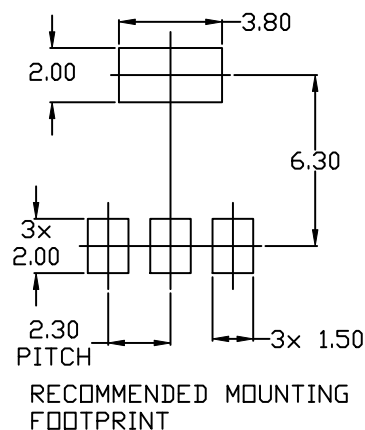
DATE 02 OCT 2018



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS D & E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.200MM PER SIDE.
4. DATUMS A AND B ARE DETERMINED AT DATUM H.
5. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.
6. POSITIONAL TOLERANCE APPLIES TO DIMENSIONS b AND b1.

MILLIMETERS			
DIM	MIN.	NOM.	MAX.
A	1.50	1.63	1.75
A1	0.02	0.06	0.10
b	0.60	0.75	0.89
b1	2.90	3.06	3.20
c	0.24	0.29	0.35
D	6.30	6.50	6.70
E	3.30	3.50	3.70
e	2.30 BSC		
L	0.20	---	---
L1	1.50	1.75	2.00
He	6.70	7.00	7.30
θ	0°	---	10°



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SOT-223 (TO-261)
CASE 318E-04
ISSUE R

DATE 02 OCT 2018

STYLE 1: PIN 1. BASE 2. COLLECTOR 3. EMITTER 4. COLLECTOR	STYLE 2: PIN 1. ANODE 2. CATHODE 3. NC 4. CATHODE	STYLE 3: PIN 1. GATE 2. DRAIN 3. SOURCE 4. DRAIN	STYLE 4: PIN 1. SOURCE 2. DRAIN 3. GATE 4. DRAIN	STYLE 5: PIN 1. DRAIN 2. GATE 3. SOURCE 4. GATE
STYLE 6: PIN 1. RETURN 2. INPUT 3. OUTPUT 4. INPUT	STYLE 7: PIN 1. ANODE 1 2. CATHODE 3. ANODE 2 4. CATHODE	STYLE 8: CANCELLED	STYLE 9: PIN 1. INPUT 2. GROUND 3. LOGIC 4. GROUND	STYLE 10: PIN 1. CATHODE 2. ANODE 3. GATE 4. ANODE
STYLE 11: PIN 1. MT 1 2. MT 2 3. GATE 4. MT 2	STYLE 12: PIN 1. INPUT 2. OUTPUT 3. NC 4. OUTPUT	STYLE 13: PIN 1. GATE 2. COLLECTOR 3. EMITTER 4. COLLECTOR		


**GENERIC
MARKING DIAGRAM***



A = Assembly Location
 Y = Year
 W = Work Week
 XXXXX = Specific Device Code
 ■ = Pb-Free Package

(Note: Microdot may be in either location)
 *This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present. Some products may not follow the Generic Marking.

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