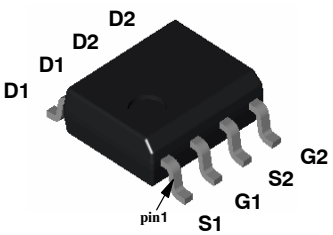
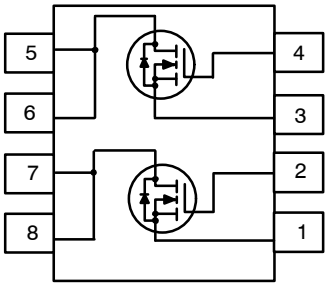
Dual N-Channel Enhancement Mode Field Effect Transistor

NDS9945



SOIC−8
CASE 751



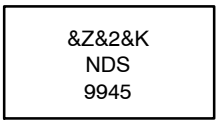
General Description

SO−8 N−Channel Enhancement Mode Power Field Effect Transistors are Produced using **onsemi**'s proprietary, high cell density, DMOS technology. This very high density process is especially tailored to provide superior switching performance and minimize on−state resistance. These devices are particularly suited for low voltage applications such as disk drive motor control, battery powered circuits where fast switching, low in−line power loss, and resistance to transients are needed.

Features

- 3.5 A, 60 V
  - $R_{DS(on)}$ = 0.100 Ω @ V_{GS} = 10 V
  - $R_{DS(on)}$ = 0.200 Ω @ V_{GS} = 4.5 V
- High Density Cell Design for Extremely Low $R_{DS(ON)}$
- High Power and Current Handling Capability in a Widely used surface mount package
- Dual MOSFET in surface mount package
- This is a Pb−Free and Halide Free Device

MARKING DIAGRAM



&Z = Assembly Plant Code
&2 = Numeric Date Code
&K = 2−Digit Lot Code
9945 = Specific Device Code

ABSOLUTE MAXIMUM RATINGS T_A = 25°C unless otherwise noted

Symbol	Parameter	Value	Unit
V_{DSS}	Drain−Source Voltage	60	V
V_{GSS}	Gate−Source Voltage	±20	V
I_D	Drain Current − Continuous (Note 1a) − Pulsed	 3.5 10	A
P_D	Power Dissipation for Dual Operation	2	W
	Power Dissipation for Single Operation (Note 1a)	1.6	
	(Note 1b)	1	
	(Note 1c)	0.9	
T_J, T_{stg}	Operating and Storage Junction Temperature Range	−55 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

ORDERING INFORMATION

Device	Package	Shipping†
NDS9945	SOIC−8 (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Unit
$R_{\theta JA}$	Thermal Resistance, Junction−to−Ambient (Note 1a)	78	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction−to−Case (Note 1)	40	°C/W

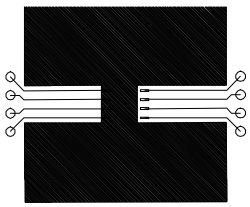
ELECTRICAL CHARACTERISTICS T_A = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Off Characteristics						
BV_{DSS}	Drain to Source Breakdown Voltage	V_{GS} = 0 V, I_D = −10 μA	60	–	–	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = −250 μA, Referenced to 25°C	–	60	–	mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 48 V, V_{GS} = 0 V	–	–	1	μA
I_{GSSF}	Gate − Body Leakage, Forward	V_{GS} = 20 V, V_{DS} = 0 V	–	–	100	nA
I_{GSSR}	Gate − Body Leakage, Reverse	V_{GS} = −20 V, V_{DS} = 0 V	–	–	−100	nA
On Characteristics (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 μA T_J = 125°C	1 0.7	1.7 –	3 2.2	V
$R_{DS(on)}$	Static Drain−Source On−Resistance	V_{GS} = 10 V, I_D = 3.5 A T_J = 125°C V_{GS} = 4.5 V, I_D = 2.5 A T_J = 125°C	– –	0.076 0.124 0.103 0.166	0.1 0.18 0.2 0.3	Ω
$I_{D(on)}$	On−State Drain Current	V_{GS} = 10 V, V_{DS} = 10 V	10	–	–	A
g_{FS}	Forward Transconductance	V_{DS} = 10 V, I_D = 3.5 A	–	5.3	–	S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 25 V, V_{GS} = 0 V, f = 1.0 MHz	–	345	–	pF
C_{oss}	Output Capacitance		–	110	–	pF
C_{rss}	Reverse Transfer Capacitance		–	25	–	pF
Switching Characteristics (Note 2)						
$t_{d(on)}$	Turn−On Delay Time	V_{DD} = 30 V, I_D = 1 A, V_{GS} = 10 V, R_{GEN} = 6 Ω	–	5	25	ns
t_r	Turn−On Rise Time		–	7.5	30	ns
$t_{d(off)}$	Turn−Off Delay Time		–	20	50	ns
t_f	Turn−Off Fall Time		–	7	40	ns
Q_g	Total Gate Change	V_{DS} = 30 V, I_D = 3.5 A, V_{GS} = 10 V	–	12.9	30	nC
Q_{gs}	Gate−Source Change		–	1.7	–	nC
Q_{gd}	Gate−Drain Change		–	3.2	–	nC
Drain−Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain−Source Diode Forward Current		–	–	1.3	A
V_{SD}	Drain−Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 1.3 A (Note 2)	–	0.8	1.2	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0 V, I_F = 1.3 A, d_{iF}/d_t = 100 A/μs	–	40	–	ns
I_{rr}	Reverse Recovery Current		–	1.5	–	A

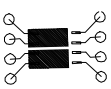
Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTES:

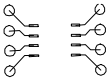
1. $R_{\theta JA}$ is the sum of the junction−to−case and case−to−ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a).78 °C/W on a 0.5 in^2 pad of 2oz copper.



b).125 °C/W on a 0.02 in^2 pad of 2oz copper.



c).135 °C/W on a 0.003 in^2 pad of 2oz copper.

Scale 1 1 on letter size paper

2. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%

TYPICAL CHARACTERISTICS

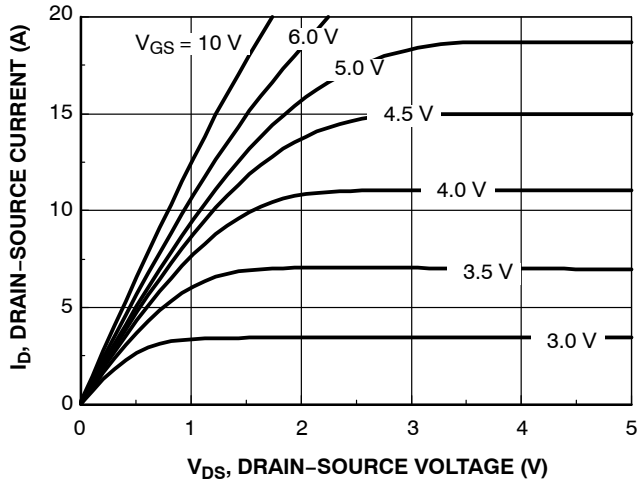


Figure 1. On–Region Characteristics

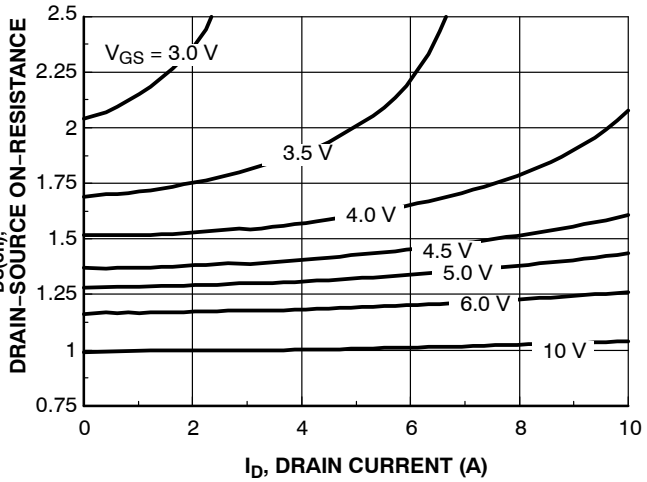


Figure 2. On–Resistance Variation With Drain Current and Gate Voltage

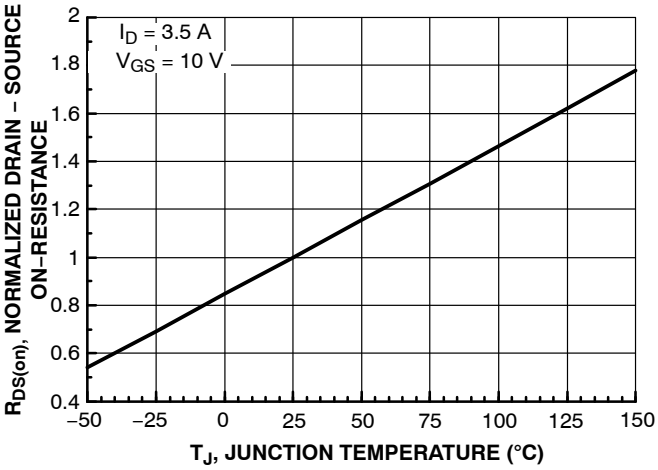


Figure 3. On–Resistance Variation with Temperature

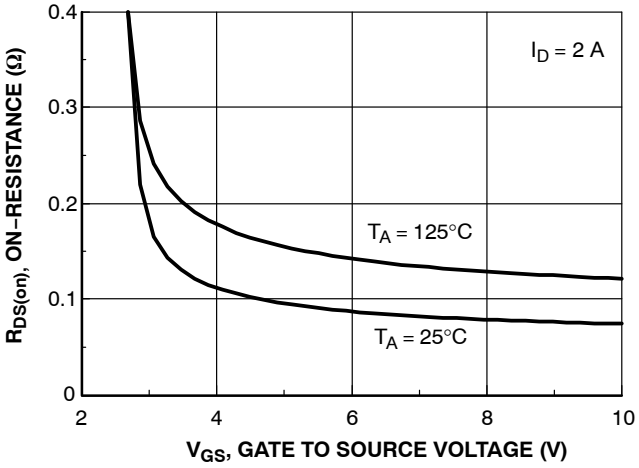


Figure 4. On–Resistance Variation with Gate–to–Source Voltage

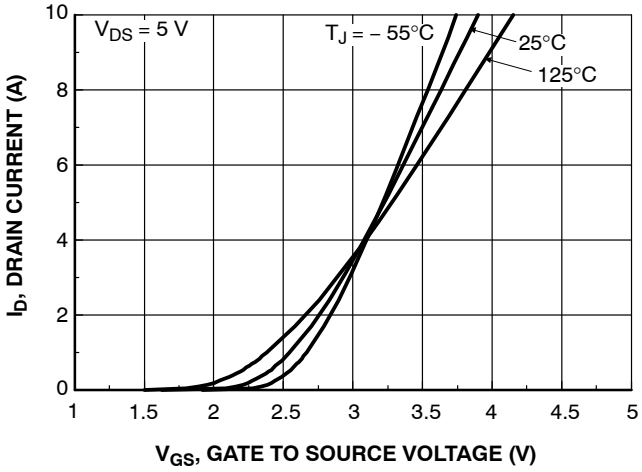


Figure 5. Transfer Characteristics

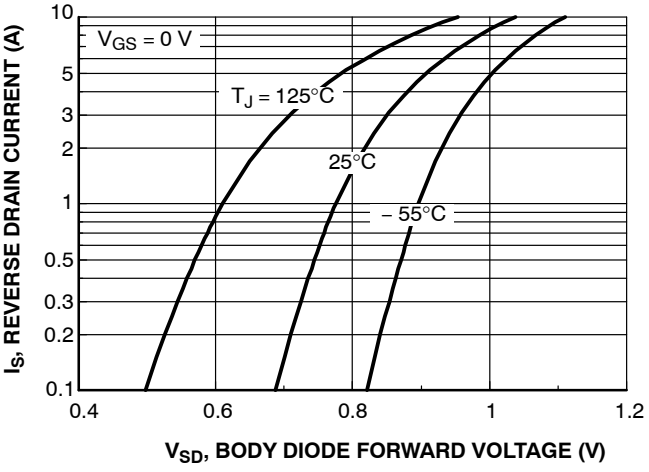


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature

TYPICAL CHARACTERISTICS (CONTINUED)

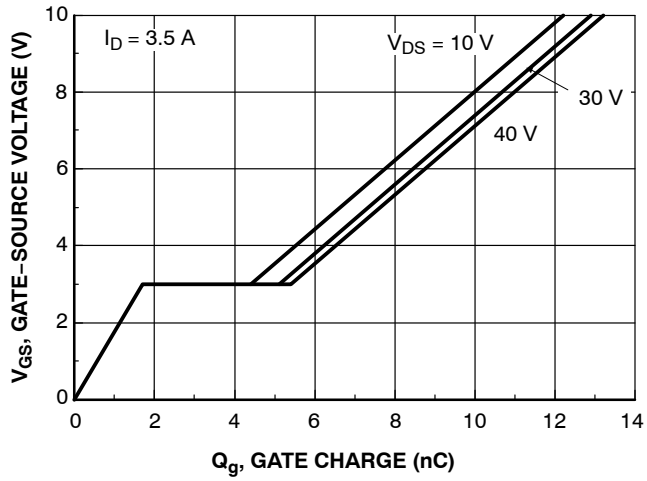


Figure 7. Gate Charge Characteristics

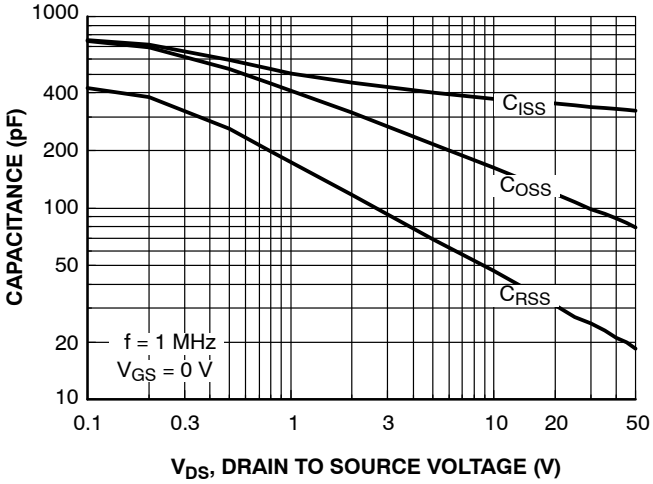


Figure 8. Capacitance Characteristics

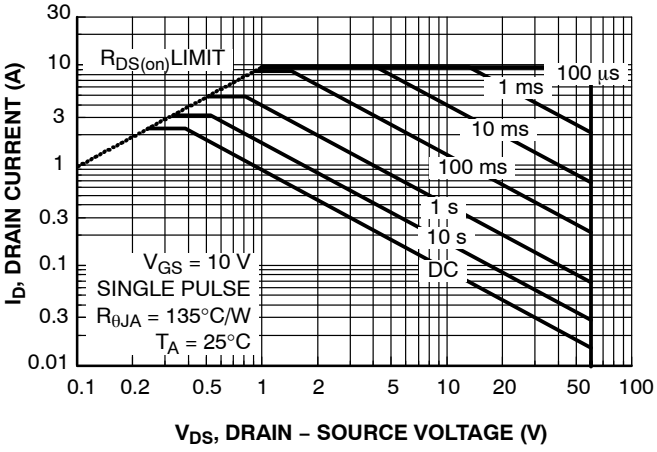


Figure 9. Maximum Safe Operating Area

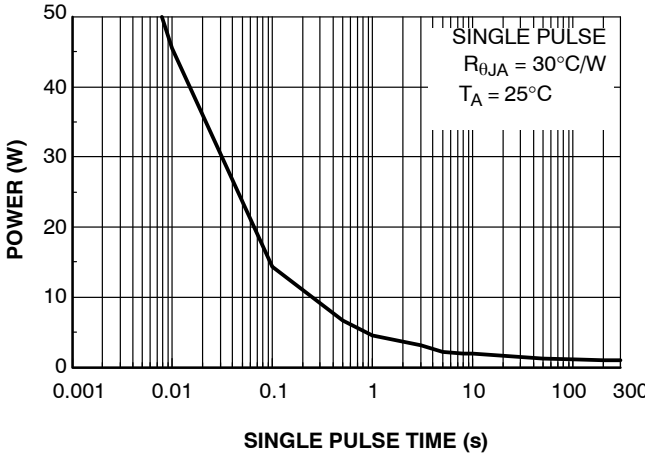


Figure 10. Single Pulse Maximum Power Dissipation

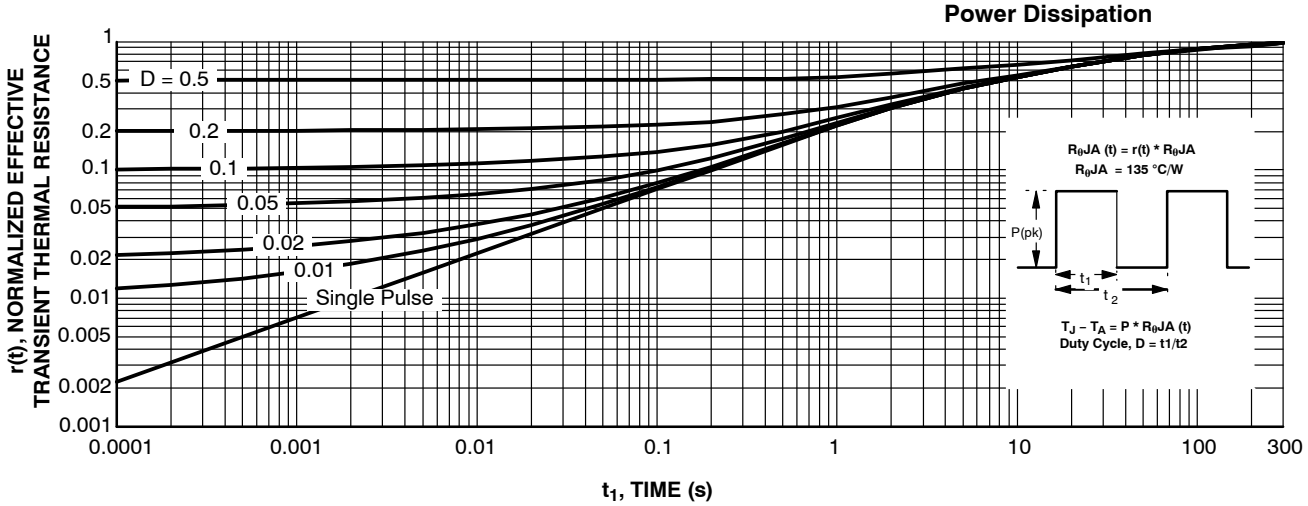


Figure 11. Transient Thermal Response Curve

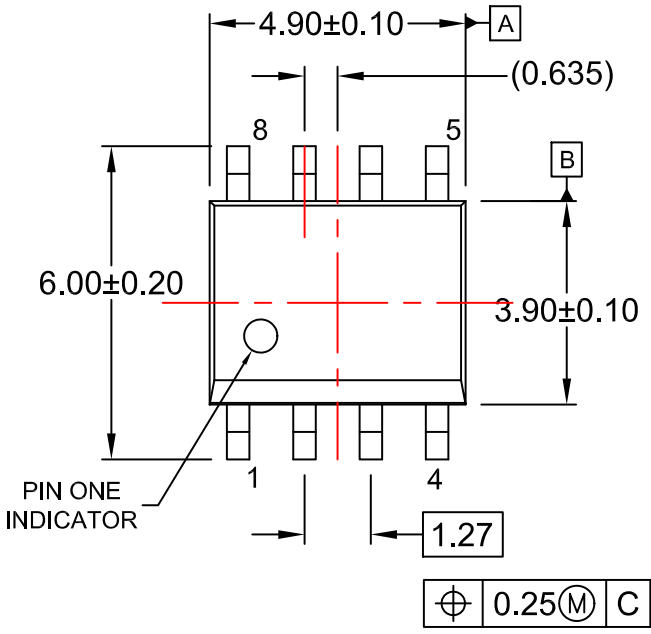
Thermal characterization performed using the conditions described in Note 1a.
Transient themal response will change depending on the circuit board design.

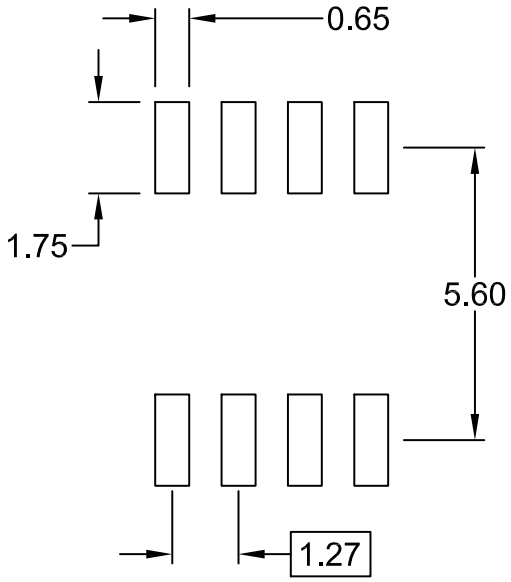
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

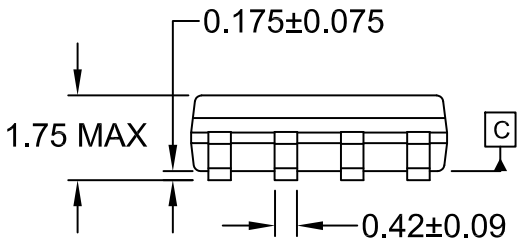
SOIC8
CASE 751EB
ISSUE A

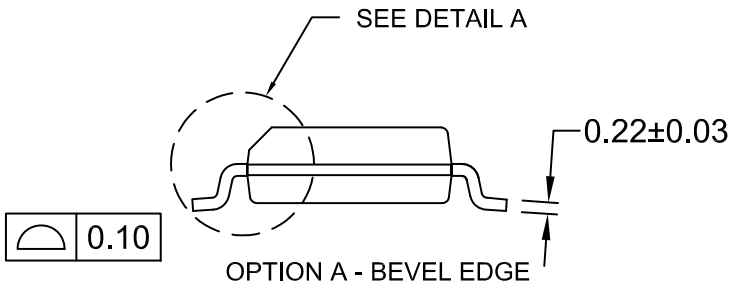
DATE 24 AUG 2017



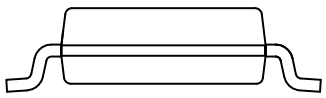


LAND PATTERN RECOMMENDATION

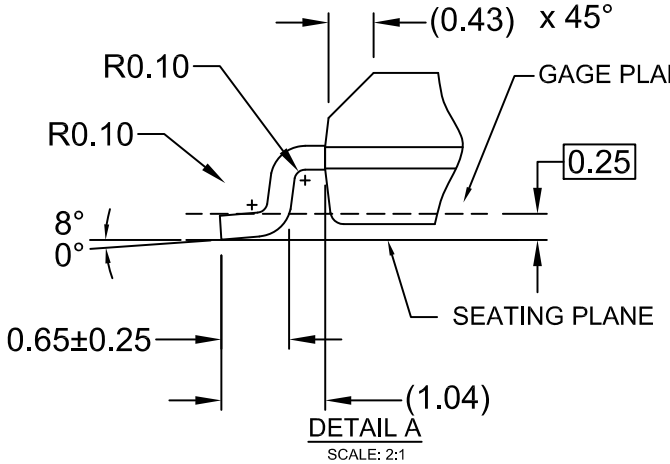




OPTION A - BEVEL EDGE



OPTION B - NO BEVEL EDGE



DETAIL A
SCALE: 2:1

NOTES:
A) THIS PACKAGE CONFORMS TO JEDEC MS-012, VARIATION AA.
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS.
D) LANDPATTERN STANDARD: SOIC127P600X175-8M

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