[MOSFET](#) – P-Channel, POWERTRENCH®

-30 V, -20 A, 10 mΩ
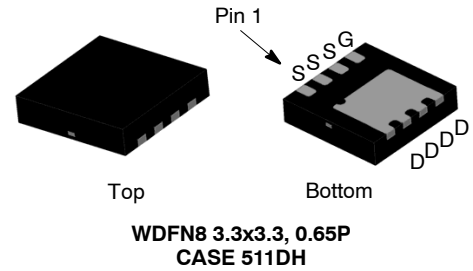
FDMC6679AZ

General Description

The FDMC6679AZ has been designed to minimize losses in load switch applications. Advancements in both silicon and package technologies have been combined to offer the lowest $r_{DS(on)}$ and ESD protection.

Features

- Max $r_{DS(on)}$ = 10 mΩ at V_{GS} = −10 V, I_D = −11.5 A
- Max $r_{DS(on)}$ = 18 mΩ at V_{GS} = −4.5 V, I_D = −8.5 A
- HBM ESD Protection Level of 8 kV Typical (Note 3)
- Extended V_{GSS} range (−25 V) for Battery Applications
- High Performance Trench Technology for Extremely Low $r_{DS(on)}$
- High Power and Current Handling Capability
- This Device is Pb−Free and Halide Free

Applications

- Load Switch in Notebook and Server
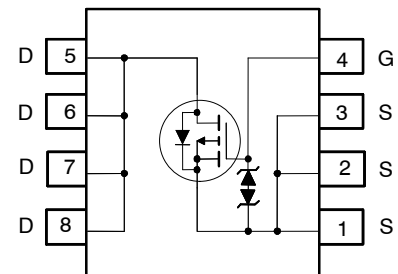- Notebook Battery Pack Power Management

Top   Bottom

WDFN8 3.3x3.3, 0.65P
CASE 511DH

MARKING DIAGRAM
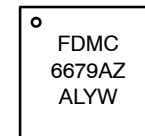
FDMC
6679AZ
ALYW

FDMC6679AZ = Specific Device Code
A = Assembly Location
L = Wafer Lot Number
YW = Assembly Start Week

PIN ASSIGNMENT

D	5	4 G
D	6	3 S
D	7	2 S
D	8	1 S

ORDERING INFORMATION

FDMC6679AZ

MOSFET MAXIMUM RATINGS (T$_A$ = 25°C unless otherwise noted)

Symbol	Parameter			Rating	Unit
V$_{DS}$	Drain to Source Voltage			−30	V
V$_{GS}$	Gate to Source Voltage			±25	V
I$_D$	Drain Current	Continuous	T$_C$ = 25°C	−20	A
		Continuous (Note 1a)	T$_A$ = 25°C	−11.5	
		Pulsed		−32	
P$_D$	Power Dissipation		T$_C$ = 25°C	41	W
	Power Dissipation (Note 1a)		T$_A$ = 25°C	2.3	
T$_J$, T$_{STG}$	Operating and Storage Junction Temperature Range			−55 to + 150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

Symbol	Parameter	Ratings	Unit
R$_{\theta JC}$	Thermal Resistance, Junction to Case	3.0	°C/W
R$_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	53	

1. R$_{\theta JA}$ is determined with the device mounted on a 1 in^2 pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR−4 material. R$_{\theta JC}$ is guaranteed by design while R$_{\theta CA}$ is determined by the user's board design.
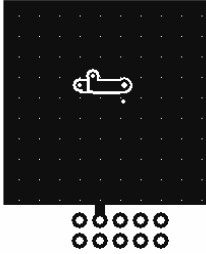
a. 53°C/W when mounted on a 1 in^2 pad of 2 oz copper

b. 125°C/W when mounted on a minimum pad of 2 oz copper

2. Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.
3. The diode connected between the gate and source serves only as protection against ESD. No gate overvoltage rating is implied.

ELECTRICAL CHARACTERISTICS ($T_J = 25°C$ unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = -250 \mu A$, $V_{GS} = 0 V$	−30			V
$\dfrac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = -250 \mu A$, Referenced to 25°C		29		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = -24 V$, $V_{GS} = 0 V$			−1	μA
		$V_{DS} = -24 V$, $V_{GS} = 0 V$, $T_J = 125°C$			−100	
I_{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm25 V$, $V_{DS} = 0 V$			±10	μA
ON CHARACTERISTICS						
$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = -250 \mu A$	−1.0	−1.8	−3	V
$\dfrac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = -250 \mu A$, Referenced to 25°C		−7		mV/°C
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = -10 V$, $I_D = -11.5 A$		8.6	10	mΩ
		$V_{GS} = -4.5 V$, $I_D = -8.5 A$		12	18	
		$V_{GS} = -10 V$, $I_D = -11.5 A$, $T_J = 125°C$		12	15	
g_{FS}	Forward Transconductance	$V_{DS} = -5 V$, $I_D = -11.5 A$		46		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	$V_{DS} = -15 V$, $V_{GS} = 0 V$, $f = 1 MHz$		2985	3970	pF
C_{oss}	Output Capacitance			570	755	pF
C_{rss}	Reverse Transfer Capacitance			500	750	pF
SWITCHING CHARACTERISTICS						
$t_{d(on)}$	Turn−On Delay Time	$V_{DD} = -15 V$, $I_D = -11.5 A$, $V_{GS} = -10 V$, $R_{GEN} = 6 \Omega$		12	21	ns
t_r	Rise Time			14	25	ns
$t_{d(off)}$	Turn−Off Delay Time			63	100	ns
t_f	Fall Time			46	73	ns
Q_g	Total Gate Charge	$V_{GS} = 0 V$ to $-10 V$, $V_{DD} = -15 V$, $I_D = -11.5 A$		65	91	nC
		$V_{GS} = 0 V$ to $-5 V$, $V_{DD} = -15 V$, $I_D = -11.5 A$		37	52	nC
Q_{gs}	Gate to Source Charge	$V_{DD} = -15 V$, $I_D = -11.5 A$		8.7		nC
Q_{gd}	Gate to Drain "Miller" Charge			17		nC
DRAIN−SOURCE DIODE CHARACTERISTICS						
V_{SD}	Source to Drain Diode Forward Voltage	$V_{GS} = 0 V$, $I_S = -11.5 A$ (Note 2)		0.83	1.30	V
		$V_{GS} = 0 V$, $I_S = -1.6 A$ (Note 2)		0.71	1.20	
t_{rr}	Reverse Recovery Time	$I_F = -11.5 A$, $di/dt = 100 A/\mu s$		31	49	ns
Q_{rr}	Reverse Recovery Charge			16	28	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

FDMC6679AZ

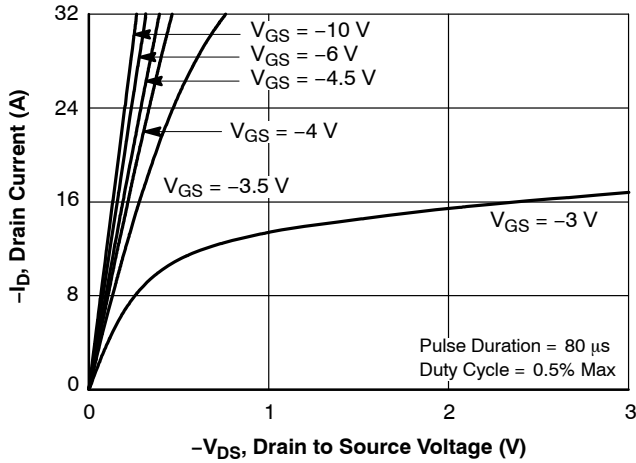**TYPICAL CHARACTERISTICS** (T_J = 25°C unless otherwise noted)

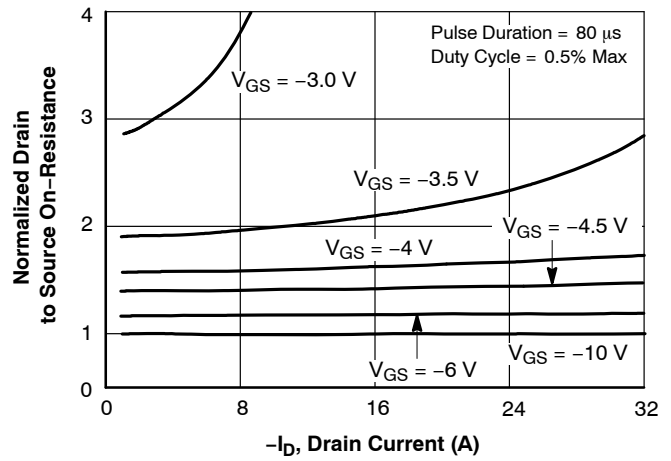Figure 1. On Region Characteristics

Figure 2. Normalized On–Resistance vs.
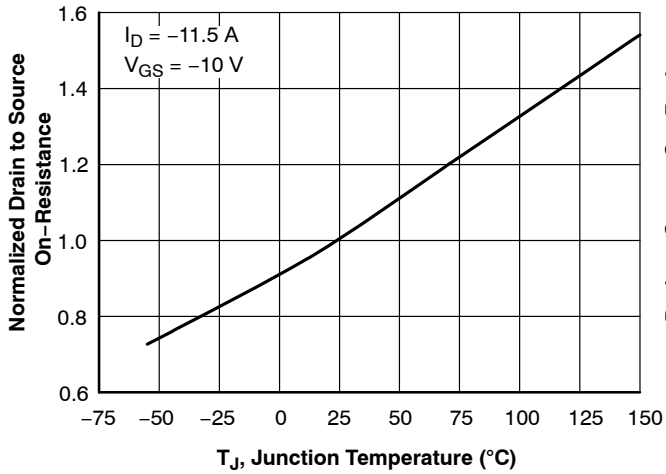Drain Current and Gate Voltage

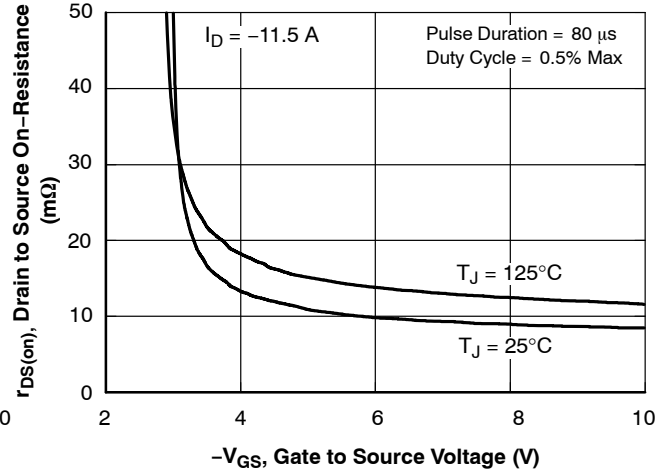Figure 3. Normalized On Resistance
vs. Junction Temperature

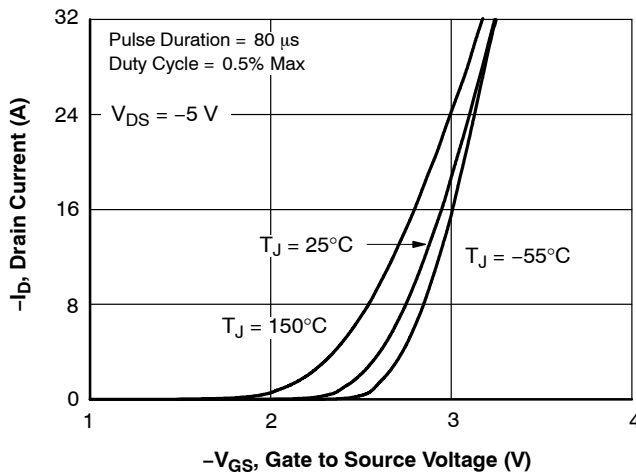Figure 4. On–Resistance vs. Gate to Source
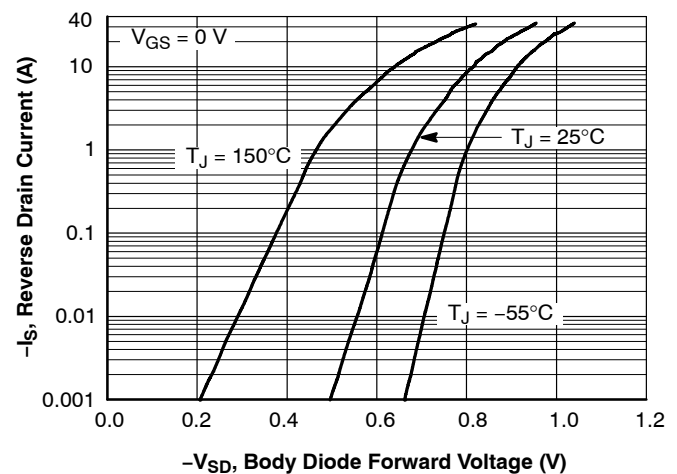Voltage

Figure 5. Transfer Characteristics

Figure 6. Source to Drain Diode Forward
Voltage vs. Source Current

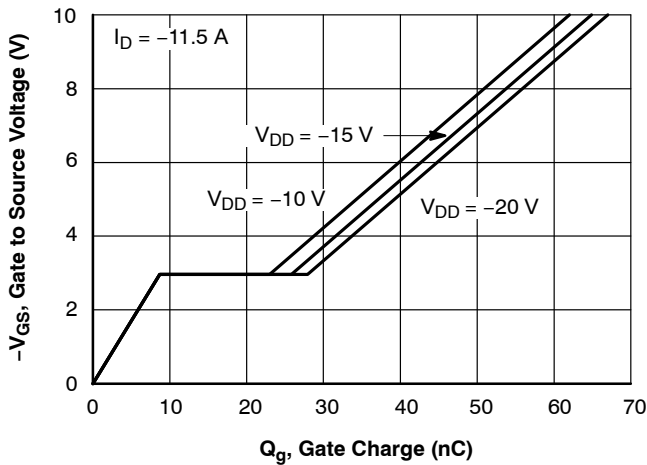**TYPICAL CHARACTERISTICS** (T_J = 25°C unless otherwise noted) (continued)

Figure 7. Gate Charge Characteristics
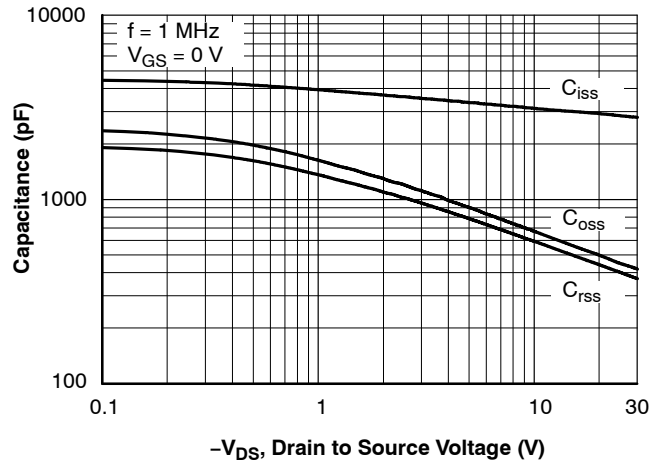
Figure 8. Capacitance vs. Drain to Source Voltage
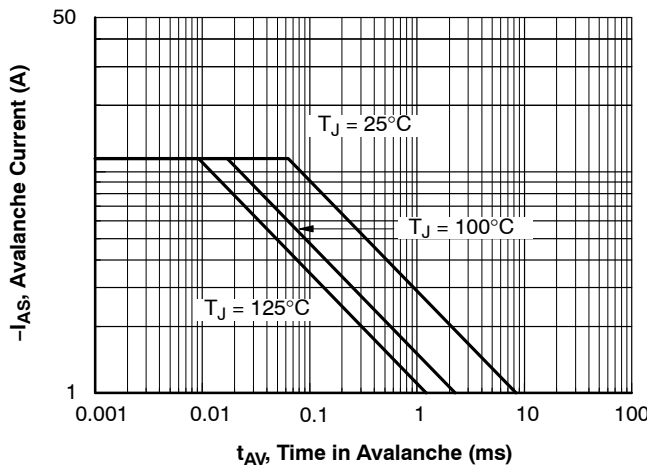
Figure 9. Unclamped Inductive Switching Capability
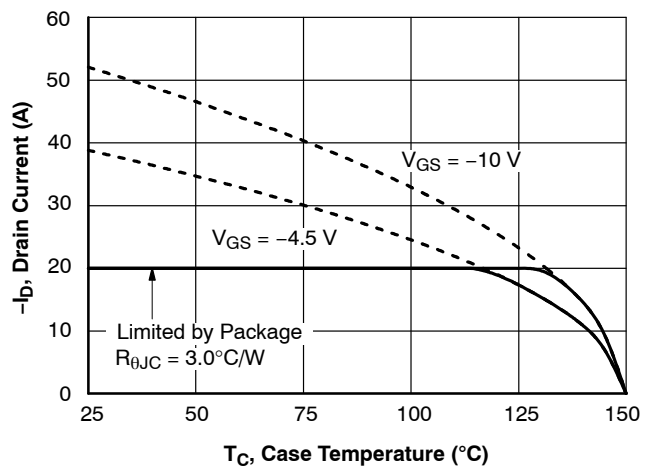
Figure 10. Maximum Continuous Drain Current vs Case Temperature
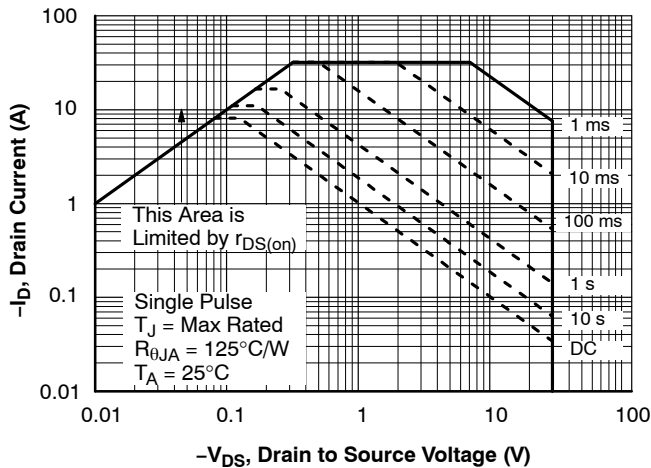
Figure 11. Forward Bias Safe Operating Area
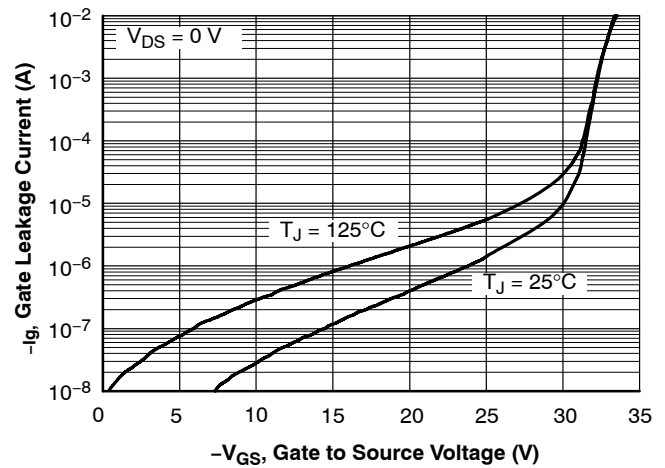
Figure 12. Igss vs. Vgss

TYPICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted) (continued)

Figure 13. Single Pulse Maximum Power Dissipation
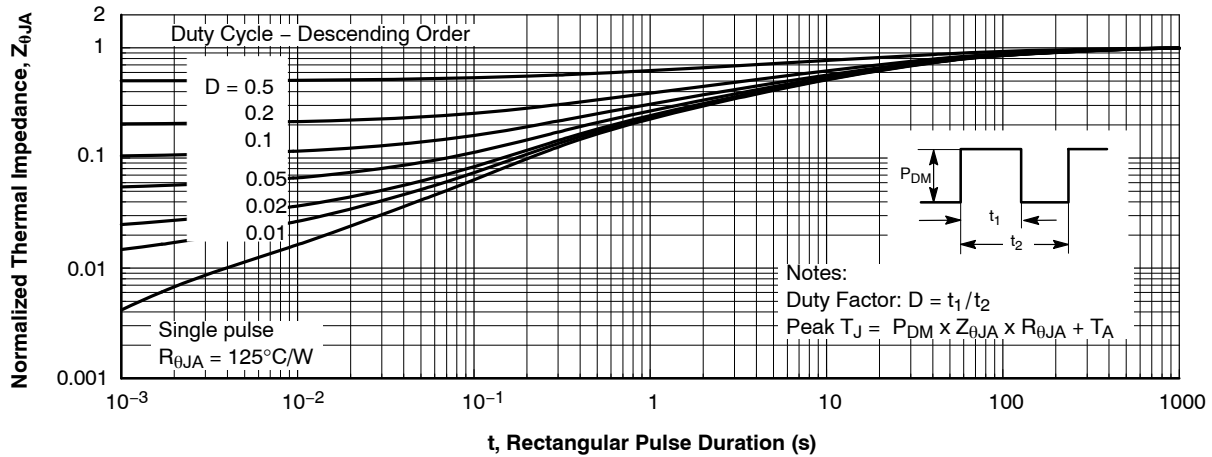
Figure 14. Junction−to−Ambient Transient Thermal Response Curve

ORDERING INFORMATION

Device	Device Marking	Package Type	Shipping†
FDMC6679AZ	FDMC6679AZ	WDFN8 3.3x3.3, 0.65P, Case 511DH (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

WDFN8 3.3x3.3, 0.65P
CASE 511DH
ISSUE O

DATE 31 JUL 2016

TOP VIEW

PIN#1 IDENT

SIDE VIEW

SEATING PLANE

BOTTOM VIEW

PIN #1 IDENT

RECOMMENDED LAND PATTERN

KEEP OUT AREA

NOTES:

A. DOES NOT CONFORM TO JEDEC REGISTRATION MO−229

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.

D. LAND PATTERN RECOMMENDATION IS EXISTING INDUSTRY LAND PATTERN.

DOCUMENT NUMBER:	98AON13625G	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.	
DESCRIPTION:	WDFN8 3.3X3.3, 0.65P		PAGE 1 OF 1

© Semiconductor Components Industries, LLC, 2019   www.onsemi.com

PUBLICATION ORDERING INFORMATION

◊

单击下面可查看定价，库存，交付和生命周期等信息

>>ON Semiconductor(安森美)