# 2SB1156

### Silicon PNP epitaxial planar type

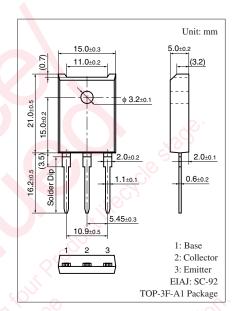
For power switching Complementary to 2SD1707

#### ■ Features

- ullet Low collector-emitter saturation voltage  $V_{\text{CE(sat)}}$
- Satisfactory linearity of forward current transfer ratio h<sub>FE</sub>
- Large collector current I<sub>C</sub>
- Full-pack package which can be installed to the heat sink with one screw

#### ■ Absolute Maximum Ratings $T_C = 25^{\circ}C$

Parameter	Symbol	Rating	Unit	
Collector-base voltage (Emitter open)	$V_{CBO}$	-130	V	
Collector-emitter voltage (Base open)	V <sub>CEO</sub>	-80	V	
Emitter-base voltage (Collector open)	$V_{EBO}$	-7	V	
Collector current	$I_{C}$	-20	A	
Peak collector current	$I_{CP}$	-30	A	
Collector power dissipation	P <sub>C</sub>	100	W	
$T_a = 25^{\circ}C$		3		
Junction temperature	$T_{j}$	150	°C	
Storage temperature	$T_{stg}$	-55 to +150	°C×(	



### ■ Electrical Characteristics $T_C = 25^{\circ}C \pm 3^{\circ}C$

Parameter	Symbol	Conditions	Min	Тур	Max	Unit
Collector-emitter voltage (Base open)	$V_{CEO}$	$I_C = -10 \text{ mA}, I_B = 0$	-80	35		V
Collector-base cutoff current (Emitter open)	$I_{CBO}$	$V_{CB} = -100 \text{ V}, I_E = 0$	20/		-10	μΑ
Emitter-base cutoff current (Collector open)	$I_{EBO}$	$V_{EB} = -5 \text{ V}, I_C = 0$	1.7		-50	μΑ
Forward current transfer ratio	h <sub>FE1</sub>	$V_{CE} = -2 \text{ V}, I_{C} = -0.1 \text{ A}$	45			_
	h <sub>FE2</sub> *	$V_{CE} = -2 \text{ V}, I_C = -3 \text{ A}$	60		260	
	h <sub>FE3</sub>	$V_{CE} = -2 \text{ V}, I_C = -10 \text{ A}$	30			
Collector-emitter saturation voltage	V <sub>CE(sat)1</sub>	$I_C = -8 \text{ A}, I_B = -0.4 \text{ A}$			- 0.5	V
	V <sub>CE(sat)2</sub>	$I_C = -20 \text{ A}, I_B = -2 \text{ A}$			-1.5	
Base-emitter saturation voltage	V <sub>BE(sat)1</sub>	$I_C = -8 \text{ A}, I_B = -0.4 \text{ A}$			-1.5	V
	V <sub>BE(sat)2</sub>	$I_C = -20 \text{ A}, I_B = -2 \text{ A}$			-2.5	
Transition frequency	$f_T$	$V_{CE} = -10 \text{ V}, I_{C} = -0.5 \text{ A}, f = 10 \text{ MHz}$		30		MHz
Turn-on time	t <sub>on</sub>	$I_C = -8 \text{ A}, I_{B1} = -0.8 \text{ A}, I_{B2} = 0.8 \text{ A}$		0.5		μs
Storage time	t <sub>stg</sub>	$V_{CC} = -50 \text{ V}$		1.0		μs
Fall time	t <sub>f</sub>			0.2		μs

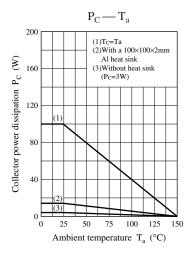
Note) 1. Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030 measuring methods for transistors.

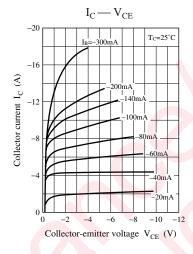
#### 2. \*: Rank classification

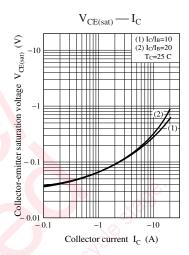
Rank	R	Q	Р
h <sub>FE2</sub>	60 to 120	90 to 180	130 to 260

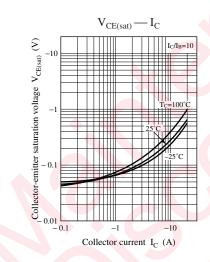
Ordering can be made by the common rank (PQ rank  $h_{FE2}=60\ to\ 240)$  in the rank classification.

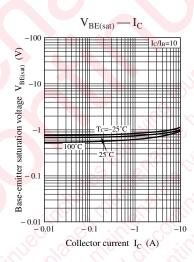
### **Panasonic**

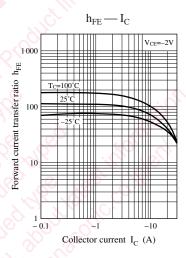


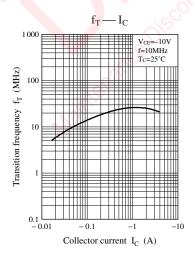


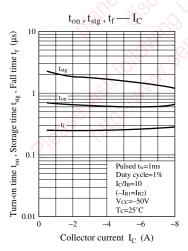


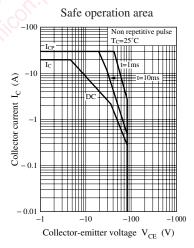


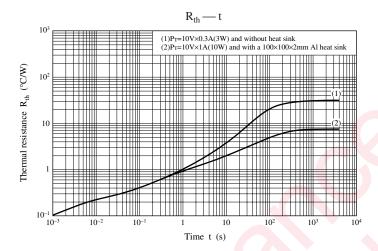












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