2SC3507

Silicon NPN triple diffusion planar type

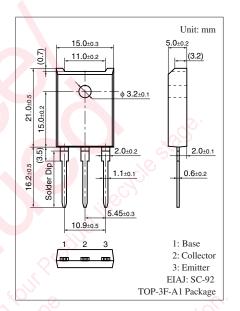
For high breakdown voltage high-speed switching

■ Features

- High-speed switching
- ullet High collector-base voltage (Emitter open) V_{CBO}
- Satisfactory linearity of forward current transfer ratio h_{FE}
- Full-pack package which can be installed to the heat sink with one screw

■ Absolute Maximum Ratings $T_C = 25^{\circ}C$

Parameter	Symbol	Rating	Unit	
Collector-base voltage (Emitter open)	V _{CBO}	1 000	V	
Collector-emitter voltage (E-B short)	V _{CES}	1 000	V	
Collector-emitter voltage (Base open)	V _{CEO}	800	V	
Emitter-base voltage (Collector open)	$V_{\rm EBO}$	7	V	
Collector current	I_{C}	5	A	
Base current	I _B	3	A	
Peak collector current	I_{CP}	10	A	
Collector power dissipation	P _C	80	w	
$T_a = 25^{\circ}C$		3.0	<i>KO.</i>	
Junction temperature	T _j	150	°C	
Storage temperature	T_{stg}	-55 to +150	°C	

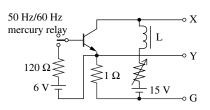


■ Electrical Characteristics $T_C = 25^{\circ}C \pm 3^{\circ}C$

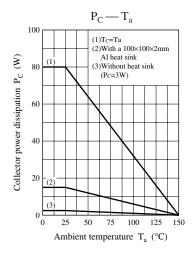
Parameter	Symbol	Conditions	Min	Тур	Max	Unit
Collector-emitter sustaining voltage *	V _{CEO(SUS)}	$I_C = 0.5 \text{ A}, L = 50 \text{ mH}$	800			V
Collector-base cutoff current (Emitter open)	I_{CBO}	$V_{CB} = 1000 \text{ V}, I_E = 0$	1.,		50	μΑ
Emitter-base cutoff current (Collector open)	I _{EBO}	$V_{EB} = 7 \text{ V}, I_{C} = 0$			50	μΑ
Forward current transfer ratio	h _{FE}	$V_{CE} = 5 \text{ V}, I_{C} = 3 \text{ A}$	6			_
Collector-emitter saturation voltage	V _{CE(sat)}	$I_C = 3 \text{ A}, I_B = 0.6 \text{ A}$			1.5	V
Base-emitter saturation voltage	V _{BE(sat)}	$I_C = 3 \text{ A}, I_B = 0.6 \text{ A}$			1.5	V
Transition frequency	f_T	$V_{CE} = 5 \text{ V}, I_{C} = 0.5 \text{ A}, f = 1 \text{ MHz}$		6		MHz
Turn-on time	t _{on}	$I_C = 3 A$			1.0	μs
Storage time	t _{stg}	$I_{B1} = 0.6 \text{ A}, I_{B2} = -1.2 \text{ A}$			2.5	μs
Fall time	t _f	$V_{CC} = 250 \text{ V}$			0.5	μs

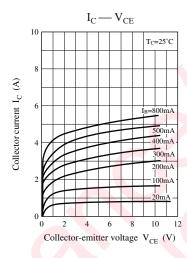
Note) 1. Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030 measuring methods for transistors.

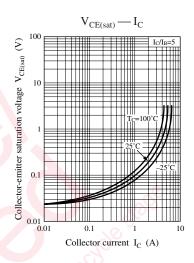
2. *: V_{CEO(SUS)} test circuit

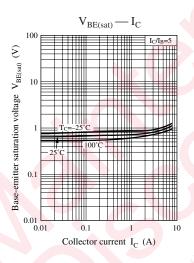


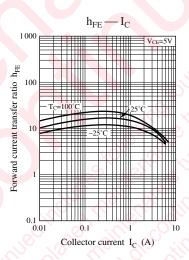
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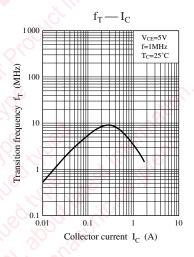


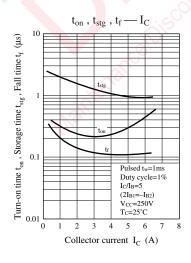


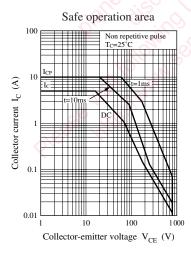




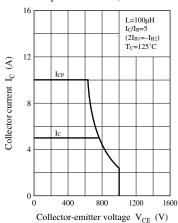




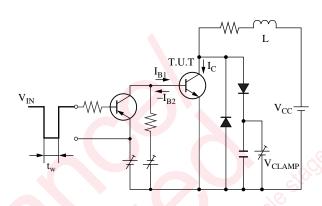


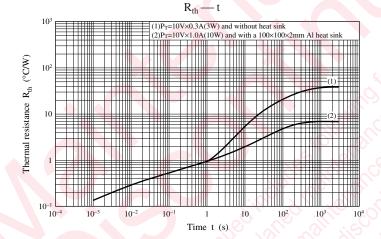


Safe operation area (Reserve bias)



Safe operation area (Reserve bias) measurement circuit





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