

2SD1773

Silicon NPN triple diffusion planar type darlington

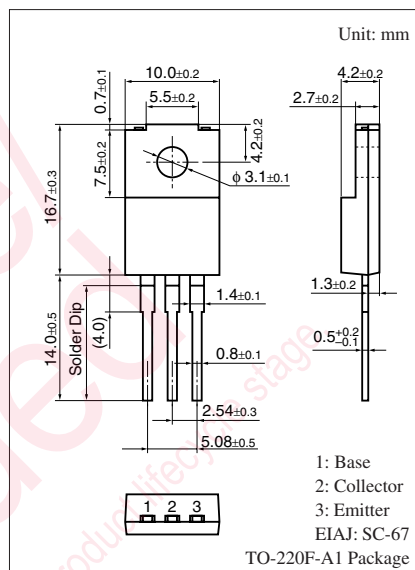
For medium speed switching
Complementary to 2SB1193

■ Features

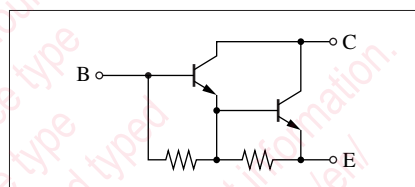
- High forward current transfer ratio h_{FE}
- High-speed switching
- Full-pack package which can be installed to the heat sink with one screw

■ Absolute Maximum Ratings $T_C = 25^\circ C$

Parameter	Symbol	Rating	Unit
Collector-base voltage (Emitter open)	V_{CBO}	120	V
Collector-emitter voltage (Base open)	V_{CEO}	120	V
Emitter-base voltage (Collector open)	V_{EBO}	7	V
Collector current	I_C	8	A
Peak collector current	I_{CP}	12	A
Collector power dissipation	P_C	50	W
	$T_a = 25^\circ C$	2.0	
Junction temperature	T_j	150	$^\circ C$
Storage temperature	T_{stg}	-55 to +150	$^\circ C$



Internal Connection

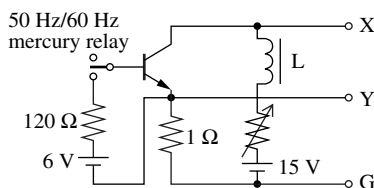


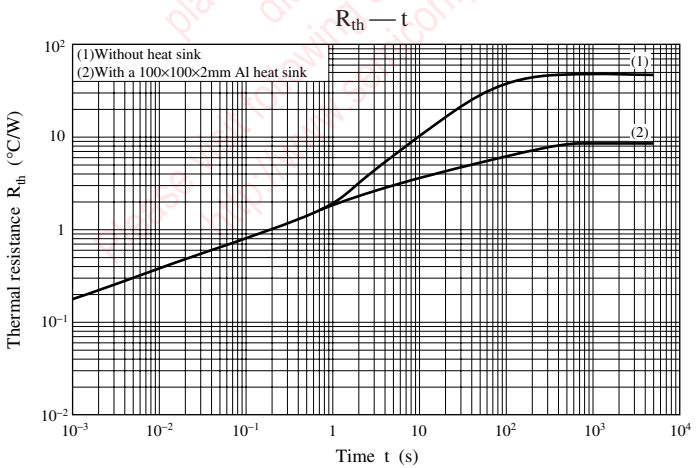
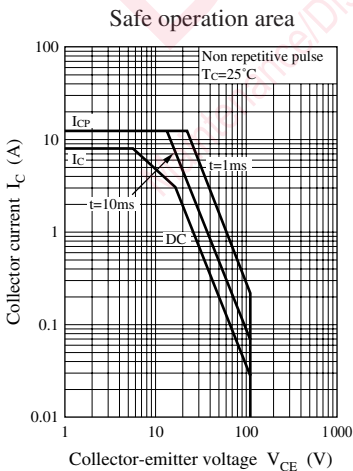
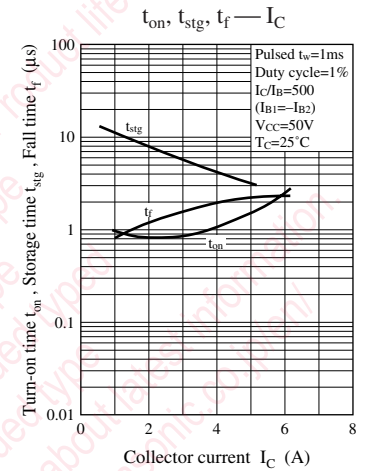
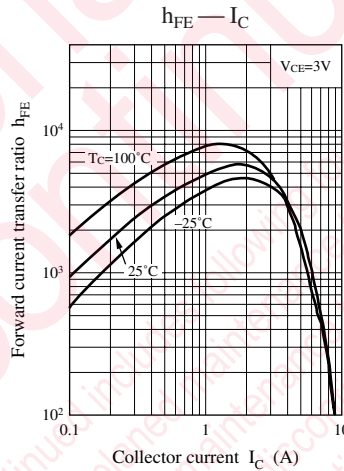
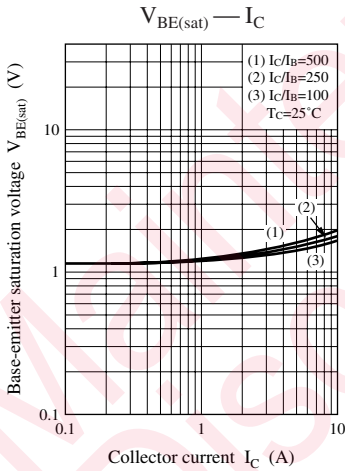
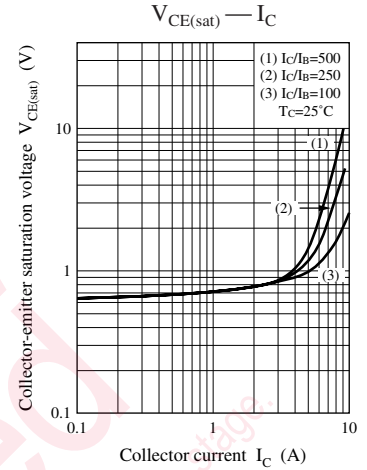
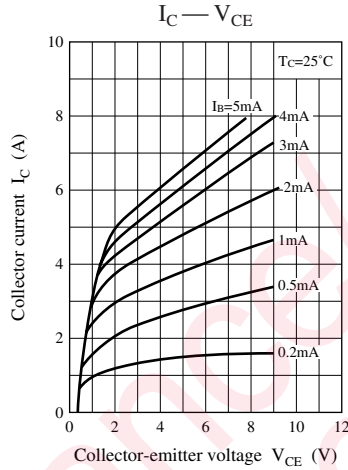
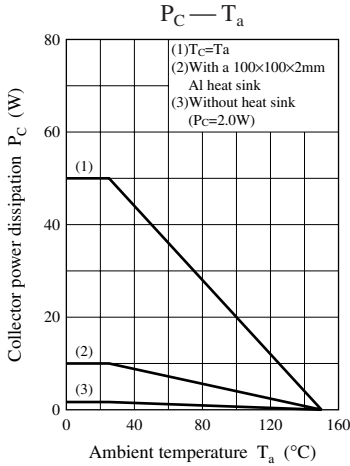
■ Electrical Characteristics $T_C = 25^\circ C \pm 3^\circ C$

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Collector-emitter sustaining voltage *	$V_{CEO(SUS)}$	$I_C = 2 A, R_{BE} = \infty, L = 10 mH$	120			V
Emitter-base voltage (Collector open)	V_{EBO}	$I_E = 50 mA, I_C = 0$	7			V
Collector-base cutoff current (Emitter open)	I_{CBO}	$V_{CB} = 120 V, I_E = 0$			100	μA
Collector-emitter cutoff current (Base open)	I_{CEO}	$V_{CE} = 100 V, R_{BE} = \infty$			10	μA
Forward current transfer ratio	h_{FE}	$V_{CE} = 3 V, I_C = 4 A$	1000		20000	—
Collector-emitter saturation voltage	$V_{CE(sat)1}$	$I_C = 4 A, I_B = 8 mA$			1.5	V
	$V_{CE(sat)2}$	$I_C = 8 A, I_B = 80 mA$			3.0	
Base-emitter saturation voltage	$V_{BE(sat)1}$	$I_C = 4 A, I_B = 8 mA$			2.0	V
	$V_{BE(sat)2}$	$I_C = 8 A, I_B = 80 mA$			3.5	
Transition frequency	f_T	$V_{CE} = 10 V, I_C = 1 A, f = 1 MHz$		20		MHz
Turn-on time	t_{on}	$I_C = 4 A, I_{B1} = 8 mA, I_{B2} = -8 mA,$		0.7		μs
Storage time	t_{stg}	$V_{CC} = 50 V$		6.0		μs
Fall time	t_f			2.0		μs

Note) 1. Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030 measuring methods for transistors.

2. *: $V_{CEO(SUS)}$ Test circuit





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