# Notification about the transfer of the semiconductor business

The semiconductor business of Panasonic Corporation was transferred on September 1, 2020 to Nuvoton Technology Corporation (hereinafter referred to as "Nuvoton"). Accordingly, Panasonic Semiconductor Solutions Co., Ltd. became under the umbrella of the Nuvoton Group, with the new name of Nuvoton Technology Corporation Japan (hereinafter referred to as "NTCJ").

In accordance with this transfer, semiconductor products will be handled as NTCJ-made products after September 1, 2020. However, such products will be continuously sold through Panasonic Corporation.

Publisher of this Document is NTCJ.
If you would find description "Panasonic" or "Panasonic semiconductor solutions", please replace it with NTCJ.
　　　※ Except below description page
　　　　 "Request for your special attention and precautions in using the technical
　　　　　information and semiconductors described in this book"

<div style="text-align:center">Nuvoton Technology Corporation Japan</div>

**Panasonic**

# AN41919A

## DC IRIS Control LSI for IP Camera and Network Camera

### FEATURES

・Built-in DC IRIS controller

・DC IRIS control by 4-line serial data communication

・PCB space saving

・Low power consumption of Iris drive by PWM

・DC Iris servo High-speed response and High stability

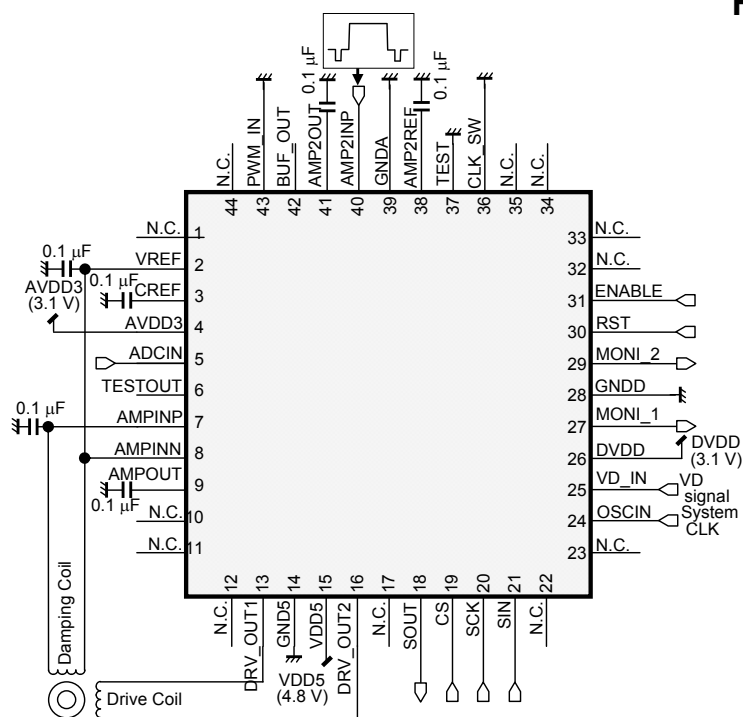・44 pin Plastic Quad Flat Non-leaded Package
  (QFN Type)

### DESCRIPTION

AN41919A is a DC IRIS control LSI for IP camera and security camera. It integrates digital PID control circuit and is able to control various IRIS motors.

### APPLICATIONS

・IP camera, security camera

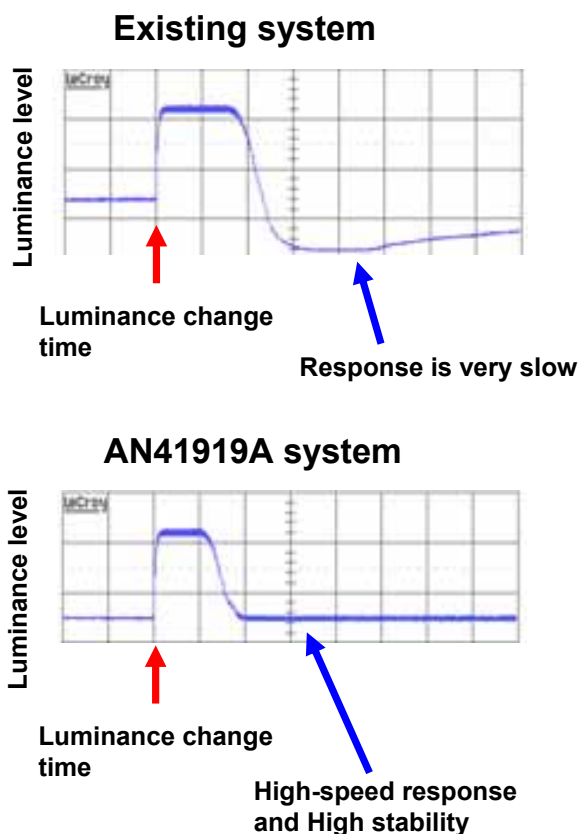### SIMPLIFIED APPLICATION



Notes)

This application circuit is an example. The operation of mass production set is not guaranteed. You should perform enough evaluation and verification on the design of mass production set. You are fully responsible for the incorporation of the above application circuit and information in the design of your equipment.

### DC Iris servo High-speed response and High stability.

**Existing system**



Luminance change time

Response is very slow

**AN41919A system**



Luminance change time

High-speed response and High stability

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# AN41919A

## ABSOLUTE MAXIMUM RATINGS

| Parameter | Symbol | Rating | Unit | Note |
|---|---|---|---|---|
| Controller supply voltage | AVDD3 | −0.3 to +4.0 | V | *1 |
| | DVDD | −0.3 to +4.0 | | |
| Supply voltage for motor controller | VDD5 | −0.3 to +6.0 | V | *1 |
| Operating ambient temperature | $T_{opr}$ | −20 to +85 | °C | *2, *4 |
| Operating junction temperature | $T_j$ | −20 to + 125 | °C | *2 |
| Storage temperature | $T_{stg}$ | −55 to +125 | °C | *2 |
| Motor driver H bridge drive current | DRV_OUT1, DRV_OUT2 | ±0.15 | A/ch | — |
| Input Voltage Range | ADCIN, AMPINP, AMPINN, AMP2INP, CREF, AMP2REF | −0.3 to (AVDD3 + 0.3) | V | *3 |
| | CS, SCK, SIN, OSCIN, VD_IN, RST, ENABLE, CLK_SW, TEST, PWM_IN | −0.3 to (DVDD + 0.3) | V | *3 |
| Output Voltage Range | VREF, TESTOUT, AMPOUT, AMP2OUT | −0.3 to (AVDD3 + 0.3) | V | *3 |
| | SOUT, MONI_1, MONI_2, BUF_OUT | −0.3 to (DVDD + 0.3) | V | *3 |
| ESD | HBM (Human Body Model) | ±2 | kV | — |
| | CDM (Charge Device Model) | ±1 | kV | — |

Notes). This product may sustain permanent damage if subjected to conditions higher than the above stated absolute maximum rating. This rating is the maximum rating and device operating at this range is not guaranteeable as it is higher than our stated recommended operating range.
When subjected under the absolute maximum rating for a long time, the reliability of the product may be affected.

*1:The values under the condition not exceeding the above absolute maximum ratings and the power dissipation.

*2:Except for the power dissipation, operating ambient temperature, and storage temperature, all ratings are for Ta = 25°C.

*3: (DVDD + 0.3 ) V must not be exceeded 4.0 V and  (AVDD + 0.3 ) V must not be exceeded 4.0 V.

*4:The power dissipation shown is the value at Ta = 85°C for the independent (unmounted) IC package without a heat sink. When using this IC, refer to the PD-Ta diagram of the package standard and design the heat radiation with sufficient margin so that the allowable value might not be exceeded based on the conditions of power supply voltage, load, and ambient temperature.

## POWER DISSIPATION RATING

| Condition | θ JA | PD (Ta=25 °C) | PD (Ta=70 °C) |
|---|---|---|---|
| Mount on PWB *1 | 71.8℃/W | 1.392W | 0.765W |
| Without PWB | 282.9℃/W | 0.353W | 0.194W |

Note). For the actual usage, please refer to the PD-Ta characteristics diagram in the package specification, supply voltage, load and ambient temperature conditions to ensure that there is enough margin follow the power and the thermal design does not exceed the allowable value.

*1: Glass-Epoxy: 50×50×0.8 (mm) ,  heat dissipation fin: Dai-pad , the state where it does not mount.

### CAUTION

Although this has limited built-in ESD protection circuit, but permanent damage may occur on it. Therefore, proper ESD precautions are recommended to avoid electrostatic damage to the MOS gates

## RECOMMENDED OPERATING CONDITIONS

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Note |
|---|---|---|---|---|---|---|
| Supply voltage range | AVDD3, DVDD | 2.7 | 3.1 | 3.6 | V | *1 |
| | VDD5 | 3.0 | 4.8 | 5.5 | V | *1 |
| Input Voltage Range | ADCIN, AMPINP, AMPINN, AMP2INP, CREF, AMP2REF | –0.3 | – | AVDD3 + 0.3 | V | *2 |
| | CS, SCK, SIN, OSCIN, VD_IN, RST, ENABLE, CLK_SW, TEST, PWM_IN | –0.3 | – | DVDD + 0.3 | V | *2 |
| Output Voltage Range | VREF, TESTOUT, AMPOUT, AMP2OUT | –0.3 | – | AVDD3 + 0.3 | V | *2 |
| | SOUT, MONI_1, MONI_2, BUF_OUT | –0.3 | – | DVDD + 0.3 | V | *2 |
| Output Current Range | DRV_OUT1, DRV_OUT2 | –0.15 | – | 0.15 | A | *1 |
| External Constants | $C_{VREF}$ | | 0.1 | | μF | |
| | $C_{CREF}$ | | 0.1 | | μF | |
| | $C_{AMPINP}$ | | 0.1 | | μF | |
| | $C_{AMPOUT}$ | | 0.1 | | μF | |
| | $C_{AMP2REF}$ | | 0.1 | | μF | |
| | $C_{AMP2OUT}$ | | 0.1 | | μF | |
| Operating ambient temperature | $Ta^{opr}$ | -20 | | 85 | ℃ | |

Note) *1 : The values under the condition not exceeding the above absolute maximum ratings and the power dissipation.
*2 : (DVDD + 0.3 ) V must not be exceeded 4.0 V and  (AVDD + 0.3 ) V must not be exceeded 4.0 V.

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## ELECRTRICAL CHARACTERISTICS

VDD5 = 4.8 V, DVDD = AVDD3 = 3.1 V.    $T_a$ = 25°C±2°C

| Parameter | Symbol | Condition | Limits | | | Unit | Note |
|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | | |
| **Current circuit** | | | | | | | |
| 3 V supply current on Reset | Icc3$_{reset}$ | RST = Low, No 27 MHz input | — | 0 | 10.0 | μA | — |
| 3 V supply current on Enable | Icc3$_{enable}$ | RST = High, ENABLE = High, 27 MHz input, Output open | — | 7 | 14 | mA | — |
| VDD5 supply current on Reset | Icc5$_{reset}$ | RST = Low, No 27 MHz input | — | 0 | 3.0 | μA | — |
| VDD5 supply current on Enable | Icc5$_{enable}$ | RST = High, ENABLE = High, 27 MHz input, Output open | — | 0.2 | 0.4 | mA | — |
| Supply current on Standby | Icc$_{standby}$ | RST = High, ENABLE = Low, 27 MHz input, output open Total current | — | 2 | 4 | mA | — |
| **Digital input / output** | | | | | | | |
| High-level input | $V_{in(H)}$ | RST | 0.54 × DVDD | — | DVDD + 0.3 | V | — |
| Low-level input | $V_{in(L)}$ | RST | −0.3 | — | 0.2 × DVDD | V | — |
| SOUT High-level output | $V_{out(H)}$ : SDATA | [SOUT] 1 mA Source | DVDD − 0.5 | — | — | V | — |
| SOUT Low-level output | $V_{out(L)}$ : SDATA | [SOUT] 1 mA Sink | — | — | 0.5 | V | — |
| MONI_1 to 2 High-level output | $V_{out(H)}$ : MUX | — | 0.9 × DVDD | — | — | V | — |
| MONI_1 to 2 Low-level output | $V_{out(L)}$ : MUX | — | — | — | 0.1 × DVDD | V | — |
| Input pull-down resistance | $R_{pullret}$ | RST, ENABLE | 50 | 100 | 200 | kΩ | — |
| **Motor driver** | | | | | | | |
| H bridge ON resistance | $R_{onIR}$ | IM = 50 mA | — | — | 5 | Ω | — |
| H bridge leak current | $I_{leakIR}$ | — | — | — | 0.8 | μA | — |

## ELECRTRICAL CHARACTERISTICS （Continued）

VM=24V,$T_a$ = 25°C±2°C unless otherwise noted.

| Parameter | Symbol | Condition | Limits | | | Unit | Note |
|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | | |
| **AMP (Damping Coil signal Amplifier)** | | | | | | | |
| Input voltage range | $V_{IN}$ | AMPINN = 1.55 V | 1.05 | — | 2.05 | V | — |
| Input offset voltage | $V_{OF}$ | — | −15 | — | 15 | mV | — |
| Output voltage (Low) | $V_{OL}$ | ILOAD = −100 μA | — | 0.2 | 0.4 | V | — |
| Output voltage (High) | $V_{OH}$ | ILOAD = 100 μA | AVDD3 − 0.4 | AVDD3 − 0.2 | — | V | — |
| Gain | $V_{OG}$ | Gain setting value : 0h | 19.7 | 21.9 | 24.1 | V/V | — |
| **AMP2 (CDS signal Amplifier)** | | | | | | | |
| Input offset voltage | $V_{OF2}$ | — | −20 | — | 20 | mV | — |
| Output voltage (Low) | $V_{OL2}$ | ILOAD = −100 μA | — | 0.2 | 0.4 | V | — |
| Output voltage (High) | $V_{OH2}$ | ILOAD = 100 μA | AVDD3 − 0.4 | AVDD3 − 0.2 | — | V | — |
| Gain | $V_{OG2}$ | Gain setting value : 9h | 1.75 | 2 | 2.25 | V/V | — |
| **Reference Voltage Block** | | | | | | | |
| Output voltage | VREF | ILOAD = 0 A, CVREF = 0.1 μF | 1.45 | 1.55 | 1.65 | V | — |

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## ELECRTRICAL CHARACTERISTICS (continued)

VDD5 = 4.8 V, DVDD = AVDD3 = 3.1 V　　$T_a$ = 25°C±2°C

| Parameter | Symbol | Condition | Limits | | | Unit | Note |
|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | | |
| **Serial port input** | | | | | | | |
| Serial clock | Sclock | — | 1 | — | 5 | MHz | *1 |
| SCK low time | T1 | — | 100 | — | — | ns | *1 |
| SCK high time | T2 | — | 100 | — | — | ns | *1 |
| CS setup time | T3 | — | 60 | — | — | ns | *1 |
| CS hold time | T4 | — | 60 | — | — | ns | *1 |
| CS disable high time | T5 | — | 100 | — | — | ns | *1 |
| SIN setup time | T6 | — | 50 | — | — | ns | *1 |
| SIN hold time | T7 | — | 50 | — | — | ns | *1 |
| SOUT delay time | T8 | — | — | — | 60 | ns | *1 |
| SOUT hold time | T9 | — | 60 | — | — | ns | *1 |
| SOUT Enable-Hi-Z time | T10 | — | — | — | 60 | ns | *1 |
| SOUT Hi-Z-Enable time | T11 | — | — | — | 60 | ns | *1 |
| SOUT  C load | $T_{SC}$ | — | — | — | 40 | pF | *1 |
| **Digital input / output** | | | | | | | |
| High-level input threshold voltage | $V_{in(H)}$ | SCK, SIN, CS, OSCIN, VD_IN, ENABLE, CLK_SW TEST | — | 1.36 | — | V | *1 |
| Low-level input threshold voltage | $V_{in(L)}$ | SCK, SIN, CS, OSCIN, VD_IN, ENABLE, CLK_SW TEST | — | 1.02 | — | V | *1 |
| RST signal pulse width | $T_{rst}$ | — | 100 | — | — | µs | *1 |
| Input hysteresis width | $V_{hysin}$ | SCK, SIN, CS, OSCIN, VD_IN, ENABLE, CLK_SW TEST | — | 0.34 | — | V | *1 |
| CS signal wait time 1 | $T_{(VD-CS)}$ | — | 400 | — | — | ns | *1 |
| CS signal wait time 2 | $T_{(CS-DT1)}$ | — | 5 | — | — | µs | *1 |

Note)　*1　: Typical Value checked by design.

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## ELECRTRICAL CHARACTERISTICS (Continued)

VDD5 = 4.8 V, DVDD = AVDD3 = 3.1 V     $T_a$ = 25°C±2°C

| Parameter | Symbol | Condition | Limits | | | Unit | Note |
|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | | |
| **IRIS control** | | | | | | | |
| AD sampling frequency | IRIS$_{Sample}$ | OSCIN = 27 MHz | — | 500 | — | kHz | *1 |
| **Thermal shutdown** | | | | | | | |
| Thermal shutdown operation temperature | T$_{tsd}$ | — | — | 150 | — | °C | *1 |
| Thermal shutdown hysteresis width | ΔT$_{tsd}$ | — | — | 40 | — | °C | *1 |
| **Supply voltage monitor circuit** | | | | | | | |
| AVDD3 Reset operation | V$_{rston}$ | — | — | 2.27 | — | V | *1 |
| AVDD3 Reset hysteresis width | V$_{rsthys}$ | — | — | 0.2 | — | V | *1 |
| VDD5 Reset operation | V$_{rstlSon}$ | — | — | 2.2 | — | V | *1 |
| VDD5 Reset hysteresis width | V$_{rstlShys}$ | — | — | 0.2 | — | V | *1 |
| **8 bit DAC for Damping Coil signal Amplifier Offset adjustment** | | | | | | | |
| Adjustment range (High) | DAOTHof | — | — | AVDD3 | — | V | *1 |
| Adjustment range (Low) | DAOTLof | — | — | 0 | — | V | *1 |
| **10 bit ADC** | | | | | | | |
| Input Range (High) | V$_{in(H)}$ | — | — | — | AVDD3 − 0.2 | V | *1 |
| Input Range (Low) | V$_{in(L)}$ | — | 0.2 | — | — | V | *1 |
| DNLE (Differential linearity error) | DNL10A | — | — | 1.0 | — | LSB | *1 |
| INLE (Integral linearity error) | INL10A | — | — | 2.0 | — | LSB | *1 |
| **Reference voltage output block** | | | | | | | |
| Output voltage 1 | VREFH | ILOAD = 100 mA, CVREF = 0.1 mF | — | — | VREF + 0.1 | V | *1 |
| Output voltage 2 | VREFL | ILOAD = -100 mA, CVREF = 0.1 mF | VREF − 0.1 | — | — | V | *1 |

Note) *1 : Typical Value checked by design.

## PIN CONFIGURATION

Top View

| Pin | Name | | Pin | Name |
|-----|------|--|-----|------|
| 1 | N.C. | | 33 | N.C. |
| 2 | VREF | | 32 | N.C. |
| 3 | CREF | | 31 | ENABLE |
| 4 | AVDD3 | | 30 | RST |
| 5 | ADCIN | | 29 | MONI_2 |
| 6 | TESTOUT | | 28 | GRDD |
| 7 | AMPINP | | 27 | MON_1 |
| 8 | AMPINN | | 26 | DVDD |
| 9 | AMPOUT | | 25 | VD_IN |
| 10 | N.C. | | 24 | OSCIN |
| 11 | N.C. | | 23 | N.C. |

Top pins (44–34): N.C., PWM_IN, BUF_OUT, AMP2OUT, AMP2INP, GRDA, AMP2REF, TEST, CLK_SW, N.C., N.C.

Bottom pins (12–22): N.C., DRV_OUT1, GRD5, VDD5, DRV_OUT2, N.C., SOUT, CS, SCK, SIN, N.C.
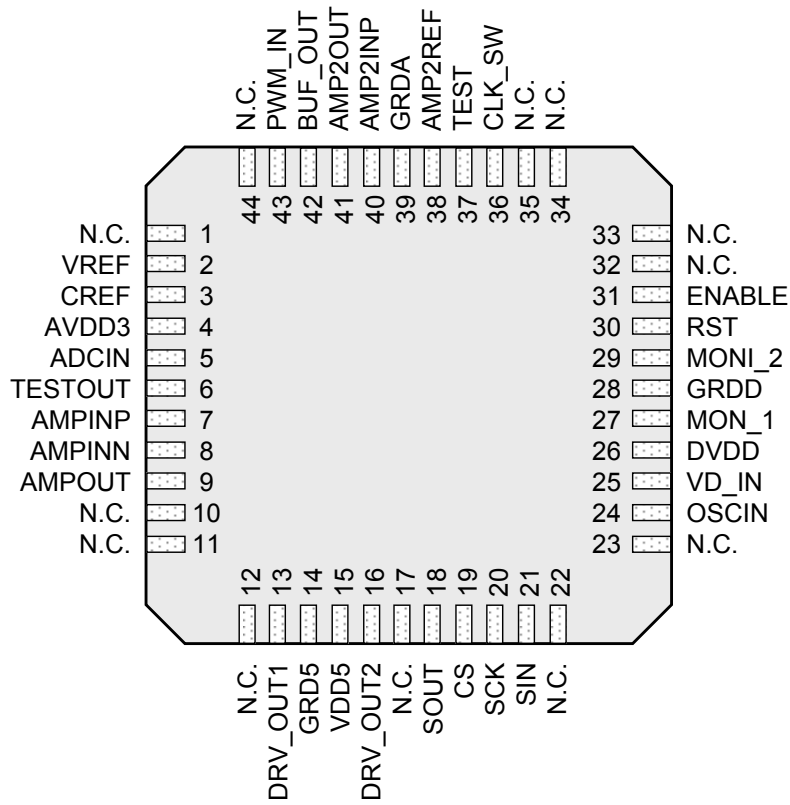
## PIN FUNCTIONS

| Pin No. | Pin name | Type | Description |
|---|---|---|---|
| 1, 10,11,12, 17, 22, 23, 32, 33, 34, 35, 44 | N.C. | — | N.C. |
| 2 | VREF | Output | Reference voltage for damping coil signal amplifier |
| 3 | CREF | — | (AVDD3)/2 capacitor connection pin |
| 4 | AVDD3 | Power supply | 3 V analog power supply |
| 5 | ADCIN | Input | ADC test input |
| 6 | TESTOUT | Output | Test output |
| 7 | AMPINP | Input | Damping coil signal amplifier non-inverting input |
| 8 | AMPINN | Input | Damping coil signal amplifier inverting input |
| 9 | AMPOUT | Output | Damping coil signal amplifier output |
| 13 | DRV_OUT1 | Output | Motor output 1 |
| 14 | GND5 | Ground | GND for motor |
| 15 | VDD5 | Power supply | Power supply for motor |
| 16 | DRV_OUT2 | Output | Motor output 2 |
| 18 | SOUT | Output | Serial data output |
| 19 | CS | Input | Chip select signal input |
| 20 | SCK | Input | Serial clock input |
| 21 | SIN | Input | Serial data input |
| 24 | OSCIN | Input | System clock input |
| 25 | VD_IN | Input | IRIS video sync signal input |
| 26 | DVDD | Power supply | 3 V digital power supply |
| 27 | MONI_1 | Output | Monitor output 1 |
| 28 | GNDD | Ground | Digital GND |
| 29 | MONI_2 | Output | Monitor output 2 |
| 30 | RST | Input | Reset signal input |
| 31 | ENABLE | Input | Enable signal input |
| 36 | CLK_SW | Input | System clock frequency select |
| 37 | TEST | Input | Test mode input |
| 38 | AMP2REF | — | Reference voltage for CDS signal amplifier |
| 39 | GNDA | Ground | 3 V analog GND |
| 40 | AMP2INP | Input | CDS signal input |
| 41 | AMP2OUT | Output | CDS signal amplifier output |
| 42 | BUF_OUT | Output | PWM signal output |
| 43 | PWM_IN | Input | PWM signal input |

Notes) Concerning detail about pin description, please refer to OPERATION and APPLICATION INFORMATION section.

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## FUNCTIONAL BLOCK DIAGRAM
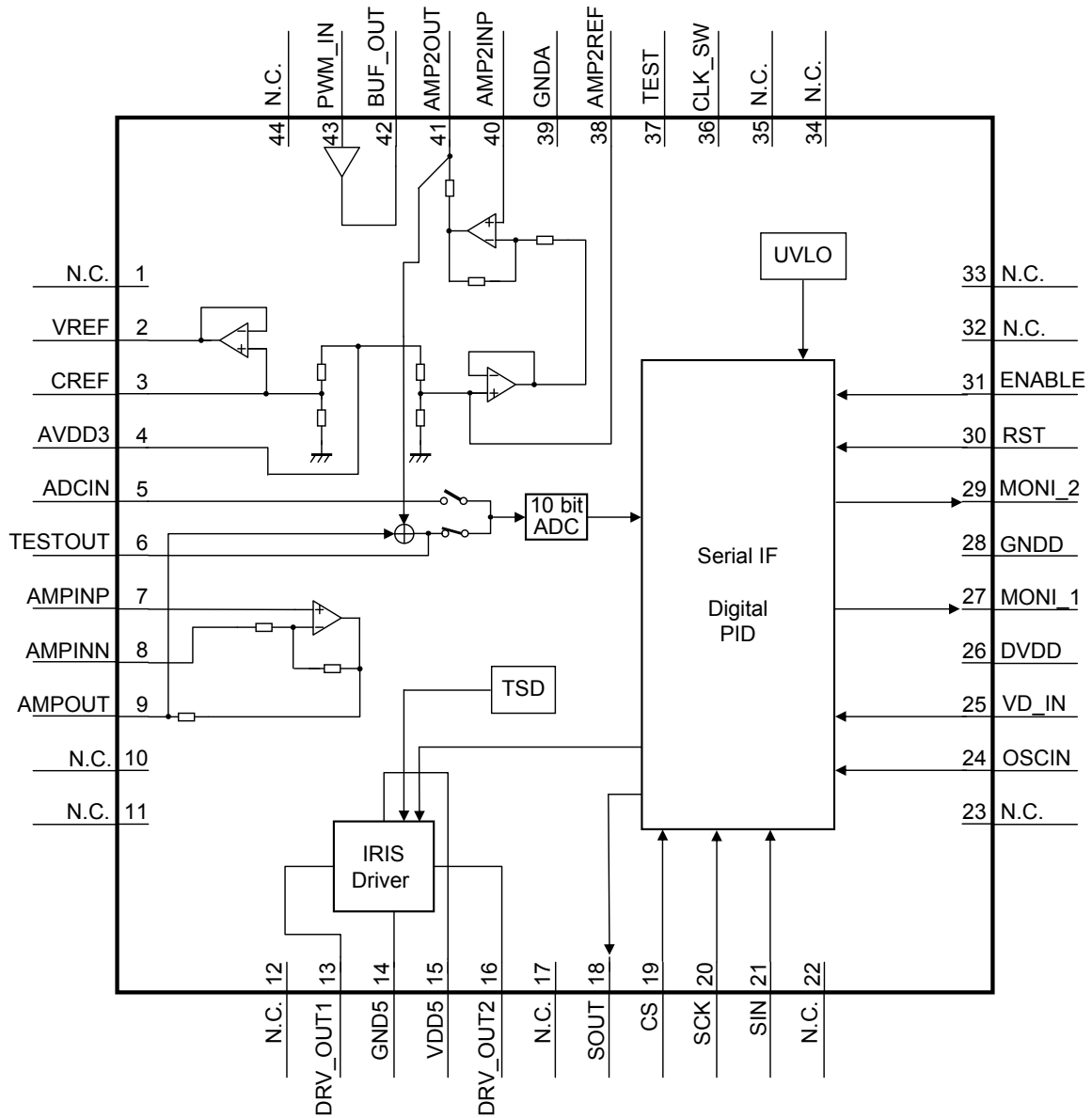


Note) This block diagram is for explaining functions. Part of the block diagram may be omitted, or it may be simplified.
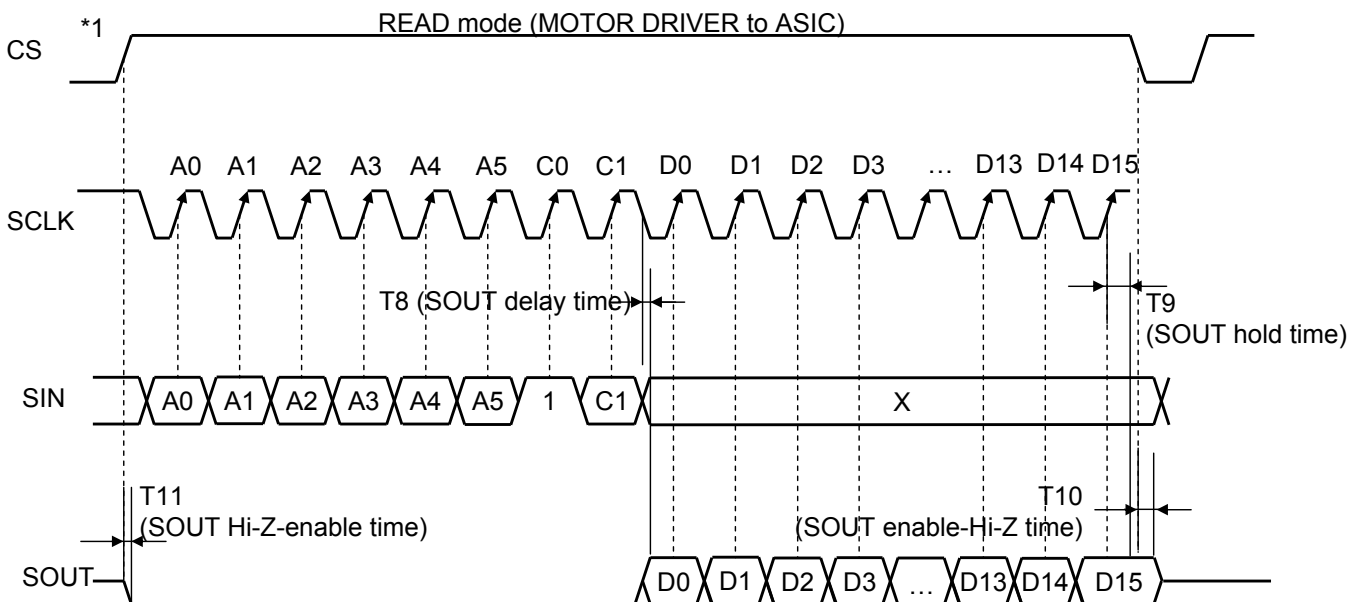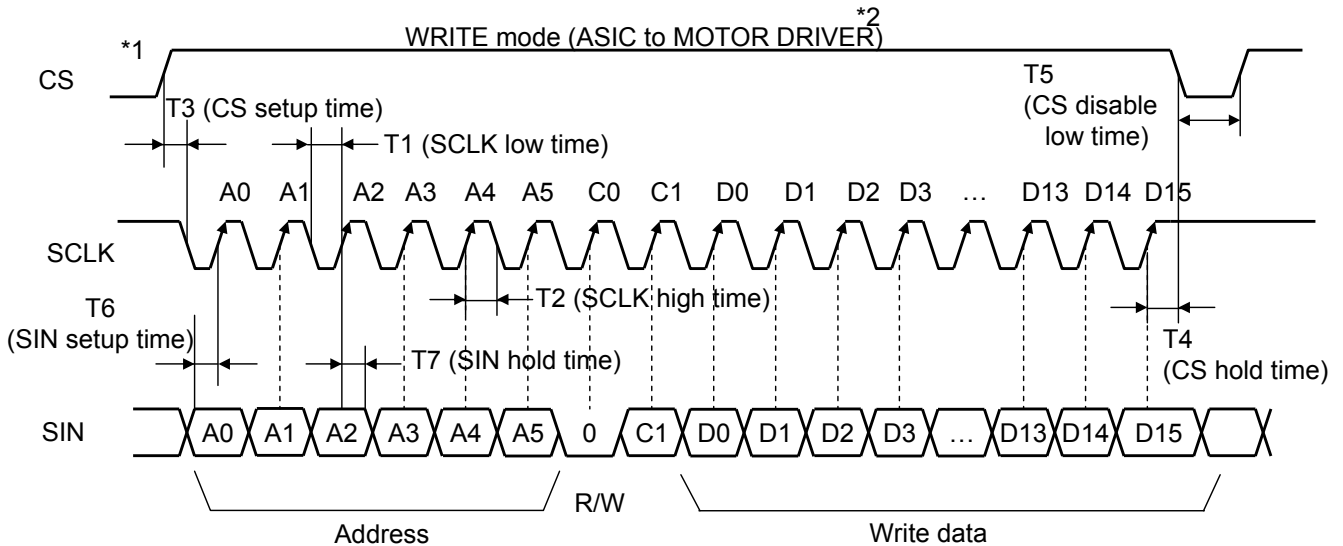
## OPERATION

### 1. Control mode

1) Read / Write of serial data

Note)The characteristics listed below are reference values derived from the design of the LSI and are not guaranteed.

Register input / output signal specification



WRITE mode (ASIC to MOTOR DRIVER)[*2]



READ mode (MOTOR DRIVER to ASIC)

Notes) *1 :CS default value of each cycle (Write / Read mode) starts from Low-level.
    *2 :It is necessary to input the system clock OSCIN in write mode.

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## OPERATION(continued)

**1. Control mode(continued)**

2) Register table

Register table

| Address | Register name | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 00h | Luminance Target | — | — | — | — | — | — | Y_TGT[9:0] | | | | | | | | | |
| 01h | Target Update Timing | Y_PWM_POL | Y_PWM_ON | CDS_AMP_OFF | Reserved | — | — | — | — | TGT_UPDATE[7:0] | | | | | | | |
| 02h | PID Filter(1) | — | — | — | TGT_FLT_OFF | TGT_LPF_FC[3:0] | | | | — | — | DEC_AVE | AVE_SPEED[4:0] | | | | |
| 03h | PID(1) | PID_INV | — | — | LMT_ENB | ARW[3:0] | | | | — | DGAIN[6:0] | | | | | | |
| 04h | PID(2) | PID_POLE[3:0] | | | | PID_ZERO[3:0] | | | | IRIS_ROUND[3:0] | | | | IRIS_CALC_NR[3:0] | | | |
| 05h | PID Filter(2) | — | — | — | — | PWM_FIL_OFF | PWM_LPF_FC[2:0] | | | AS_FLT_OFF | ASOUND_LPF_FC[2:0] | | | OVER_LPF_FC_2ND[1:0] | | OVER_LPF_FC_1ST[1:0] | |
| 06h | Offset DAC | — | — | — | — | — | — | — | — | DAMP_OFFSET_DAC[7:0] | | | | | | | |
| 07h | Analog Adder | — | — | — | — | Y_MIX[3:0] | | | | — | — | — | — | DAMP_MIX[3:0] | | | |
| 08h | Analog LPF/Gain | Y_GAIN[3:0] | | | | DAMP_GAIN[3:0] | | | | — | — | Y_FLT[1:0] | | — | — | DAMP_FLT[1:0] | |
| 09h | PWM/Enable | TESTEN1 | — | DT_ADJ_IRIS[1:0] | | — | PWM_IRIS[2:0] | | | PID_CLIP[3:0] | | | | ASWMODE[1:0] | | VD_POL | ENABLE |
| 0Ah | ADC Read | — | — | — | — | — | — | IRSAD[9:0] read only | | | | | | | | | |
| 0Bh | Reserved | Panasonic Reserved | | | | | | | | | | | | | | | |
| 0Ch | Pulse Generator | — | — | — | — | — | — | START1[9:0] | | | | | | | | | |
| 0Dh | Pulse Generator | P1EN | — | — | — | WIDTH1[11:0] | | | | | | | | | | | |
| 0Eh | Pulse Generator | — | — | — | — | — | — | START2[9:0] | | | | | | | | | |
| 0Fh | Pulse Generator | P2EN | — | — | — | — | — | — | — | — | — | WIDTH2[5:0] | | | | | |
| 20h | Test mode selection | TESTEN2 | — | — | — | — | — | Panasonic Reserved | | — | — | — | — | PLS_SEL[3:0]* | | | |
| 21h | Test mode selection | — | — | — | — | — | DUTY_TEST | TGT_IN_TEST[9:0] | | | | | | | | | |
| 22h | Reserved | Panasonic Reserved | | | | | | | | | | | | | | | |
| 3Fh | Reserved | Panasonic Reserved | | | | | | | | | | | | | | | |

— : Usprohibited

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## OPERATION(continued)

**1.  Control mode(continued)**

3)  Register function table

| Address | Register name / Bit wide | Function |
|---|---|---|
| 00h | Y_TGT[9:0] | Luminance target |
| 01h | TGT_UPDATE[7:0] | Y_TGT  update delay time |
| | CDS_AMP_OFF | Luminance signal amplifier enable / disable |
| | Y_PWM_ON | PWM (luminance signal modulation) buffer enable / disable |
| | Y_PWM_POL | PWM_IN polarity selection |
| 02h | AVE_SPEED[3:0] | DEC_AVE time controller |
| | DEC_AVE | Moving average of Luminance target |
| | TGT_LPF_FC[3:0] | Luminance target value LPF cut-off frequency |
| | TGT_FLT_OFF | IRIS target value LPF function enable / disable |
| 03h | DGAIN[6:0] | PID controller digital gain |
| | ARW[3:0] | Number of bits in PID controller integrator |
| | LMT_ENB | PID controller integral stop |
| | PID_INV | PID controller polarity |
| 04h | IRIS_CALC_NR[3:0] | PID controller integral error cumulative prevention level |
| | IRIS_ROUND[3:0] | PID controller differential error cumulative prevention level |
| | PID_ZERO[3:0] | PID controller zero point |
| | PID_POLE[3:0] | PID controller pole |
| 05h | OVER_LPF_FC_1ST[1:0] | ADC feedback filter (1) cut-off frequency |
| | OVER_LPF_FC_2ND[1:0] | ADC feedback filter (2) cut-off frequency |
| | ASOUND_LPF_FC[2:0] | Filter cut-off frequency before PID controller |
| | AS_FLT_OFF | Filter before PID controller enable / disable |
| | PWM_LPF_FC[2:0] | LPF cut-off frequency after PID controller |
| | PWM_FLT_OFF | LPF after PID controller enable / disable |
| 06h | DAMP_OFFSET_DAC[7:0] | Offset adjustment for damping coil output amplifier |
| 07h | DAMP_MIX[3:0] | Damping coil signal mixed gain |
| | Y_MIX[3:0] | Luminance signal mixed gain |
| 08h | DAMP_FLT[1:0] | Damping coil signal LPF cut-off frequency |
| | Y_FLT[1:0] | Luminance signal LPF cut-off frequency |
| | DAMP_GAIN[3:0] | Damping coil signal amplifier gain |
| | Y_GAIN[3:0] | Luminance signal amplifier gain |

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## OPERATION(continued)

**1. Control mode(continued)**

3) Register function table(continued)

| Address | Register name / Bit wide | Function |
|---|---|---|
| 09h | ENABLE | Enable / Disable CTL |
| | VD_POL | VD_IN polarity selection |
| | ASWMODE[1:0] | ADCIN pin connection selection |
| | PID_CLIP[3:0] | PWM max-duty control |
| | PWM_IRIS[2:0] | PWM frequency of IRIS block output |
| | DT_ADJ_IRIS[1:0] | Dead time correction of IRIS block output |
| | TESTEN1 | Test mode enable 1 |
| 0Ah | IRSAD[9:0] | ADC output for IRIS (read only) |
| 0Ch | START1[9:0] | Pulse 1 start time |
| 0Dh | WIDTH1[11:0] | Pulse 1 width |
| | P1EN | Pulse 1 output enable |
| 0Eh | START2[9:0] | Pulse 2 start time |
| 0Fh | WIDTH2[5:0] | Pulse 2 width |
| | P2EN | Pulse 2 output enable |
| 20h | PLS_SEL[3:0]* | Monitor output selection |
| | TESTEN2 | Test mode enable 2 |
| 21h | DUTY_TEST | IRIS test mode 1 |
| | TGT_IN_TEST[9:0] | IRIS test mode 2 |

Please refer to a application note for details.

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## APPLICATIONS INFORMATION

### 1. Notes

1) Power-on and Supply voltage

When supplying to AVDD3 (Pin 4) ,VDD5  (Pin 15) , and DVDD  (Pin 26), or raising supply voltage for these pins, set the rising speed of supply  voltage to less than 0.05 V/μs. AVDD3, VDD5, and DVDD can be powered on in any sequence.
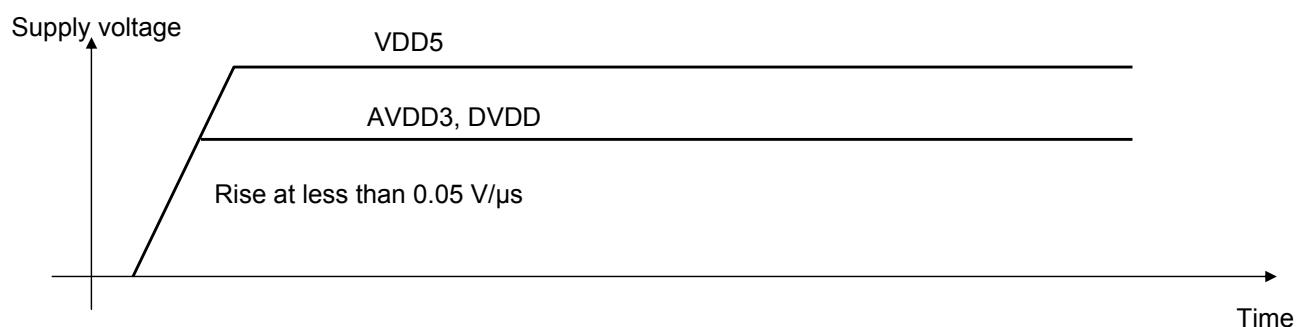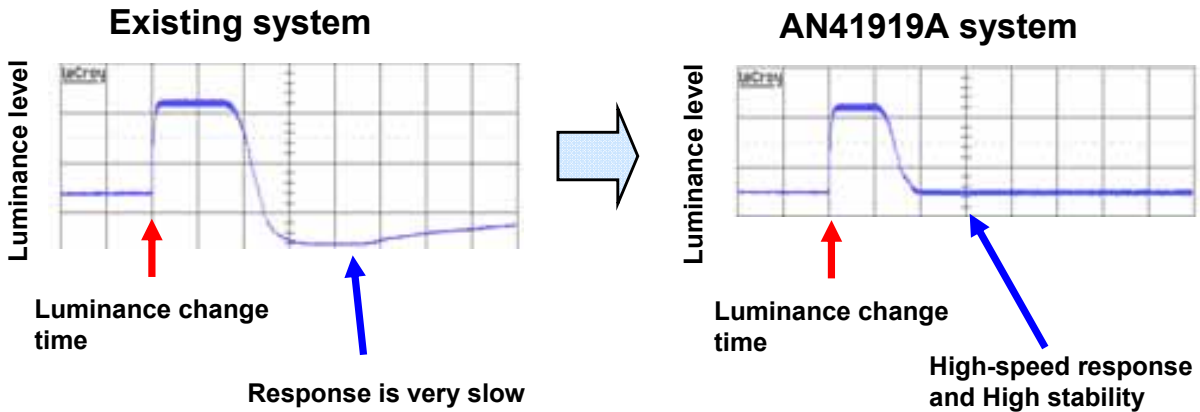


Connections to VREF and CREF
To VREF (Pin 2), do not connect other than recommended capacitor and damp coil.
To CREF (Pin 3), do not connect other than recommended capacitor.

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## TYPICAL CHARACTERISTICS CURVES

### 1,High-spped response of luminance change.

**Existing system**

**AN41919A system**

Luminance change time

Response is very slow

Luminance change time

High-speed response and High stability

### 2,Characteristic of supply voltage monitor.
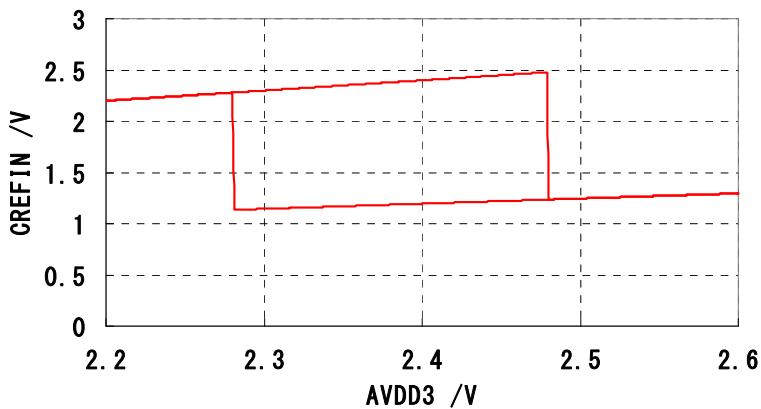
**(1) AVDD3**
 Operation voltage : 2.28V
 Return voltage : 2.48V
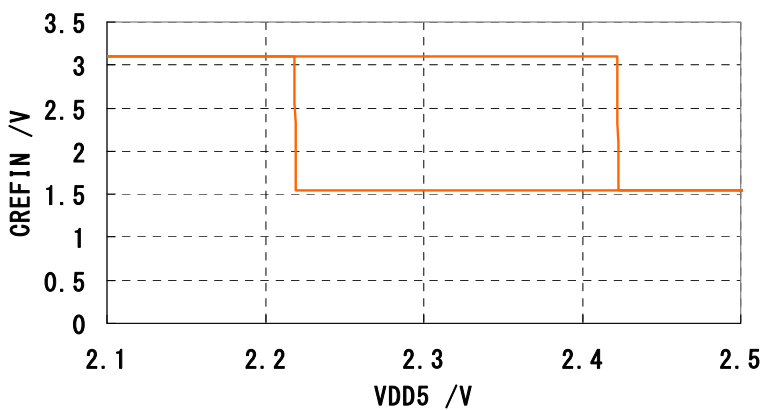
**(2) VDD5**
 Operation voltage : 2.22V
 Return voltage : 2.42V

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## PACKAGE INFORMATION ( Reference Data )

**Package Code:  *QFN044-P-0606D**

unit:mm
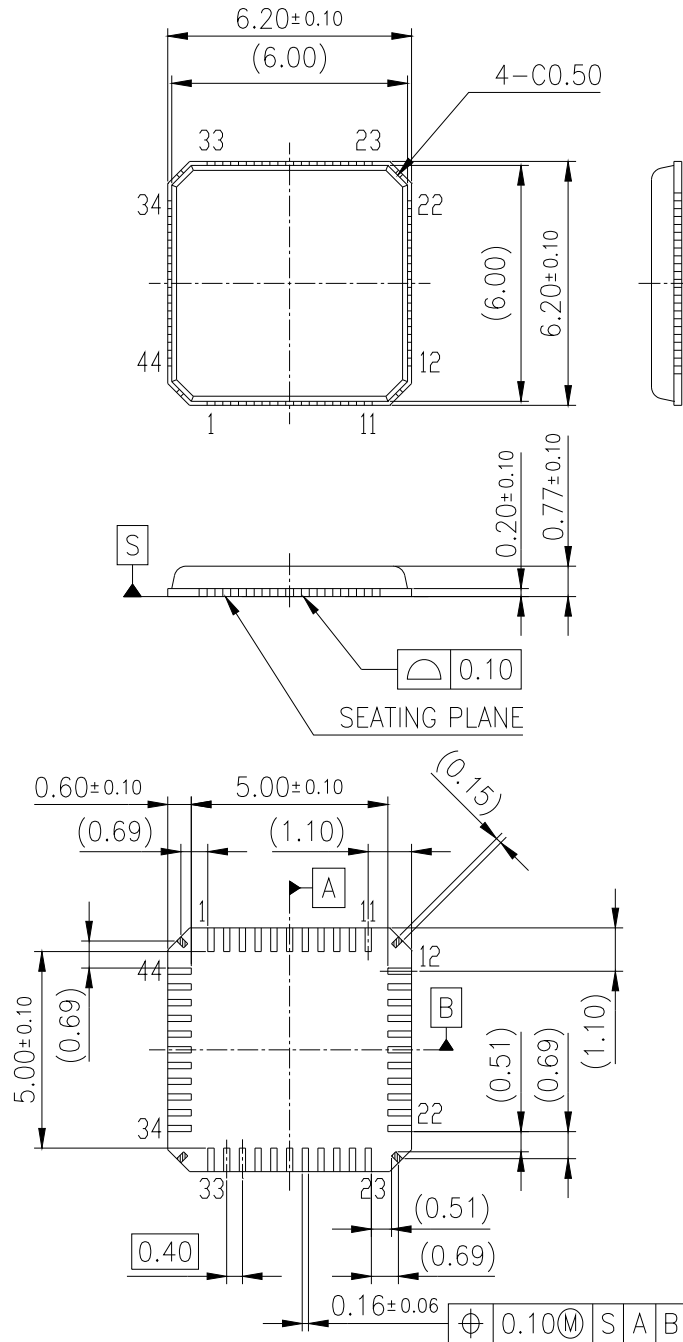


| Body Material | : | Br / Sb Free Epoxy Resin |
|---|---|---|
| Lead Material | : | Cu Alloy |
| Lead Finish Method | : | Pd Plating |

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(3) Medical equipment for life support

(4) Submarine transponder

(5) Control equipment for power plant

(6) Disaster prevention and security device

(7) Weapon

(8) Others : Applications of which reliability equivalent to (1) to (7) is required

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## USAGE NOTES

1. When designing your equipment, comply with the range of absolute maximum rating and the guaranteed operating conditions (operating power supply voltage and operating environment etc.). Especially, please be careful not to exceed the range of absolute maximum rating on the transient state, such as power-on, power-off and mode-switching. Otherwise, we will not be liable for any defect which may arise later in your equipment.

   Even when the products are used within the guaranteed values, take into the consideration of incidence of break down and failure mode, possible to occur to semiconductor products. Measures on the systems such as redundant design, arresting the spread of fire or preventing glitch are recommended in order to prevent physical injury, fire, social damages, for example, by using the products.

2. Comply with the instructions for use in order to prevent breakdown and characteristics change due to external factors (ESD, EOS, thermal stress and mechanical stress) at the time of handling, mounting or at customer's process. When using products for which damp-proof packing is required, satisfy the conditions, such as shelf life and the elapsed time since first opening the packages.

3. Pay attention to the direction of LSI. When mounting it in the wrong direction onto the PCB (printed-circuit-board), it might smoke or ignite.

4. Pay attention in the PCB (printed-circuit-board) pattern layout in order to prevent damage due to short circuit between pins. In addition, refer to the Pin Description for the pin configuration.

5. Perform a visual inspection on the PCB before applying power, otherwise damage might happen due to problems such as a solder-bridge between the pins of the semiconductor device. Also, perform a full technical verification on the assembly quality, because the same damage possibly can happen due to conductive substances, such as solder ball, that adhere to the LSI during transportation.

6. Take notice in the use of this product that it might break or occasionally smoke when an abnormal state occurs such as output pin-VCC short (Power supply fault), output pin-GND short (Ground fault), or output-to-output-pin short (load short) .

   And, safety measures such as an installation of fuses are recommended because the extent of the above-mentioned damage and smoke emission will depend on the current capability of the power supply.

7. The protection circuit is for maintaining safety against abnormal operation. Therefore, the protection circuit should not work during normal operation.

   Especially for the thermal protection circuit, if the area of safe operation or the absolute maximum rating is momentarily exceeded due to output pin to VCC short (Power supply fault), or output pin to GND short (Ground fault),  the LSI might be damaged before the thermal protection circuit could operate.

8. Unless specified in the product specifications, make sure that negative voltage or excessive voltage are not applied to the pins because the device might be damaged, which could happen due to negative voltage or excessive voltage generated during the ON and OFF timing when the inductive load of a motor coil or actuator coils of optical pick-up is being driven.

9. The product which has specified ASO (Area of Safe Operation) should be operated in ASO

10. Verify the risks which might be caused by the malfunctions of external components.

11. Apply voltage from a low-impedance to power supply pins and connect a bypass capacitor to the LSI as near as possible.

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