Panasonic

Doc No.

Doc Title

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DOCUMENT COVER PAGE

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Note: This cover page establishes the Doc No., Title and current status of the attached document.

SDSC-PSE-AN7135

Product Specifications for AN7135

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Issue Level	Rev	Eff Date				
1	5	23-FEB-06				
Total no. of pag	_					

(excluding this page)

Revision History

Issue	Rev	Eff Date	S/N	Page	Change Details	Remarks
1	4	15-FEB-04	1	-	Added this cover page.	
			2	6	Removed this page.	
	***************************************		3	6A	Added this page for leadfree specification.	
			4	6A	Amended Outer Lead Surface Process &	
					Chip Mounting Method.	
				-	Only Modified Modified	
	5	23-FEB-06	1	6A	Amended Outer Lead Surface process.	

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Product Specifications EXT

AN7135

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EXTERNAL ISSUE

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Structure	Silicon Monolithic Bipolar IC	
Appearance	FP12S Pin Plastic Package (with Fin)	
Application	Low Frequency Power Amplifier	
Function	7.5W(3Ω) x 2 Channel Power amplifier With Standby Function	

A	Absolute Maximum Ratings				
No.	Item	Symbol	Ratings	Unit	Note
1	Storage Temperature	Tstg	-55 ~ +150	°C	1
2	Operating Ambient Temperature	Topr	-30 ~ +75	°C	1
3	Operating Ambient Pressure	Popr	1.013x10 ⁵ ±0.61x10 ⁵	Pa	
4	Operating Constant Acceleration	Gopr	9,810	m/s²	
5	Operating Shock	Sopr	4,900	m/s²	
6	Supply Voltage	Vcc	24	V	
7	Supply Current	Icc	4.0	A	
8	Power Dissipation	P_{D}	62.5	W	2

1				
-	Operating Supply Voltage Range	Vcc	5V ~ 18V	Note 3

Note 1: The temperature of all item shall be Ta=25°C except storage temperature and operating ambient temperature.

Note 2: $R_{\theta j-c} = 2.0$ °C/W

Note 3: 24V during no signal.

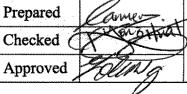
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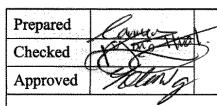
В	B Electrical Characteristics (Unless otherwise specified, the ambient temperature is 25°C ± 2°C)								
No.	Item	Symbol	Test Cir-	Conditions		Limits		TT 14	T
INU.	Item	Symbol	cuit		min	typ	max	Unit	Note
1	Quiescent Circuit Current	Icq	1	V _{IN} =0mV	-	14	20	mA	
2	Output Noise Voltage	Vno	1	V _{IN} =0mV, R _g =10kΩ	•	0.25	0.50	mV	1
3	Voltage Gain	Gv	1	V _{IN} =3mV	42.5	44.5	46.5	dB	
4	Total Harmonic Distortion	THD	1	V _{IN} =3mV		0.40	0.75	%	
5	Maximum Power Output	Po	1	THD=10%	7.0	7.5		W	
6	Channel Balance	СВ	1	V _{IN} =3mV	-1	0	+1	dВ	
7	Ripple Rejection	RR	1	Vcc(ripple) = 280 mV f(ripple) = 120 Hz Rg = 0Ω Sine wave	45	50	-	dB	1
8	Input Offset Voltage	Vin (o.s)	1	Input pin open	-	10	30	mV	
9	Standy-by current	Istb	1	Pin 3 open	-		30	μΑ	

< Vcc = 15.0V, RL = 3Ω , Freq = 1kHz, Driving 2 channel >

Note 1) Use filter 15Hz ~ 30kHz (12dB/OCT) when measurement.

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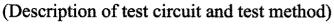
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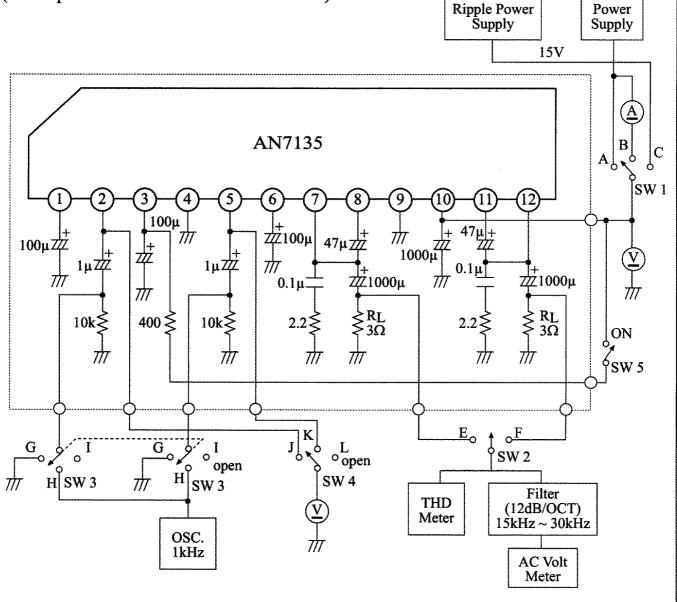


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ITEM	SW 1	SW 2	SW 3	SW 4	SW 5
B1	В	-	G	L	ON
B2	A	E or F	I	L	ON
B3	A	E or F	Н	L	ON
B4	A	E or F	H	L	ON
B5	A	E or F	H	L	ON
B 6	Α	E or F	H	L	ON
B 7	С	E or F	G	L	ON
B8	A	_	I	J or K	ON
B 9	A	-	I	-	OFF

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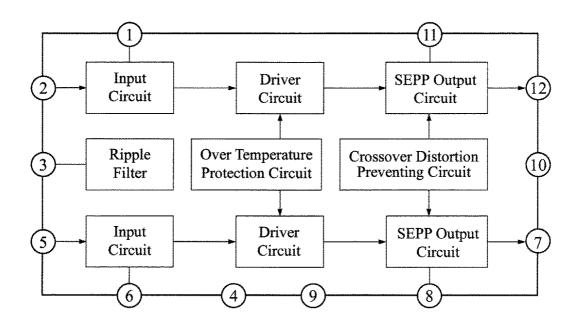
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Product Specifications

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Circuit Function Block Diagram



Pin Descriptions

Pin No.	Description	Pin No.	Description
1	Channel 1 negative feedback	7	Channel 2 output
2	Channel 1 input	8	Channel 2 bootstrap
3	Repple filter / Stand-by	9	GND (Output side)
4	GND (Input side)	10	Power supply
5	Channel 2 input	11	Channel 1 bootstrap
6	Channel 2 negative feedback	12	Channel 1 output

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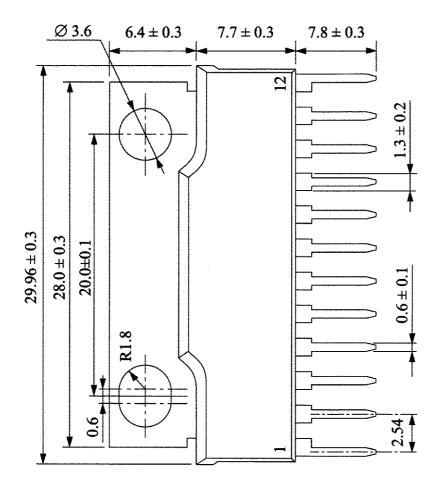
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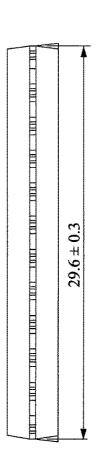
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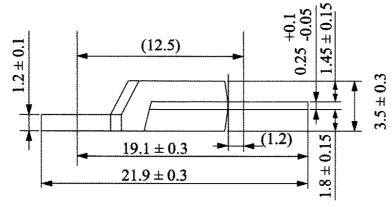
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Package Name | FP 12S

Unit: mm







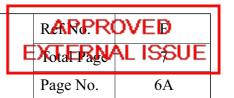
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Prepared	Yiap Shi Hui		
Checked	John Ng		
Approved	T. Sugimura		

Product Specifications (Leadfree)

AN7135



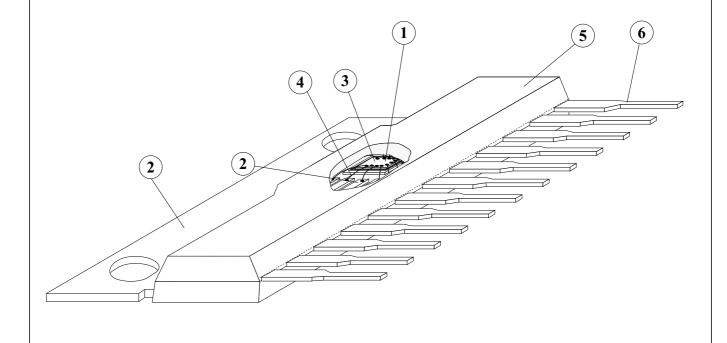
(Structure Description)

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Chip surface passivation	SiN,	PSG,	Others ()	1
Lead frame material	Fe group,	Cu group,	Others ()	2,6
Inner lead surface process	Ag plating,	Au plating,	Others ()	2
Outer lead surface process	General Custome SC Buyback:	er: Solder Plating (98Sn-2E Solder Dip (95.5Sn-2Ag			6
Chip mounting method	Ag paste,	Au-Si alloy, Solder	(95.5Pb-2.5Ag-2S	Sn)**,	3
Wire bonding method	Thermalsonic	bonding,	Others ()	4
Wire material	Au,		Others ()	4
Mold material	Epoxy,		Others ()	5
Molding method	Transfer mole	d, Multiplunger mold,	Others ()	5
Fin material	Cu group,		Others ()	7

Package FP12S

** Under RoHS exemption clause, Lead (Pb) in high melting temperature type solder (ie. tin-lead solder alloy containing more than 85% of lead), is exempted until 2010.



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Semiconductor Company, Matsushita Electric Industrial Co., Ltd

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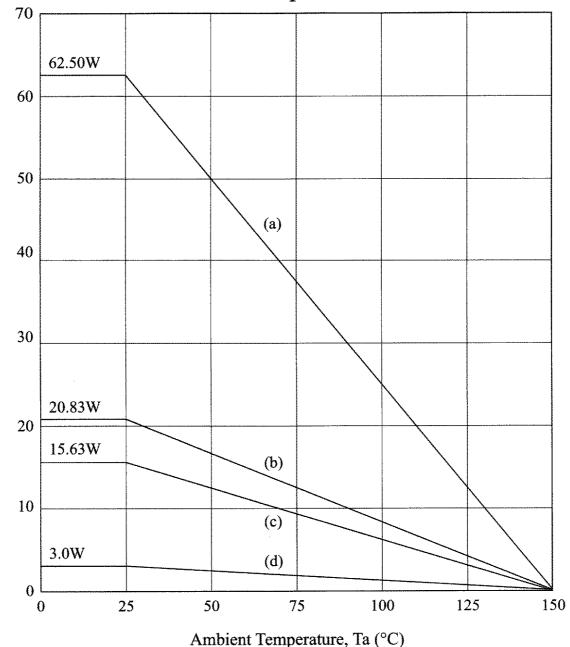
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(a) 62.50W Unlimited heatsink (θ j-c = 2°C/W)

- (b) 20.83W (θf=4.0°C/W)

 Heat sink of 100cm² x 3mm Al (black lacquer) or 200cm² x 2mm Al (without lacquer)
- (c) 15.63W ($\theta f=6.0^{\circ}C/W$) Heat sink of $100cm^2$ x 2mm Al (without lacquer)
- (d) 3.0W at Ta=30°C(θ j-a=40°C/W) No Heat sink

Power Dissipation PD -Ta



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Power Dissipation, PD (W)

单击下面可查看定价,库存,交付和生命周期等信息

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