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8	Maisus	nita Electric	Industrial Co	D., Lta.	
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Product Standards

Page 2

Total Pages

17

Contents

	3
■ Features	3
Applications	3
Package	3
■ Туре	3
Application Circuit Example	4
Block Diagram	5
Pin Descriptions	
Absolute Maximum Ratings	7
Operating Supply Voltage Range	7
Recommended Operating Conditions	7
Electrical Characteristics	8
Electrical Characteristics (Reference values for design)	9
■ Test Circuit Diagram	10
Electrical Characteristics Test Procedures	13
Technical Data	16
Usage Notes	17

2006-08-24		
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Product Standards

AN8015SH

AN8015SH

Single-channel step-down, step-up, or inverting use DC-DC converter control IC

Overview

AN8015SH is a single-channel DC-DC converter control IC using the PWM method.

This IC can provide any one output type from among step-down, step-up and inverting output.

Its operating supply voltage range is wide and its consumption current is small. In addition, since it uses the 10-pin surface

mounting type package with 0.5 mm pitch, it is suitable for highly efficient miniature potable power supply, especially for a negative output power supply.

Features

- Wide operating supply voltage range (3.6 V to 34 V)
- Small consumption current (1.8 mA typical)
- Converter control in a wide output frequency range is possible (2 kHz to 500 kHz).
- Built-in timer latch short-circuit protection circuit (charge current : 1.1 µA typical)
- Incorporating the under-voltage lock-out (U.V.L.O) circuit
- Incorporating a high precision reference voltage circuit (2.46 V (allowance: ±3%))
- Output block is open-collector (darlington) type.
- High absolute maximum rating of output current (100 mA)
- Maximum duty ratio is fixed and has small sample-to-sample variations (90% ±5%)

Applications

• LCD displays, digital still cameras, and PDAs

Package

• 10 pin Plastic Shrink Small Outline Package (SSOP Type)

■ Туре

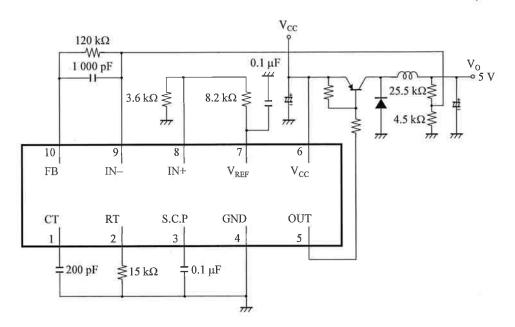
• Silicon Monolithic Bipolar IC

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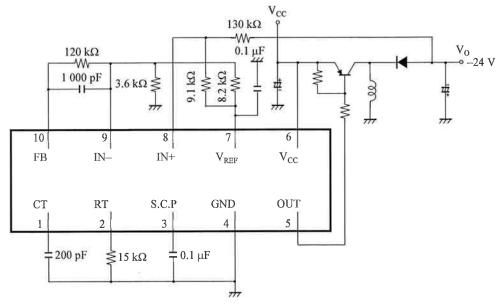
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		Total Pages	Page	
		17	4	

Application Circuit Example

1. Chopper method step-down type



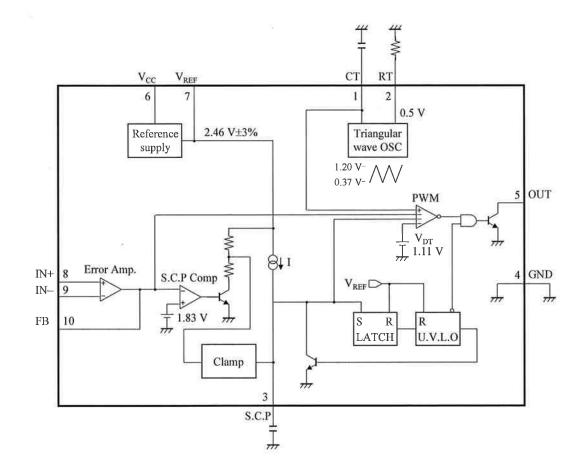
2. Chopper method inverting type



2006-08-24		
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	Product Standards	AN8015SH		
		Total Pages	Page	
		17	5	

Block Diagram



2006-08-24		
Established	Revised	
2108015005060	070	Semiconductor Company, Matsushita Electric Industrial Co., Ltd

	AN80	15SH
Product Standards	Total Pages	Page
	17	6

Pin Descriptions

Pin No.	Pin name	Туре	Description	
1	СТ		Pin for connecting oscillator timing capacitor	
2	RT		Pin for connecting oscillator timing resistor	
3	S.C.P		Pin for connection the time constant setting capacitor for short-circuit protection	
4	GND	Ground	Grounding pin	
5	OUT	Output	pen collector type output pin	
6	V _{cc}	Power supply	ower supply voltage application pin	
7	V _{REF}	Output	eference voltage output pin	
8	IN+	Input	Error amplifier non-inverted input pin	
9	IN-	Input	rror amplifier inverted input pin	
10	FB	Output	Output pin of error amplifier	

2006-08-24		
Established	Revised	
2108015006060)70	Semiconductor Company, Matsushita Electric Industrial Co., Ltd.

	AN8015SH	
Product Standards	Total Pages	Page
	17	7

Absolute Maximum Ratings

A No.	Parameter	Symbol	Rating	Unit	Notes
1	Supply voltage	V _{cc}	35	v	*1
2	Supply current	I _{cc}	<u>-4</u>	mA	
3	Power dissipation	P _D	115	mW	*2
4	Operating ambient temperature	T _{opr}	-30 to +85	°C	*3
5	Storage temperature	T _{stg}	-55 to +150	°C	*3
6	IN- pin allowable application voltage	V _{IN-}	-0.3 to V _{REF}	v	(<u>-</u>)
7	IN+ pin allowable application voltage	V _{IN+}	-0.3 to V _{REF}	v	
8	Output pin allowable application voltage	V _{OUT}	35	v	
9	Collector output current	I _{OUT}	100	mA	1

Notes) *1 : The values under the condition not exceeding the above absolute maximum ratings and the power dissipation.

*2: The power dissipation shown is the value at $T_a = 85^{\circ}C$ for the independent (unmounted) IC package.

When using this IC, refer to the P_D - T_a diagram of the package standard page 4 and use under the condition not exceeding the allowable value. *3 : Except for the power dissipation, operating ambient temperature, and storage temperature, all ratings are for $T_a = 25^{\circ}$ C.

Operating supply voltage range

Parameter	Symbol	Range	Unit	Notes
Supply voltage range	V _{cc}	3.6 to 34	V	*

Note) *: The values under the condition not exceeding the above absolute maximum ratings and the power dissipation.

Recommended Operating Conditions

Parameter	Symbol	Min	Max	Unit	Notes
Error amplifier input voltage	V _{IN}	- 0.1	0.8	V	*
Collector output voltage	V _{OUT}		34	V	*
Collector output current	I _{OUT}	_	50	mÅ	*
Timing capacitance	CT	100	27 000	pF	*
Timing resistance	R _T	5.6	15	kΩ	*
Oscillation frequency	four	2	500	kHz	*
Reference voltage output current	I _{REF}	-3	0	mA	*
Time constant setting capacitance for soft start short-circuit protection	C _{SCP}	1 000	-	pF	*

Note) *: Do not apply current or voltage from external source to any pin not listed above.

In the circuit current, (+) means the current flowing into IC and (-) means the current flowing out of IC.

2006-08-24		
Established	Revised	
210801500706070		Semiconductor Company, Matsushita Electric Industrial Co.,

2.		AN80	15SH
	Product Standards	Total Pages	Page
		17	8

Electrical Characteristics at $V_{CC} = 12 \text{ V}$, $R_T = 15 \text{ k}\Omega$, $C_T = 200 \text{ pF}$ Note) $T_a = 25^{\circ}\text{C}\pm2^{\circ}\text{C}$ unless otherwise specified.

в	Deservator	Cumhal	Test	Conditions		Limits		Unit	Notes
No.	Parameter	Symbol	circuits	Conditions	Min	Тур	Max	Unit	
Refe	rence Voltage Block								
1	Reference voltage	V _{REF}	1	$I_{\text{REF}} = -1 \text{ mA}$	2.386	2.46	2.534	V	
2	Input regulation with input fluctuation	Line	1	$V_{CC} = 3.6 \text{ to } 34 \text{ V}$ $I_{REF} = -1 \text{ mA}$	-	5	20	mV	
3	Load regulation	Load	1	$I_{REF} = -0.1 \text{ to } -1 \text{ mA}$		2	10	mV	
U.V.	L.O. Block				10				
4	Circuit operation start voltage	V _{UON}	2	-	2.8	3.1	3.4	V	
5	Hysteresis width	V _{HYS}	2		100	200	300	mV	
Erro	r Amplifier Block								
6	Input offset voltage	V _{IO}	3	_	-6	0	6	mV	
7	Input bias current	IB	3	—	-500	-25		nA	
8	Common-mode input voltage range	V _{ICR}	3	—	- 0.1		0.8	V	
9	High-level output voltage	V _{EH}	4	-	V _{REF} - 0.3	$V_{\text{REF}} - 0.1$	-	v	
10	Low-level output voltage	V _{EL}	4		-	0.1	0.3	V	
Outp	out Block								
11	Oscillation frequency	four	5	$R_{\rm T} = 15 \text{ k}\Omega, C_{\rm T} = 200 \text{ pF}$	175	195	215	kHz	
12	Maximum duty ratio	D _{MAX}	5	$R_{T} = 15 \text{ k}\Omega, C_{T} = 200 \text{ pF}$	85	90	95	%	
13	Output saturation voltage	V _{OL}	5	$I_0 = 50 \text{ mA}, R_T = 15 \text{ k}\Omega$		0.9	1.2	V	
14	Output leak current	I _{leak}	5	$V_{CC} = 34$ V, when output transistor is off			10	μĀ	
Shoi	t-circuit Protection Circuit Block								
15	Input threshold voltage	V _{THPC}	6		1.73	1.83	1.93	V	
16	Input standby voltage	V _{STBY}	6		1.15	1.25	1.35	V	
17	Input latch voltage	V _{IN}	6	-	5 -5	30	120	mV	
18	Charge current	I _{CHG}	6	$V_{SCP} = 0 V$	-1.32	-1.1	- 0.88	μA	
Who	le Device								
19	Total consumption current	I _{cc}	1	$R_T = 15 k\Omega$		1.8	2.8	mA	

2006-08-24		
Established	Revised	
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	Product Standards	AN8015SH	
Prod		Total Pages	Page
		17	9

Electrical Characteristics (Reference values for design) at $V_{CC} = 12 \text{ V}$, $R_T = 15 \text{ k}\Omega$, $C_T = 200 \text{ pF}$

Note) $T_a = 25^{\circ}C \pm 2^{\circ}C$ unless otherwise specified.

в	Demoster	Ormhal	Test	Quaditions	Refe	rence v	alues	Unit	Notes
No.	Parameter	Symbol circuits		Conditions	Min	Тур	Max	Unit	Notes
Refe	rence Voltage Block			10			ŝ		
20	Input regulation with input fluctuation 2	L _{INE2}	1	$V_{CC} = 3.6 V \text{ to } 20 V$	-	10 (max)		mV	*1
21	Output voltage temperature characteristics 1	V_{TC1}	I	Ta = -30 to 25°C	—	±0.5		%	*1
22	Output voltage temperature characteristics 2	V _{TC2}	1	$Ta = 25 to 85^{\circ}C$		±0.5		%	*1
23	Reference short-circuit current	I _{RS}	1			-20	-	mA	*1
Erro	r Amplifier Block				12				
24	Output sink current	I _{SINK}	4	$V_{FB} = 0.8 V$		8	-	mA	*1
25	Output source current	I _{SOURCE}	4	$V_{FB} = 0.8 V$	-	-120		μA	*1
26	Open-loop gain	Av	4		-	70	-	dB	*1
27	Common-mode ripple rejection ratio	CMRR	3			50	2000	dB	*1
Outp	out Block								
28	RT pin voltage	V _{RT}	5		-	0.5	-	V	*1
29	Maximum oscillation frequency	f _{OUT(MAX)}	5	$R_T = 5.6 \text{ k}\Omega, C_T = 150 \text{ pF}$		500	-	kHz	*1
30	Frequency supply voltage characteristics	f_{dV}	5	$f_{OUT} = 200 \text{ kHz},$ V _{CC} = 3.6 V to 34 V		±2		%	*1
31	Frequency temperature characteristics 1	f _{dT} 1	5	$f_{OUT} = 200 \text{ kHz},$ $Ta = -30 \text{ to } 25^{\circ}\text{C}$	-	±3		%	*1
32	Frequency temperature characteristics 2	f _{dT} 2	5	$f_{OUT} = 200 \text{ kHz}$, Ta = 25 to 85°C	-	±3	-	%	*1
Shor	t-circuit Protection Circuit Block								
33	Comparator threshold voltage	V _{THL}	6	-		1.83	_	V	*1
Who	le Device								
34	Total consumption current 2	I _{cc} 2	1	$R_{\rm T} = 5.6 \text{ k}\Omega, C_{\rm T} = 150 \text{ pF}$	-	2.5	-	mA	*1

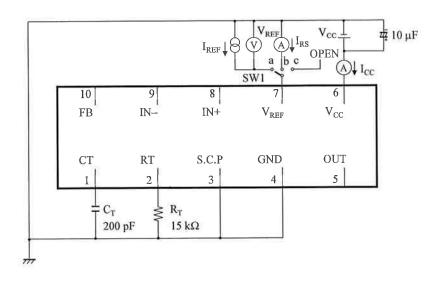
Note) *1: The above characteristics are reference values for design of the IC and are not guaranteed by inspection. If a problem does occur related to these characteristics, Matsushita will respond in good faith to user concerns,

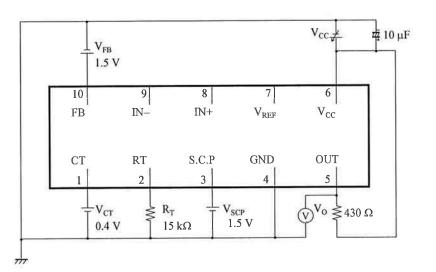
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Product Standards	Total Pages	Page
	17	10

Test Circuit Diagram

1. Test Circuit 1



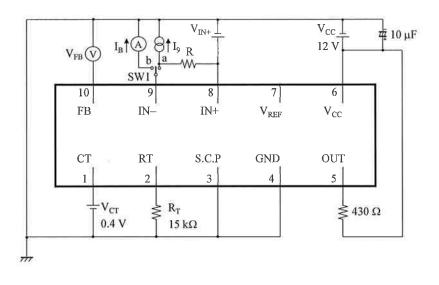


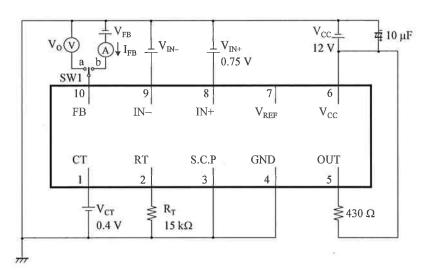
2006-08-24		
Established	Revised	
2108015010060	70	Semiconductor Company, Matsushita Electric Industrial Co., Ltd.

	Product Standards	AN8015SH	
		Total Pages	Page
		17	11

Test Circuit Diagram (continued)

3. Test Circuit 3



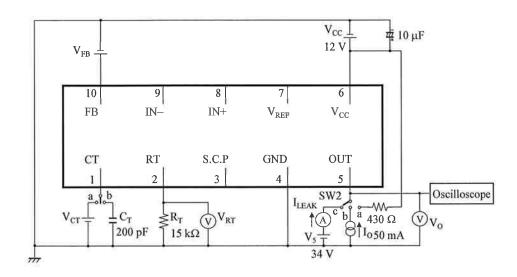


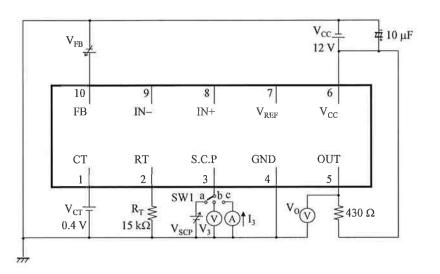
2006-08-24		
Established	Revised	
2108015011060	70	Semiconductor Company, Matsushita Electric Industrial Co., Ltd.

	AN8015SH	
Product Standards	Total Pages	Page
	17	12

Test Circuit Diagram (continued)

5. Test Circuit 5





2006-08-24		
Established	Revised	
2108015012060	070	Semiconductor Company, Matsushita Electric Industrial Co., Ltd.

	Product Standards	AN8015SH	
		Total Pages	Page
		17	13

Electrical Characteristics Test Procedures

1. Test Circuit1

C No.	Parameter	Conditions	Measuring Method
1	Reference voltage	$SW1 = a, V_{CC} = 12 V, I_{REF} = -1 mA$	Measure the voltage of V _{REF} .
2	Input regulation with input fluctuation	SW1 = a, V_{CC} = 3.6 V \rightarrow 34 V, I _{REF} = 0 A	Check the regulation of V _{REF} .
3	Load regulation	SW1 = a, V_{CC} = 12 V, I _{REF} = $-0.1 \text{ mA} \rightarrow -1 \text{ mA}$	Check the regulation of V _{REF} .
19	Total consumption current	SW1 = c, V_{CC} = 12 V, RT = 15 k Ω	Measure the current of I _{CC} .
23	Reference short-circuit current	SW1 = b, $V_{CC} = 12 V$	Measure the current of I _{RS} .

2. Test Circuit2

C No.	Parameter	Conditions	Measuring Method
4	Circuit operation start voltage	$V_{CT} = 0.4 \text{ V}, V_{SCP} = 1.5 \text{ V}, V_{FB} = 1.5 \text{ V}$	Measure the V_{CC} voltage when the V_0 changes from High to Low level while increasing the V_{CC} voltage gradually.
5	Hysteresis width	$V_{CT} = 0.4 \text{ V}, V_{SCP} = 1.5 \text{ V}, V_{FB} = 1.5 \text{ V}$	V_{O} $V_{HYS} = V_{UON} - V_{UOFF}$

C No.	Parameter	Conditions	Measuring Method
6	Input offset voltage	SW1 = a, V_{CC} = 12 V, V_{IN+} = 0.75 V, V_{CT} = 0.4 V	Measure the I_9 current when the V_{FB} changes while increasing the I_9 current gradually, calculate V_{IO} = R \times I_9 .
8	Common-mode input voltage range	SW1 = a, V_{CC} = 12 V, V_{CT} = 0.4 V	Check the V_{FB} voltage when $V_{IN+} = -0.1$ V or 0.8 V, while changes the I ₉ current gradually.
27	Common-mode ripple rejection ratio	SW1 = a, V_{CC} = 12 V, V_{CT} = 0.4 V	Measure the difference of ΔV_{IO} when $V_{IN+} = -0.1$ V or 0.8 V, and calculate from the following formula. CMRR = $20\log_{10} \frac{0.9}{\Delta V_{IO}}$
7	Input bias current	SW1 = b, V_{CC} = 12 V, V_{IN+} = 0.75 V, V_{CT} = 0.4 V	Measure the current of I _B .

2006-08-24		
Established	Revised	
2108015013060)70	Semiconductor Company, Matsushita Electric Industrial Co., Ltd.

	Product Standards	AN8015SH	
		Total Pages	Page
		17	14

Electrical Characteristics Test Procedures (continued)

4. Test Circuit4

C No.	Parameter	Conditions	Measuring Method
9	High-level output voltage	$\begin{split} & \text{SW1} = \text{a, V}_{\text{CC}} = 12 \text{ V, V}_{\text{CT}} = 0.4 \text{ V,} \\ & \text{V}_{\text{IN+}} = 0.75 \text{ V, V}_{\text{IN-}} = 0.7 \text{ V} \end{split}$	Measure the voltage of V ₀ .
10	Low-level output voltage	SW1 = a, $V_{CC} = 12$ V, $V_{CT} = 0.4$ V, $V_{IN+} = 0.75$ V, $V_{IN-} = 0.8$ V	Measure the voltage of V ₀ .
24	Output sink current	$\begin{split} & \text{SW1} = \text{b}, \text{V}_{\text{CC}} = 12 \text{V}, \text{V}_{\text{CT}} = 0.4 \text{V}, \\ & \text{V}_{\text{IN+}} = 0.75 \text{V}, \text{V}_{\text{IN-}} = 0.8 \text{V}, \text{V}_{\text{FB}} = 0.8 \text{V} \end{split}$	Measure the current of I_{FB} .
25	Output source current	$\begin{split} SW1 = b, V_{CC} &= 12 \ V, V_{CT} = 0.4 \ V, \\ V_{IN+} &= 0.75 \ V, V_{IN-} = 0.7 \ V, V_{FB} = 0.8 \ V \end{split}$	Measure the current of $I_{\rm FB}$.
26	Open-loop gain	SW1 = a, V_{CC} = 12 V, V_{CT} = 0.4 V	$A_{V} = 20 \log_{10} \frac{V_{EH} - V_{EL}}{\Delta V_{IN-}}$ V_{EH} V_{EL} V_{IN-} V_{IN-}

C No,	Parameter	Conditions	Measuring Method
11	Oscillation frequency	SW1 = b, SW2 = a, $V_{CC} = 12 V, V_{FB} = 1.5 V$	Oscilloscope waveform $f_{OUT} = -\frac{1}{T} Hz$
12	Maximum duty ratio	SW1 = b, SW2 = a, $V_{CC} = 12 \text{ V}, V_{FB} = 1.5 \text{ V}$	$D_{MAX} = \frac{t_{ON}}{T} \times 100 (\%)$ $C_{O} = \frac{1}{2} V$ $C_{O} = \frac{1}{T} \times 100 (\%)$ $C_{O} = \frac{1}{T} \times \frac{1}{T} + 1$
13	Output saturation voltage	SW1 = a, SW2 = b, $V_{CC} = 12 V$, $V_{FB} = 0.5 V$, $V_{CT} = 0.4 V$, $I_0 = 50 mA$	Measure the voltage of V_0 .
14	Output leak current	SW1 = a, SW2 = c, V_{CC} = 12 V, V _{FB} = 0.3 V, V_{CT} = 0.4 V, V_5 = 34 V	Measure the current of $I_{\rm LEAK}$.
28	RT pin voltage	SW1 = b, SW2 = a, $V_{CC} = 12 V, V_{FB} = 1.5 V$	Measure the voltage of V_{RT} .

2006-08-24		
Established	Revised	
2108015014060	070	Semiconductor Company, Matsushita Electric Industrial Co., Ltd

	AN8015SH		
Product Standards	Total Pages	Page	
	17	15	

Electrical Characteristics Test Procedures (continued)

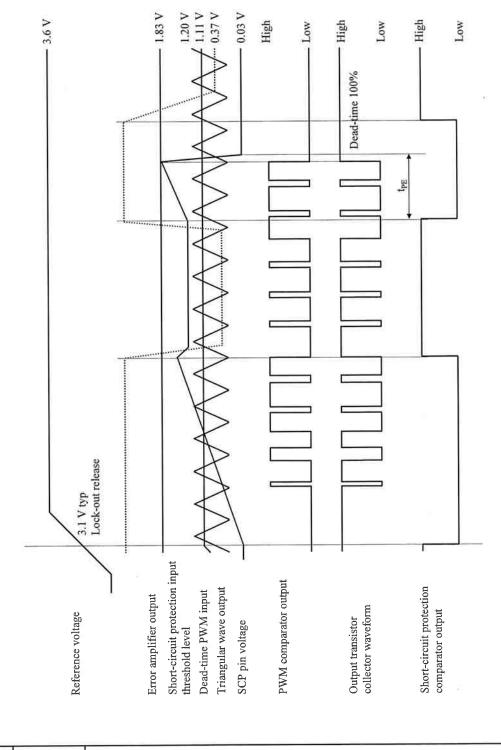
C No.	Parameter	Conditions	Measuring Method
15	Input threshold voltage	SW1 = a, $V_{CC} = 12 V$, $V_{CT} = 0.4 V$, $V_{FB} = 2.1 V$	Measure the V_{SCP} voltage when the V_0 changes from Low to High level while increasing the V_{SCP} voltage gradually.
16	Input standby voltage	$SW1 = b, V_{CC} = 12 V, V_{CT} = 0.4 V, V_{FB} = 1.5 V$	Measure the voltage of V_3 .
17	Input latch voltage	SW1 = b, V_{CC} = 12 V, V_{CT} = 0.4 V, V_{FB} = 2.1 V	Measure the voltage of V_3 .
18	Charge current	$SW1 = c, V_{CC} = 12 V, V_{CT} = 0.4 V, V_{FB} = 1.5 V$	Measure the current of I_3 .
33	Comparator threshold voltage	SW1 = b, $V_{CC} = 12$ V, $V_{CT} = 0.4$ V	Measure the V_{FB} voltage when the V_O changes from Low to High level while increasing the V_{FB} voltage gradually.

2006-08-24		
Established	Revised	
2108015015060	070	Semiconductor Company, Matsushita Electric Industrial Co., Ltd.

	AN8015SH		
Product Standards	Total Pages	Page	
	17	16	

Technical Data

Timing chart



2108015016060	070	Semiconductor Company, Matsushita Electric Industrial Co., Ltd.
Established	Revised	
2006-08-24		

	AN8015SH		
Product Standards	Total Pages	Page	
	17	17	

Usage Notes

This IC uses the constant current given by the timing resistor R_T as the bias current of the triangular oscillation block and the PWM comparator for consumption current reduction. The total consumption current is approximately 1.8 mA (typical) when R_T is 15 k Ω , and it increases to approximately 2.5 mA (typical) when R_T is 5.6 k Ω .

It is possible to use the circuit in the recommended operating range of 2 kHz to 500 kHz of the oscillation frequency. However, the timing resistor R_T versus the oscillation frequency should be set within the recommended range shown in figure 1. Also, refer to the figure 2, Timing capacitance-Oscillation frequency for setting the timing capacitance.

For a high frequency use, the overshoot and undershoot amounts increase due to operation delay of the triangular oscillation comparator, and the maximum duty ratio drops. This effect can be alleviated by speeding up through the reduction of the resistor R_{T} and increase in the circuit current.

Note that this IC can not be used as an IC for slave when the several ICs are operated in parallel synchronous mode.

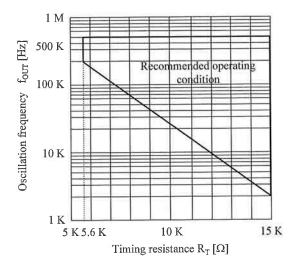


Figure 1. Timing resistance recommended condition

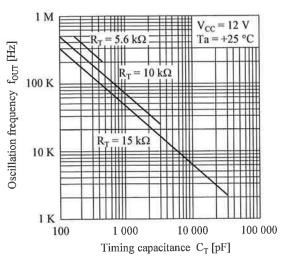


Figure 2. Timing capacitance-Oscillation frequency

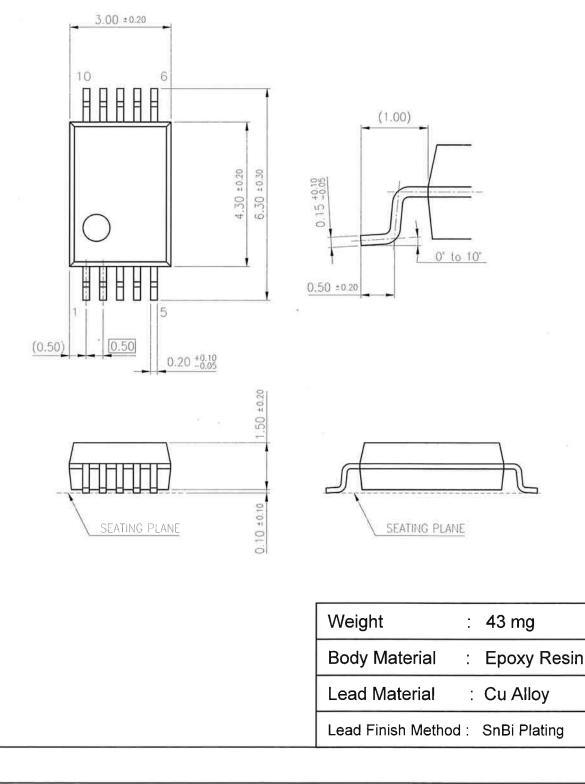
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PACKAGE STANDARDS
SSOP010-P-0225ATotal PagesPage62

1. Outline Drawing

Unit:mm

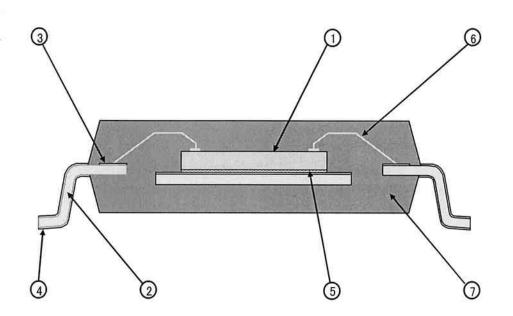


PACKAGE STANDARDS SSOP010-P-0225A

Total Pages	Page
6	3

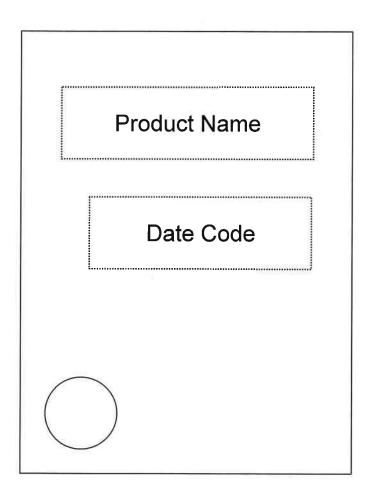
2. Package Structure (Technical Report)

Chip Material		Si	(1)	
Leadframe material		Cu alloy	2	
Inner lead surface		Ag plating	3	
Outer lead surface		SnBi plating	4	
Chip mount	Method	Resin adhesive method	- (5)	
ompmount	Material	Adhesive material		
Wirebond	Method	Thermo-compression bonding	_ 6	
WIREDOND	Material	Au		
Molding	Method	Multiplunger molding	0	
MOIGHIE	Material	Epoxy resin	$\neg \cup$	



PACKAGE STANDARDS		
SSOP010-P-0225A	Total Pages	Page
330F010-F-0223A	6	4

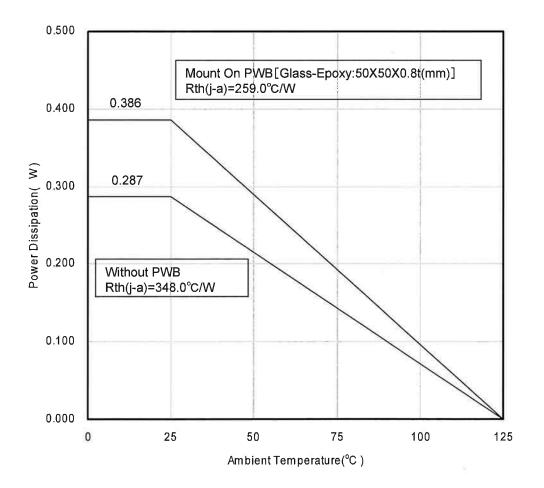
3. Mark Drawing



PACKAGE STANDARDS SSOP010-P-0225A

Total Pages	Page
6	5

4. Power Dissipation (Technical Report)



PACKAGE STANDARDS

SSOP010-P-0225A

Total Pages	Page
6	6

5. Power Dissipation (Supplementary Explanation)

[Experiment environment]

Power Dissipation (Technical Report) is a result in the experiment environment of SEMI standard conformity. (Ambient air temperature (Ta) is 25 degrees C)

[Supplementary information of PWB to be used for measurement]

The supplement of PWB information for Power Dissipation data (Technical Report) are shown below.

Indication	Total Layer	Resin Material
Glass-Epoxy	1-layer	FR-4
4-layer	4-layer	FR-4

[Notes about Power Dissipation (Thermal Resistance)]

Power Dissipation values (Thermal Resistance) depend on the conditions of the surroundings, such as specification of PWB and a mounting condition, and a ambient temperature. (Power Dissipation (Thermal Resistance) is not a fixed value.)

The Power Dissipation value (Technical Report) is the experiment result in specific conditions (evaluation environment of SEMI standard conformity) and keep in mind that Power Dissipation values (Thermal resistance) depend on circumference conditions and also change.

[Definition of each temperature and thermal resistance]

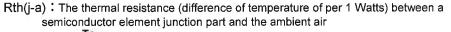
Ta : Ambient air temperature

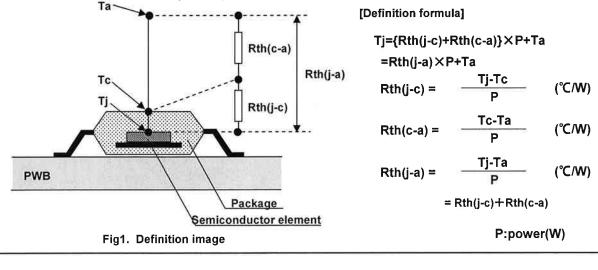
%The temperature of the air is defined at the position where the convection, radiation, etc. don't affect the temperature value, and it's separated from the heating elements.

- Tc : It's the temperature near the center of a package surface. The package surface is defined at the opposite side if the PWB.
- Tj : Semiconductor element surface temperature (Junction temperature.)

Rth(j-c) : The thermal resistance (difference of temperature of per 1 Watts) between a semiconductor element junction part and the package surface

Rth(c-a): The thermal resistance (difference of temperature of per 1 Watts) between the package surface and the ambient air





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