To: Digi-Key

Issue No. : ECJ05100301

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PRODUCT SPECIFICATION FOR APPROVAL

Product Description : Multilayer Ceramic Chip Capacitors

Product Part Number : ECJ3YF1C106Z (1206/F/16V/10uF)

Customers Part Number :

Country of Origin : Japan

Applications :

※If you approve this specification, please fill in and sign the below and return 1copy to us.

Approval No :

Approval Date :

Excecuted by :

(signature)

Title :

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If there is a question, please ask the engineering section about it directly.

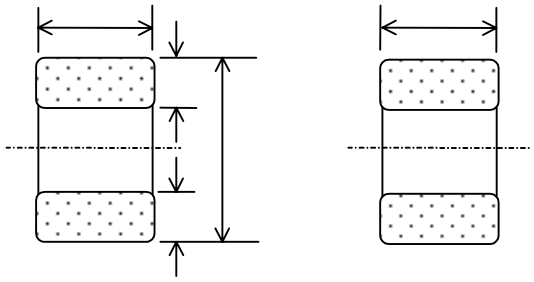
Panasonic

CLASSIFICATION	SPECIFICATIONS	No. 151S-ECJ-KAM46E
SUBJECT	Multilayer Ceramic Chip Capacitors 13type (EIA 1206) High Capacitance (P/N : ECJ3YF1C106Z) Individual Specification	PAGE 1 of 1 DATE 3 Oct, 2005

1. Scope

This specification applies to High Capacitance Multilayer Ceramic Chip Capacitor 13 type (EIA 1206), Temp. Char.: F, Rated voltage DC 16V , Nominal Capacitance 10 μF.

2. Style and Dimensions



3. Operating Temperature Range

Table 2

	Temperature Characteristics	Operating Temp. Range.
Class2	F	-30 to +85 °C

4. Individual Specification

Table 3

Part Number	Rated Voltage	Temp. Char.	Nominal Capacitance	Cap. Tolerance
ECJ3YF1C106Z	DC 16V	F	10 μF	+80 , -20 %

5. Explanation of Part Numbers

E C J 3 Y F 1 C 1 0 6 Z

E C J: Common Code

3: Size Code

Code	Size
3	13 type (EIA 1206)

Y: Packaging Style

Code	Packaging Style
Y	φ180Reel Embossed Taping 2000pcs./reel

F: Temp. Char. Code

1 C: Nominal Cap.

Z: Cap. Tolerance Code

6. Temperature Characteristics

Table 4

Temp. Char. Code	Capacitance Change rate from Temperature			Measurement Temperature Range	Reference Temperature
	Temp. Char.	Without voltage application	With 1/2 Rated voltage application		
F	F	+30 , -80%	+30 , -95%	- 25 to + 85 °C	+ 20 °C

7. Soldering method

Flow soldering shall not be applied.

Note ;

Panasonic Electronic Devices Co., Ltd.	APPROVAL	CHECK	DESIGN
	Y.Sakaguchi	S. Endoh	T.Shinriki

CLASSIFICATION	SPECIFICATIONS	No. 151S-ECJ-KGM46E
SUBJECT	Multilayer Ceramic Chip Capacitors 13type (EIA 1206) High Capacitance (P/N : ECJ3YF1C106Z) Common Specification	PAGE 1 of 7 DATE 3 Oct, 2005

1. Information

1- 1.Applicable laws and regulations

(1) Any ozone-depleting substances listed in the Montreal Protocol are not used in the manufacturing processes for parts and materials used in this product.

(2) PBB and PBDE are intentionally excluded from materials used in this product.

(3) All the materials used in this product are registered materials under the Law Concerning Examination and Regulation of Manufacture and Handling of Chemical Substances.

(4) This product complies with the RoHS, DIRECTIVE 2002/95/EC on the Restriction of the use of certain Hazardous Substances in electrical and electronic equipment.

(5) This product is exported with export procedures under export related laws and regulations such as the Foreign Exchange and Foreign Trade Law.

1- 2.Limitation in Applications

This product was designed and manufactured for general-purpose electronic equipment such as household, office, information & communication equipment. When the following applications, which are required higher reliability and safety because the trouble or malfunction of this product may threaten the lives and/or properties, are examined, separate specifications suitable for the application should be exchanged.

・Aerospace / Aircraft equipment, Warning / Antitheft equipment, Medical equipment, Transport equipment (Motor vehicles, Trains, Ship and Vessel), Highly public information processing equipment, Others equivalent to the above.

1- 3.Production factory

(1) Panasonic Electronic Devices Hokkaido Co., Ltd.

(2) Tianjin Matsushita Electronic Components Co., Ltd.(TMCOM)

(3) Matsushita Electronic Devices (M) Sdn. Bhd.(MEDEM)

2. Scope

2- 1.This specification applies to High Capacitance Multilayer Ceramic Chip Capacitor 13type (P/N : ECJ3YF1C106Z) . If there is a difference between this common specification and any individual specifications, priority shall be given to the individual specifications.

2- 2.This product shall be used for general-purpose electronic equipment such as audiovisual, household, office, information & communication equipment.

Unreasonable applications may accelerate performance deterioration or short/open circuits as failure modes affecting the life end.

Adequate safety shall be ensured especially for product design required a high level of safety with the following considerations.

1)Previously examine how a single trouble in this product affects the end product.

2)Design a protection circuit as Failsafe-design to avoid unsafe system resulting from a single trouble with this product.

Whenever a doubt about safety arises from this product, immediately inform us for technical consultation without fail, please.

2- 3.This specification is a part of contract documents pertaining to the trade made by and between your company and Matsushita Electric Industrial Co., Ltd.

3. Part Number Code

ECJ	3	Y	F	1C	106	Z
(1)	(2)	(3)	(4)	(5)	(6)	(7)

3- 1.Common Code (1)

ECJ : Multilayer Ceramic Chip Capacitors

3- 2.Size (2), Packaging Styles (3), Temperature Characteristic (4), Rated Voltage (5), Capacitance Tolerance (7) : Shown in Individual Specification.

Note ;

Panasonic Electronic Devices Co., Ltd.	APPROVAL	CHECK	DESIGN
	Y.Sakaguchi	S.Endoh	T.Shinriki

3- 3.Nominal Capacitance (6)

The Nominal Capacitance value is expressed in pico farads(pF) and is identified by a three-digit number ; the first two digit represent significant figures and the last digit specifies the number of zero to follow.

Symbol (Ex.)	Nominal Cap.
105	1000000pF(1μF)
106	10000000pF(10μF)
476	47000000pF(47μF)

4. Operating Temperature Range

Shown in Individual Specification.

5. Performance

The performance of the capacitor and its test condition shall be specified in Table 2.

5- 1.Pretreatment

Before test and measurements, the following pretreatment shall be applied when necessary.

5-1-1. Heat Treatment

The capacitors shall be kept in a temperature of 150+0/-10°C for 1 hour and then shall be stored in a room temperature for 48 +/- 4 hours, before initial measurement.

5-1-2. Voltage Treatment

D.C. voltage shall be applied for 1 hour in the specified test condition and then shall be stored in a room temperature for 48 +/- 4 hours, before initial measurement.

6. Test

Unless otherwise specified, all test and measurements shall be made at a temperature of 15 to 35°C and at a relative humidity of 45 to 75%.

If results obtained are doubted a further test should be carried out at a temperature of 20±2℃ and a relative humidity of 60 to 70%.

7. Structure

The structure shall be in a monolithic form as shown in Fig. 1.

Fig. 1

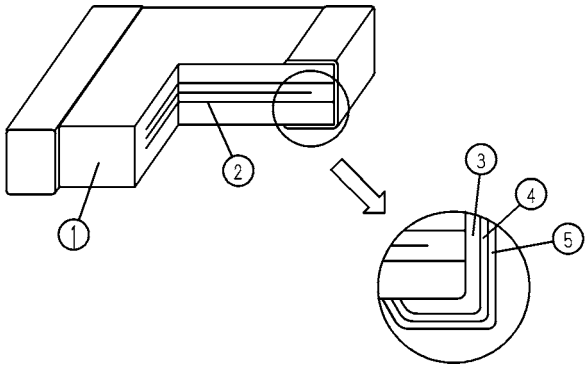


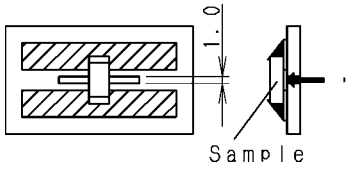
Table 1

No.	Name
①	Dielectric
②	Inner electrode
③	Substrate electrode
④	Intermediate electrode
⑤	External electrode

.

Note ;

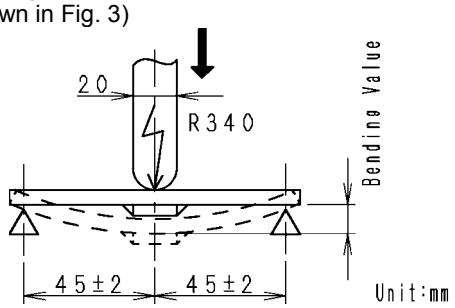
Table 2

No	Contents		Performance	Test Method
1	Appearance		There shall be no defects which affect the life and use.	With a magnifying glass (3 times).
2	Dimensions		Shown in Individual Specification.	With slide calipers and a micrometer.
3	Dielectric Withstanding voltage		There shall be no dielectric breakdown or damage.	Test voltage : 250% of rated voltage Apply a DC voltage of the above value for 1 to 5 seconds. Charge/discharge current shall be within 50mA.
4	Insulation Resistance(I.R.)		500/C MΩ min. (C : Nominal Cap. in μF)	Measuring voltage : Rated voltage Measuring voltage time : 60+/-5s Charge/discharge current shall be within 50mA.
5	Capacitance		Shall be within the specified tolerance.	Measuring Frequency : 1kHz+/-10% Measuring Voltage : 1.0+/-0.2Vrms For the class2 Capacitors, perform the heat treatment in par. 5-1-1. Our Measurement instrument is shown in the Table 3.
6	Dissipation Factor (tan δ)		0.125 max.	
7	Temperature Coefficient	Without Voltage Application	Temp. Char. F : Within +30,-80%	Measure the capacitance at each stage by changing the temperature in the order of step 1 to 4 shown in the table below. Calculate the rate of change regarding the capacitance at stage 3 as the reference. (Unit : °C) Temp. Char. / Stage 1: F: 20+/-2; 2: -25+/-3; 3: 20+/-2; 4: 85+/-2; 5: 20+/-2 For the test with voltage applied, apply a DC voltage which is 50% of the rated voltage immediacy after stage 5 of the test with no voltage application, and take the measurement in the order of steps 5, 2, 3 and 4. Determine the rate of change from the capacitance at stage 3 of the test with no voltage application.
		With Voltage Application	Temp. Char. F : Within +30,-95%	
	Adhesion		The terminal electrode shall be free from peeling or signs of peeling.	Solder the specimen to the testing jig shown in the figure., and apply a 5N force in the arrow direction for 10 seconds.  Material : Alumina board (95% min.) or glass epoxy board. Thickness : 1.0mm min.

(continue)

Note ;

Table 2

No	Contents		Performance		Test Method
9	Bending Strength	Appearance	There shall be no cracks and other mechanical damage.		After soldering capacitor on the substrate 1mm of bending shall be applied for 5 seconds. Bending speed : 1mm/s (shown in Fig. 3) 
		Capacitance	Temp. Char.	Change from the value before test.	
			F	Within +/- 30%	
10	Vibration Proof	Appearance	There shall be no cracks and other mechanical damage.		Solder the specimen to the testing jig shown in Fig. 2. Apply a variable vibration of 1.5mm total amplitude in the 10 to 55 to10Hz vibration frequency range swept in 1 min. in 3 mutually perpendicular directions for 2 hours each, a total of 6 hours.
		Capacitance	Shall be within the specified tolerance.		
		tan δ	Shall meet the specified initial value.		
11	Resistance to Solder Heat	Appearance	There shall be no cracks and other mechanical damage.		Solder both method Preconditioning : Heat Temperature (See 5.1.1)/Class2 Solder temperature : 270+/-5°C Dipping period : 3+/-0.5s Preheat condition : Order / Temp.(°C) / Period(s) 1 / 80 to 100 / 300 to 360 2 / 150 to 200 / 300 to 360 Use solder H63A(JIS-Z-3282).For the flux, use rosin (JIS-K-5902) ethanol solution of a concentration of about 25% by weight. Use tweezers for the holder to dip the specimen. Recovery : 48+/-4 hours
		Capacitance	Temp. Char.	Change from the value before test.	
			F	Within +/- 20%	
		tan δ	Shall meet the specified initial value.		
		I.R.	Shall meet the specified initial value.		
		Withstand voltage	There shall be no dielectric breakdown or damage.		
12	Solderability		More than 95% of the soldered area of both terminal electrodes shall be covered with fresh solder.		Solder temperature : 230+/-5°C Dipping period : 4+/-1s Dip the specimen in solder so that both terminal electrodes are completely submerged. Use solder H63A(JIS-Z-3282). For the flux use rosin (JIS-K-5902) of ethanol solution of a concentration of about 25% by weight. Use tweezers for the holder to dip the specimen.

(continue)

Note ;

Table 2

<table>
<tr><th>No</th><th colspan="2">Contents</th><th colspan="2">Performance</th><th>Test Method</th></tr>
<tr><td rowspan="5">13</td><td rowspan="5">Temperature cycle</td><td>Appear-ance</td><td colspan="2">There shall be no cracks and other mechanical damage.</td><td rowspan="5">Solder the specimen to the testing jig shown in Fig. 2. Condition the specimen to each temperature from step 1 to 4 in this order for the period shown in the table below. Regarding this conditioning as one cycle, perform 5 cycles continuously.
<table><tr><th>Step</th><th>Temperature (°C)</th><th>Period (min.)</th></tr><tr><td>1</td><td>Minimum operation temperature +/- 3</td><td>30+/-3</td></tr><tr><td>2</td><td>Room temperature</td><td>3 max.</td></tr><tr><td>3</td><td>Maximum operation temperature +/-5</td><td>30+/-3</td></tr><tr><td>4</td><td>Room temperature</td><td>3 max.</td></tr></table>
For the class2 capacitors, perform the heat treatment in par. 5-1-1.
Before the measurement after test, the specimen shall be left to stand at room temperature for the following period :
48+/-4 h</td></tr>
<tr><td rowspan="2">Capaci-tance</td><td>Temp. Char.</td><td>Change from the value before test.</td></tr>
<tr><td>F</td><td>Within +/- 20%</td></tr>
<tr><td>tan δ</td><td colspan="2">Shall meet the specified initial value.</td></tr>
<tr><td>I.R.</td><td colspan="2">Shall meet the specified initial value.</td></tr>
<tr><td>With-stand voltage</td><td colspan="2">There shall be no dielectric breakdown or damage.</td></tr>
<tr><td rowspan="4">14</td><td rowspan="4">Moisture Resistance</td><td>Appear-ance</td><td colspan="2">There shall be no cracks and other mechanical damage.</td><td rowspan="4">For the class2 capacitors, perform the heat treatment in par. 5-1-1.
Solder the specimen to the testing jig shown in Fig. 2.

Test temperature : 40+/-2°C
Relative humidity : 90 to 95%
Test period : 500+24/0 h

Before the measurement after test, the specimen shall be left to stand at room temperature for the following period :
48+/-4 h</td></tr>
<tr><td rowspan="2">Capaci-tance</td><td>Temp. Char.</td><td>Change from the value before test.</td></tr>
<tr><td>F</td><td>Within +/- 30%</td></tr>
<tr><td>tan δ</td><td colspan="2">0.2 max.</td></tr>
<tr><td>I.R.</td><td colspan="2">50/C MΩ min.
(C : Nominal Cap. in μF)</td></tr>
<tr><td rowspan="5">15</td><td rowspan="5">Moisture Resistant Loading</td><td>Appear-ance</td><td colspan="2">There shall be no cracks and other Mechanical damage.</td><td rowspan="5">For the class2 capacitors, perform the heat treatment in par. 5-1-2.
Solder the specimen to the testing jig shown in Fig. 2.

Test temperature : 40+/-2°C
Relative humidity : 90 to 95%
Applied voltage : Rated voltage (DC Voltage)
Charge/discharge current : within 50mA.
Test period : 500+24/0 h

Before the measurement after test, the specimen shall be left to stand at room temperature for the following period :
48+/-4 h</td></tr>
<tr><td rowspan="2">Capaci-tance</td><td>Temp. Char.</td><td>Change from the value before test.</td></tr>
<tr><td>F</td><td>Within +/- 30%</td></tr>
<tr><td>tan δ</td><td colspan="2">0.2 max.</td></tr>
<tr><td>I.R.</td><td colspan="2">25/C MΩ min.
(C : Nominal Cap. in μF)</td></tr>
</table>

(continue)

Note ;

Table 2

No	Contents		Performance		Test Method
16	High Temperature Resistant Loading	Appearance	There shall be no cracks and other mechanical damage.		For the class2 capacitors, perform the voltage treatment in par. 5-1-2. Solder the specimen to the testing jig shown in Fig. 2. Test temperature : Max. Rated temp. +/-3°C Applied voltage : Rated voltage x 200 % (DC Voltage) Charge/discharge current : within 50mA. Test period : 1000+48/0 h Before the measurement after test, the specimen shall be left to stand at room temperature for the following period : 48+/-4 h
		Capacitance	Temp. Char.	Change from the value before test.	
			F	Within +/- 30%	
		tan δ	0.2 max.		
		I.R.	50/C MΩ min. (C : Nominal Cap. in μF)		

When uncertainty occurs in the weather resistance characteristic tests (temperature cycle, moisture resistance, moisture resistant loading, high temperature resistant loading), the same tests shall be performed for the capacitor itself.

Table 3

	Our Standard Measuring Instrument
Measuring Instrument	4278A 1kHz/1MHz Capacitance Meter (Agilent Technologies)
Measuring Mode	Parallel Mode
Recommended Measuring Jig	16034e Test Fixture (Agilent Technologies)

For High Cap Type, signal voltage may be unable to be applied to depending on conditions of measuring instruments. We would appreciate it if you would confirm whether High Cap Type is under the measurable environment or not by checking that the fixed signal voltage is applied or not. (For example, ALC function is ON, HPA is expanded.)

Note ;

Fig. 2 Testing jig

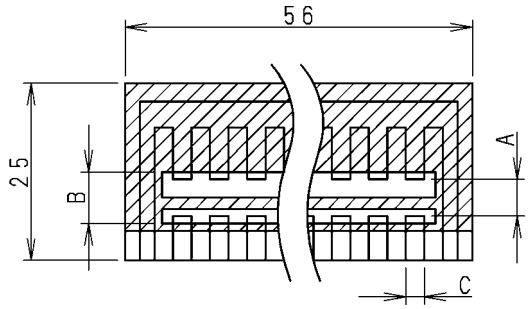


Table 4

Type (EIA)	A	B	C
13type (1206)	2.2	5.0	2.0

Unit : mm

Material : Glass epoxy board
Thickness : 1.6mm
:Copper foil (0.035mm thick)
:Solder resist

Fig. 3 Testing jig

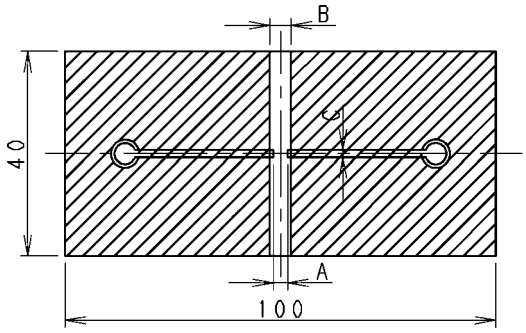


Table 5

Type (EIA)	A	B	C
13type (1206)	2.2	5.0	2.0

Unit : mm

Material : Glass epoxy board
Thickness : 1.6mm
:Copper foil (0.035mm thick)
:Solder resist

Note ;

1. Precautions for Use

The Multilayer Ceramic Chip Capacitors (hereafter referred to as “Capacitors”) may fail in a short circuit mode in an open-circuit mode when subjected to severe conditions of electrical, environmental and/or mechanical stress beyond the specified “Rating and specified “Conditions” in the Specifications, resulting in burn out, flaming or glowing in the worst case.

The following “Operating Conditions and Circuit Design” and “Precautions for Assembly” shall be taken in your major consideration.

If you have a question about the “Precautions for Use”, please contact our engineering section or factory.

2. Operating Conditions and Circuit Design

2- 1.Circuit Design

2-1-1. Operating Temperature Range

The specified “Operating Temperature Range” in the Specifications is absolute maximum and minimum temperature rating.

So in any case, each of the Capacitors shall be operated within the specified “Operating Temperature Range”.

2-1-2. Design of Voltage application

The Capacitors shall not be operated exceeding the specified “Rated Voltage” in the Specification.

If voltage ratings are exceeded, the Capacitors could result in failure or damage. In case of application of DC and AC voltages to the Capacitors, the designed peak voltage shall be within the specified “Rated Voltage”.

In case of AC of pulse voltage, the peak voltage shall be within the specified “Rated Voltage”. If high frequency voltage or fast rising pulse voltage is applied continuously even within the “Rated Voltage”, contact our engineering section before use. Such continuous application affects the life of the Capacitors.

2-1-3. Charging and Discharging Current

The Capacitors shall not be operated beyond the specified “Maximum Charging/Discharging Current Ratings” in the Specifications. Applications to a low impedance circuit such as a ”secondary power circuit” are not recommended for safety.

2-1-4. Temperature Rise by Dielectric Loss of the Capacitors

The “Operating Temperature Range” mentioned above shall include a maximum surface temperature rise of 20℃, which is caused by the Dielectric loss of the Capacitor and applied electrical stresses (such as voltage, frequency and wave form etc.). It is recommended to measure and check “Surface Temperature of the Capacitor” in your equipment at room temperature (up to 25℃).

2-1-5. Restriction on Environmental Conditions

The Capacitors shall not be operated and / or stored under the following environmental conditions.

(1) Environmental conditions
  (a) To be exposed directly to water or salt water
  (b) To be dew formation
  (c) Under conditions of corrosive gases such as hydrogen sulfide, sulfurous acid, chlorine and ammonia
(2) Under severe conditions of vibration or impact beyond the specified conditions in the Specifications

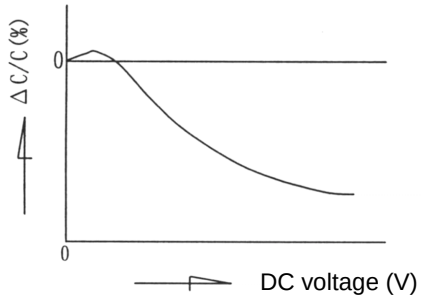
2-1-6. DC voltage characteristics

The Capacitors (Class 2) employ dielectric ceramics with dielectric constant having voltage dependency, and if applied DC voltage is high, capacitance may broadly change. For the specified capacitance, the following should be confirmed.

(1) If capacitance change by applied voltage is within the allowable range, or if its application allows unlimited capacitance change.
(2) DC voltage characteristics demonstrate, even if applied voltage is under the rated voltage, capacitance change rate increases with higher voltage (Capacitance down). Accordingly, when the Capacitors are used for circuits with narrow capacitance allowable range such as time constant circuits, we recommend to apply lower voltage upon due consideration on capacitance aging in addition to the above.

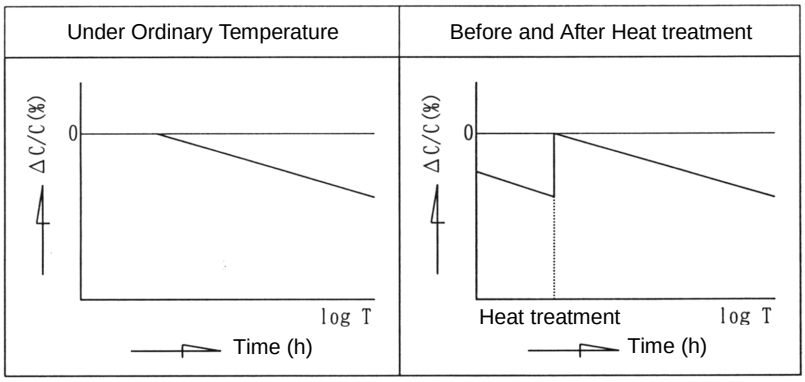
Note ;

Capacitance change vs. DC voltage



2-1-7. Capacitance aging

The ceramic dielectrics of the Capacitors (Class 2) have capacitance aging. Accordingly, when the Capacitors are used for the circuits, which require a narrow capacitance allowable range, such as time constant circuits, pay due consideration to capacitance aging for use.



2-1-8. Piezoelectricity

Dielectrics used for the Capacitors (Class 2) may cause the following Piezoelectricity (or Electrostriction).

(1) If the signal of a specific frequency is applied to the Capacitors, electric and acoustic noise may be generated by resonating the characteristic frequency which is determined by the dimensions of the Capacitor.
As a measure to prevent this phenomenon, changing the size of the Capacitor is effective to change its resonance frequency.
Also there is another measure changing the materials of the Capacitors to the Low-loss type, which has no (or less) piezoelectricity, or to Class1.
which has no (or less) piezoelectricity, or to Class1 is also available.

(2) Vibration or impact applied to the Capacitors may cause noise because mechanical force is converted to electrical signals (Especially, application to around the amplifier unit) .
As a measure to prevent this phenomenon, changing the materials of the Capacitor to the Low-loss type, which has no (or less) piezoelectricity, or to Class1 is also available.

(3) Even if a whining sound is generated, there is no problem in product performance and reliability, however, check the worrisome phenomenon which may generate noise in your equipment.
As a measure to prevent this phenomenon, changing to the Capacitor different in characteristics, size and shape as shown in the (1), (2) above is effective.
As the other measures, changing the mounting direction of the Capacitors to bring under control the resonance with equipment bodies such as printed circuit board, or the Capacitors are fixed with equipment bodies such as printed circuit board by adhesive may be effective.

2- 2.Design of Printed Circuit Board

2-2-1. Selection of Printed Circuit Board

When the Capacitors are mounted and soldered on an Aluminum Substrate, the substrate has influences on Capacitor's reliabilities against "Temperature Cycles" and "Heat shock" because of difference in thermal expansion coefficient between them.
It shall be carefully confirmed that the actual board applied does not deteriorate the characteristics of the Capacitors.

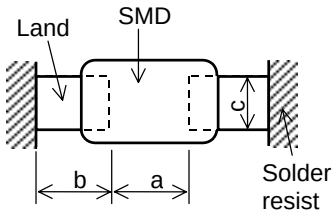
Note ;

2-2-2. Design of Land Pattern

(1) Recommended land dimensions are shown below for proper amount of solder to prevent cracking at the time of excessive stress to the Capacitors due to increased amount of solder.

{ Recommended land dimensions (Ex.) }

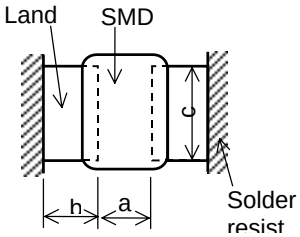
[For General Electronic Equipment, High Capacitance, Low ProfileType, 100V・200V series]



Unit in mm

Type (EIA)	Component Dimension L	W	T	a	b	c
06 (0201)	0.6	0.3	0.3	0.2 to 0.3	0.25 to 0.3	0.2 to 0.3
10 (0402)	1.0	0.5	0.5	0.4 to 0.5	0.4 to 0.5	0.4 to 0.5
11 (0603)	1.6	0.8	0.8	0.8 to 1.0	0.6 to 0.8	0.6 to 0.8
12 (0805)	2.0	1.25	0.6 to 1.25	0.8 to 1.2	0.8 to 1.0	0.8 to 1.0
13 (1206)	3.2	1.6	0.6 to 1.6	1.8 to 2.2	1.0 to 1.2	1.0 to 1.3
23 (1210)	3.2	2.5	1.4 to 2.5	1.8 to 2.2	1.0 to 1.2	1.8 to 2.3
34 (1812)	4.5	3.2	2.5 to 3.2	3.0 to 3.5	1.2 to 1.6	2.3 to 3.0

[Wide-width Type]

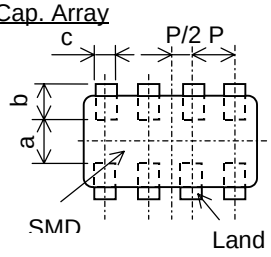


Unit in mm

Type (EIA)	Component Dimension L	W	T	a	b	c
21(0508)	1.25	2.0	0.85	0.5 to 0.7	0.5 to 0.6	1.4 to 1.9
31(0612)	1.6	3.2	0.85	0.8 to 1.0	0.6 to 0.7	2.5 to 3.0

[Array Type]

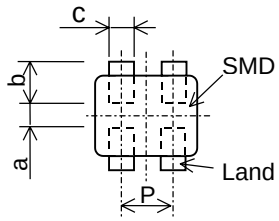
4 Cap. Array



Unit in mm

Type (EIA)	Component Dimension L	W	T	a	b	c	P
12 (0805)	2.0	1.25	0.85	0.55 to 0.75	0.5 to 0.6	0.2 to 0.3	0.4 to 0.6
13 (1206)	3.2	1.6	0.85	0.9 to 1.1	0.7 to 0.9	0.35 to 0.45	0.7 to 0.9

2-fold Array

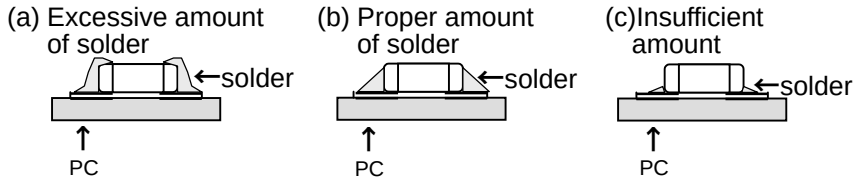


Unit in mm

Type (EIA)	Component Dimension L	W	T	a	b	c	P
11 (0504)	1.37	1.0	0.6	0.3 to 0.4	0.45 to 0.55	0.3 to 0.4	0.54 to 0.74
			0.8	0.3 to 0.6	0.4 to 0.7	0.46 to 0.56	0.71 to 0.91

(2) The size of lands shall be designed to be equal between the right and left sides. If the amount of solder on the right land is different from that on the left land, the component may be cracked by stress to one side of the component since the side with a larger amount of solder solidifies later at the time of cooling.

Recommended Amount of Solder



Note ;

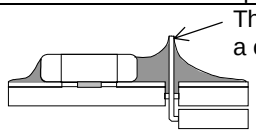
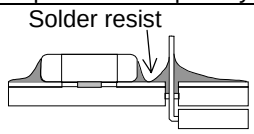
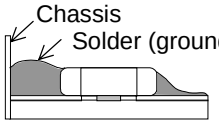
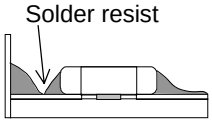
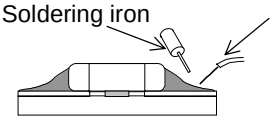
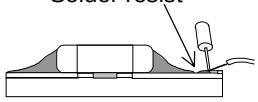
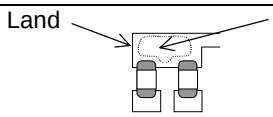
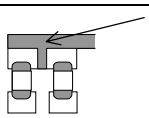
2-2-3. Applications of Solder Resist

Applications of Solder resist are effective to prevent solder bridges and to control amounts of solder on PC boards.

(1) Solder resist shall be utilized to equalize the amounts of solder on both sides.

(2) If the Capacitors are arranged in succession, solder resist shall be used to divide the pattern in the mixed mounting with a component with lead wires or in the arrangement near a chassis etc. See the table below.

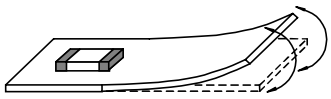
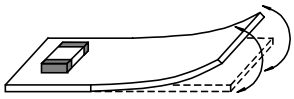
NG Examples and Recommended Examples

	NG Examples	Improved Examples by pattern division
Mixed mounting with a component with lead wires		
Arrangement near chassis		
Retrofitting of Component with lead wires		
Lateral arrangement		

2-2-4. Component Layout

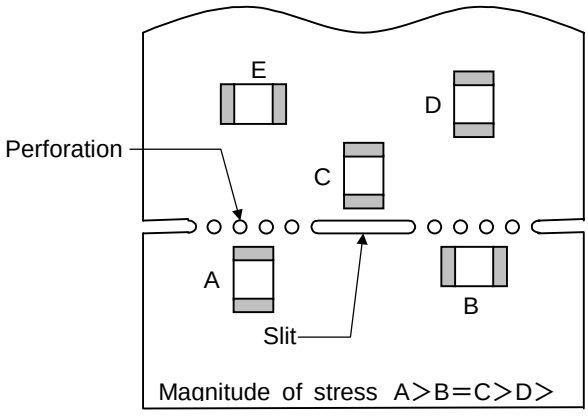
The Capacitors / components shall be placed on the PC board so as to have both electrodes subjected to uniform stresses, or to position the component electrodes at right angles to the grid glove or bending line to avoid cracking in the Capacitors caused by the bending of the PC board after or during placing / mounting the Capacitors / components on the PC board.

(1) The recommended layout of the Capacitor to minimize mechanical stress caused by warp or bending of a PC board is as below.

	NG Example	Recommended Example
Warp of Circuit board		

(2) The following drawing is for your reference since mechanical stress near the dividing/breaking position of a PC board varies depending on the mounting position of the Capacitors.

(3) The magnitude of mechanical stress applied to the Capacitors when the circuit board is divided is in the order of push back < slit < V-groove < perforation.
Also take into account the layout of the Capacitors and the dividing/breaking method.



2-2-5. Mounting Density and Spaces

If components are arranged in too narrow spaces, the components are affected by Solder bridges and Solder balls. Each space between components should be carefully determined.

Note ;

3. Precautions for Assembly

3- 1.Storage

(1) The Capacitors shall be stored under 5 - 40℃ and 20 - 70%RH, not under severe conditions of high temperature and humidity.

(2) If the storage place is humid, dusty, and contains corrosive gasses (hydrogen sulfide, sulfurous acid, hydrogen chloride and ammonia, etc.), the solderability of the terminal electrodes may deteriorate.
Also, storage in a place subjected to heating or exposed to direct sunlight causes deformed tapes and reels of taped version and/or components sticking to tapes, which results in troubles at the time of mounting.

(3) The storage period shall be within 6 months. Products stored for more than 6 months shall be checked their solderability before use.

(4) The Capacitors of high dielectric constant series (Class 2, Characteristic B,X7R,X5R and F,Y5V) change in capacitance with the passage of time, “Capacitance aging”, due to the inherent characteristics of ceramic dielectric materials. The changed capacitance can be recovered by heat treatment to each initial value at the time of shipping. (See 2. Operating Condition and Circuit Design, 2-1-7. Capacitance aging)

(5) When the initial capacitance is measured, the Capacitors shall be heat-treated at 150+0/-10℃ for 1 hour and then subjected to ordinary temperature and humidity for 48±4 hours before measuring the initial value.

3- 2.Adhesives for Mounting

(1) The amount and viscosity of an adhesive for mounting shall be such that the adhesive shall not flow off on the land during it’s curing.

(2) If the amount of adhesive is insufficient for mounting, the Capacitor may fall after or during soldering.

(3) If the adhesive is too low in its viscosity, the Capacitors may be out of alignment after or during soldering.

(4) Adhesives for mounting can be cured by ultraviolet or infrared radiation. In order to prevent the terminal electrodes of the Capacitors from oxidizing, the curing shall be dune at conditions of 160℃ max., for 2 minutes max.

(5) If curing is insufficient, the Capacitor may fall after or during soldering. Also insulation resistance between terminal electrodes may deteriorate due to moisture absorption. In order to prevent these problems, the curing conditions shall be sufficiently examined.

3- 3.Chip Mounting Consideration

(1) When mounting the Capacitors/components on a PC board, the capacitor bodies shall be free from excessive impact loads such as mechanical impact or stress in the positioning, pushing force and displacement of vacuum nozzles at the time of mounting.

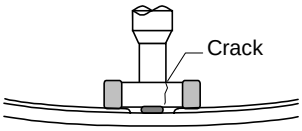
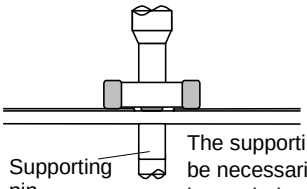
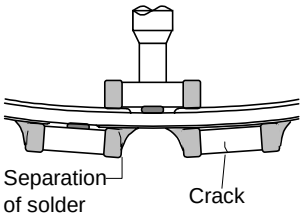
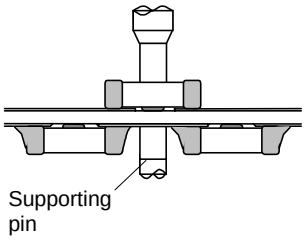
(2) The maintenance and inspections for Chip Mounter must be performed regularly.

(3) If the bottom dead center of the vacuum nozzle is too low, the Capacitor is cracked by an excessive force at the time of mounting.
The following precautions and recommendations are for your reference in use.
   (a) Set and adjust the bottom dead center of the vacuum nozzles to the upper surface of the PC board after correcting the warp of the PC board.
   (b) Set the pushing force of the vacuum nozzle at the time of mounting to 1 to 3 N in static load.
   (c) For double surface mounting, apply a supporting pin on the rear surface of the PC board to suppress the bending of the PC board in order to minimize the impact of the vacuum nozzles. The typical examples are shown in the table below.
   (d) Adjust the vacuum nozzles so that their bottom dead center at the time of mounting is not too low.

(4) The closing dimensions of positioning chucks shall be controlled and the maintenance, checks and replacement of positioning chucks shall be regularly performed to prevent chipping or cracking of the Capacitors caused by mechanical impact at the time of positioning due to worn positioning chucks.

(5) Maximum stroke of the nozzle shall be adjusted so that the maximum bending of PC board does not exceed 0.5mm at 90mm span. The PC board shall be supported by means of adequate supporting pins.

Note ;

	NG Examples	Improved Examples by pattern division
Single surface mounting		
Double surface mounting		

3- 4.Selection of Soldering Flux

Soldering flux may seriously affect the performance of the Capacitors. The following shall be confirmed before use.

(1) Soldering flux having a halogen based content of 0.1 wt. % (converted to chlorine) or below shall be used. Do not use soldering flux with strong acid.

(2) When applying water-soluble soldering flux, wash the Capacitors sufficiently because the soldering flux residue on the surface of PC boards may deteriorate the insulation resistance on the Capacitor surface due to insufficient cleaning.

3- 5.Soldering

3-5-1. Flow soldering

In flow soldering process, abnormal and large thermal and mechanical stresses, caused by "Temperature Gradient" between the mounted Capacitors and melted solder in a soldering bath, may be applied directly to the Capacitors, resulting in failures and damages of the Capacitors, So it is essential that soldering process shall be controlled to the following recommended conditions.

(1) Application of Soldering flux:
The soldering flux shall be applied to the mounted Capacitors thinly and uniformly by foaming method.

(2) Preheating:
The mounted Capacitors/Components shall be preheated sufficiently so that the "Temperature Gradient" between the Capacitors/Components and the melted solder shall be 150℃ max. (100 to130℃)

(3) Immersion into Soldering Bath:
The Capacitors shall be immersed into a soldering bath of 240 to 260℃ for 3 to 5 seconds.

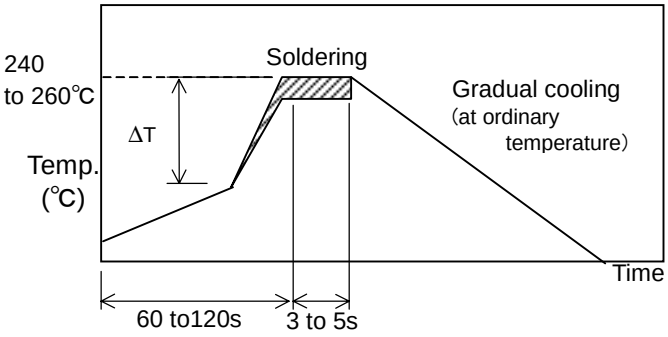
(4) Gradual Cooling:
The Capacitors shall be cooled gradually to room ambient temperature with the cooling temperature rates of 8℃/s max. from 250℃ to 170℃ and 4℃/s max. from 170℃ to 130℃.

(5) Flux Cleaning:
When the Capacitors are immersed into a cleaning solvent, it shall be confirmed that the surface temperatures of devices do not exceed 100℃.

(6) One time of flow soldering under the conditions shown in the figure below [Recommended profile of Flow soldering (Ex)] do not cause any problems.
However, fully pay attention to the possible warp and bending of the PC board.

Note ;

Recommended profile of Flow soldering [Ex.]



〈Allowable temperature difference ΔT〉

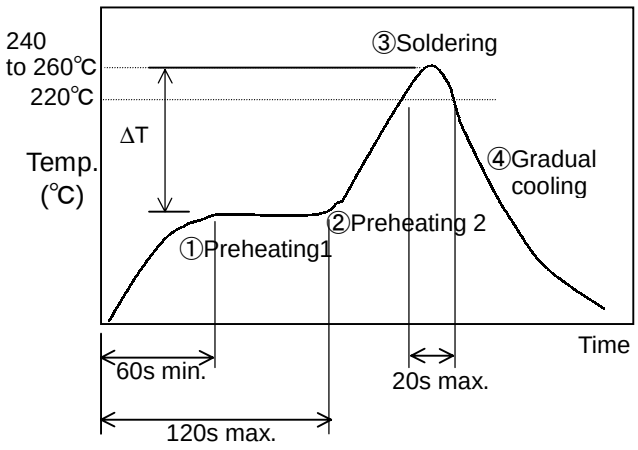
Size	Temp. Tol.
0603 to 1206	ΔT ≦ 150 °C
0508, 0612	

3-5-2. Reflow soldering

In reflow soldering, the mounted Capacitors/Components are generally heated and soldered by a thermal conduction system such as an “Infrared radiation and hot blast soldering system” or a “Vapor Phase Soldering System (VPS)”.
Large temperature gradients such as a rapid heating and cooling in the process may cause electrical failures and mechanical damages of the devices.
It is essential that the soldering process shall be controlled by the following recommended conditions and precautions.

(1) Preheating 1:
The mounted Capacitors/Components shall be preheated sufficiently for 60 to 90 seconds so that the surface temperatures of them to be 140 to 160℃.
(2) Preheating 2 :
After “Preheating 1”, the mounted Capacitors/Components shall be heated to the elevated temperature of 150 to 220℃ for 2 to 5 seconds.
(3) Soldering:
Heating section:220℃ or above within 20 sec .
(4) Gradual cooling:
After the soldering, the mounted Capacitors/Components shall be gradually cooled to room ambient temperature for preventing mechanical damages such as cracking of the devices.
(5) Flux Cleaning:
When the Capacitors are immersed into a cleaning solvent, it shall be confirmed that the surface temperatures of devices do not exceed 100℃.
(6) Two times of flow soldering under the conditions shown in the figure below [Recommended profile of Reflow soldering (Ex)] do not cause any problem. However, fully pay attention to the possible warp and bending of the PC board.

Recommended profile of Reflow soldering (Ex.)



〈 Allowable temperature difference ΔT〉

Size	Temp. Tol.
0201 to 1206	ΔT≦ 150 °C
0508, 0612, 0504	
1210 to 1812	ΔT≦ 130 °C

Note ;

3-5-3. Hand soldering

In hand soldering of the Capacitors, large temperature gradient between the preheated Capacitors and the tip of soldering iron may cause electrical failures and mechanical damages such as cracking or breaking of the devices.

The soldering shall be carefully controlled and carried out so that the temperature gradient is kept minimum with the following recommended conditions for hand soldering.

(1) Condition 1 (with preheating)

(a) Soldering :

ϕ1.0mm Thread eutectic solder with soldering flux* in the core.

*Rosin-based and non-activated flux is recommended.

(b) Preheating:

The Capacitors shall be preheated so that “Temperature Gradient” between the devices and the tip of soldering iron is 150℃ or below.

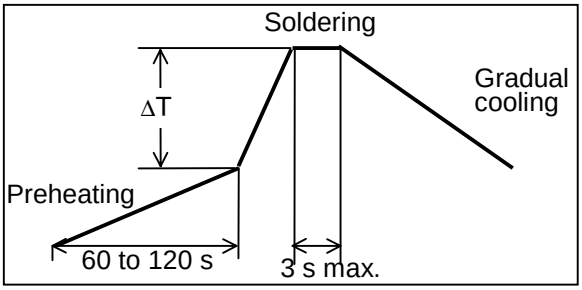
(c) Temperature of Iron tip: 300℃ max.

(The required amount of solder shall be melted in advance on the soldering tip.)

(d) Gradual Cooling:

After soldering, the Capacitors shall be cooled gradually at room ambient temperature.

Recommended profile of Hand Soldering [Ex.]



〈Allowable temperature difference ΔT〉

Size	Temp. Tol.
0201 to 1206	ΔT≦ 150 °C
0508, 0612, 0504	
1210 to 1812	ΔT≦ 130 °C

(2) Condition 2 (without preheating)

Modification with a soldering iron is acceptable without preheating if within the conditions specified below.

(a) Soldering iron tip shall never directly touch the ceramic dielectrics and terminal electrodes of the Capacitors.

(b) The lands are sufficiently preheated with a soldering iron tip before sliding the soldering iron tip to the terminal electrode of the Capacitor for soldering.

Conditions of Hand soldering without preheating

	Condition	
Chip size	0201 to 0805, 0508, 0504	1206 to 1812 , 0612
Temperature of soldering iron	270 °C Max.	250 °C Max.
Wattage	20W Max.	
Shape of soldering iron tip	ϕ3mm Max.	
Soldering time with soldering iron	3s Max.	

3- 6.Post Soldering Cleaning

3-6-1. Residues of soldering fluxes on the PC board after cleaning with an inappropriate solvent may deteriorate on the electrical characteristics and reliability (particularly, insulation resistance) of the Capacitors.

3-6-2. Inappropriate cleaning conditions (Such as insufficient cleaning, excessive cleaning) may impair the electrical characteristics and reliability of the Capacitors.

(1) If cleaning is insufficient :

(a) The halogen substance in the residues of the soldering flux may cause the metal of terminal electrodes to corrode.

(b) The halogen substance in the residues of the soldering flux on the surface of the Capacitors may deteriorate the insulation resistance.

(c) Water-soluble soldering flux may have more remarkable tendencies of (a) and (b) above compared to those of rosin soldering flux.

(2) If cleaning is excessive :

Note ;

(a) Too much output of ultrasonic cleaning may deteriorate the strength of the terminal electrodes or cause cracking in the solder and/or ceramic bodies of the Capacitors due to vibrated PC boards.
The following conditions are for Ultrasonic cleaning.
Ultrasonic wave output: 20 W/L max.
Ultrasonic wave frequency: 40 kHz max.
Ultrasonic wave cleaning time: 5 min. max.

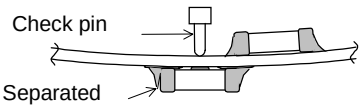
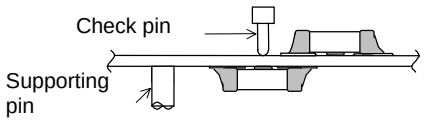
3-6-3. Cleaning with contaminated cleaning solvent may cause the same results in case of insufficient cleaning due to the high density of liberated halogen.

3- 7.Process Inspection

When the mounted PC boards are inspected with measuring terminal pins, abnormal and excess mechanical stresses shall not be applied to the PC board and mounted components, to prevent failures or damages of the devices.

(1) The mounted PC boards shall be supported by some adequate supporting pins setting their bending to 90 mm span 0.5mm max.

(2) It shall be confirmed that measuring pins have a right tip shape, are equal in height and are set in the right positions.
The following figures are for your reference to avoid the possible bending of PC board.

	NG Example	Recommended Example
Bending of PC board		

3- 8.Protective Coat

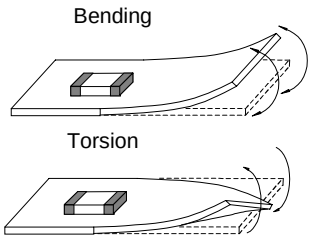
When the surface of a PC board on which the Capacitors have been mounted is coated with resin to protect against moisture and dust, it shall be confirmed that the protective coat does not have influences on the reliability of the Capacitors in the actual equipment.

(1) Coating materials, such as being corrosive and chemically active, shall not be applied to the Capacitors and other components.

(2) Coating materials with large thermal expansivity shall not be applied to the Capacitors for preventing failures or damages (such as cracking) of the devices in the curing process.

3- 9.Dividing/Breaking of PC Boards

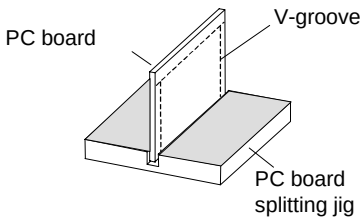
(1) Abnormal and excessive mechanical stresses such as bending or torsion as below, which cause cracking in the Capacitors, on the components on the PC board shall be kept minimum in the dividing/breaking.

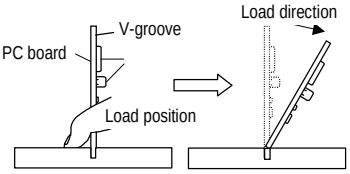
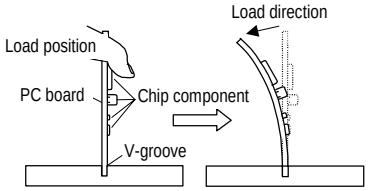


(2) Dividing/Breaking of the PC boards shall be done carefully at moderate speed by using a jig or apparatus to prevent the Capacitors on the boards from mechanical damages.

(3) Examples of PCB dividing/breaking jig
The outline of PC board breaking jig is shown below.
As a recommended example, Dividing/Breaking of the PC boards shall be done by holding the position near the jig where is free from bending, and so as to be compressive stress for the components such as the Capacitors on the PC board.
And as a NG example, if holding the PC board at any position apart from the jig, tensile stress to the Capacitor may cause cracking in the Capacitors.

Outline of Jig



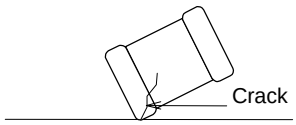
Recommended Example	NG Example
	

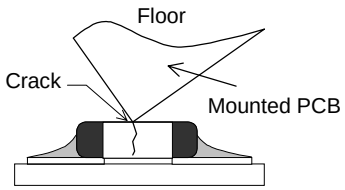
Note ;

3- 10.Mechanical Impact

(1) The Capacitors shall be free from any excessive mechanical impact.
The Capacitor body, which is made of ceramics, may be damaged or cracked by dropping impact.
Never use dropped capacitors because their quality may be already impaired and its failure level of significance may be increased. Particularly, large size capacitors tend to be damaged or cracked more easily.

(2) When handling the PC boards on which the Capacitors are mounted, the Capacitors shall not collide with another PC board.
When mounted PC boards are handled or stored in a stacked state, impact caused by colliding between the corner of the PC board and the Capacitor may cause damage or cracking in the Capacitor and deteriorate the withstand voltage and insulation resistance of the Capacitor.





4. Other

Various precautions described above are typical ones.
For special mounting conditions, please contact us.

Precautions for Use above are from

> The Technical Report EIAJ RCR-2335 Caution Guide Line for Operation of Fixed Multilayer Ceramic Capacitors for Electronic Equipment by Japan Electronics and Information Technology Industries Association (March 2002 issued)

Please refer to above technical report for details.

Note ;

CLASSFICATION	SPECIFICATIONS	No. 151S-ECJ-SV040E
SUBJECT	Multilayer Ceramic Chip Capacitor Packaging Specifications	PAGE 1 of 6
		DATE 28 Jul, 2005

1. Scope
This specification applies to taped and reeled packing for Multilayer ceramic chip capacitors.

2. Applicable Standards
EIAJ (Electric Industries Association of Japan) Standard EIAJ RC-1009B
JIS (Japanese Industrial Standard) Standard JIS C 0806

3. Packing Specification
3- 1.Structure and Dimensions
Paper taping packaging is carried out according the following diagram
1) Carrier tape : Shown in Fig. 6.
2) Reel : Shown in Fig. 7.
3) Packaging : We shall pack suitably in order prevent damage during transportation or storage.

3- 2.Packing Quantity

Type	Thickness of Capacitor(mm)	Carrier-Tape		Quantity (pcs./reel)			
		Material	Taping Pitch	φ180mm Reel		φ330mm Reel	
				Packaging Code	Quantity	Packaging Code	Quantity
06type (0201)	0.30 +/- 0.03	Paper (Press Carrier Tape)	2mm	J	15000	---	---
10type (0402)	0.50 +/- 0.05	Paper (Punch Carrier Tape)	2mm	E	10000	W	50000
11type (0603)	0.8 +/- 0.1		4mm	V	4000	Z	10000
12type (0805)	0.6 +/- 0.1		4mm	V	5000	Z	20000
	0.85 +/- 0.10		4mm	V	4000	Z	10000
	1.25 +/- 0.10 1.25 +/- 0.15 1.25 +/- 0.20	Plastic (Embossed Tape)	4mm	F	3000	---	---
13type (1206)	0.6 +/- 0.1	Paper (Punch Carrier Tape)	4mm	V	5000	Z	20000
	0.85 +/- 0.10		4mm	V	4000	Z	10000
	1.15 +/- 0.10	Plastic (Embossed Taps)	4mm	F	3000	---	---
	1.6 +/- 0.2		4mm	Y	2000	---	---
23type (1210)	2.0 +/- 0.2		4mm	Y	2000	---	---
	2.5 +/- 0.3		4mm	Y	1000	---	---
34type (1812)	2.5 +/- 0.3		8mm	Y	500	---	---
	3.2 +/- 0.3		8mm	Y	500	---	---

Explanation of Part Numbers (Example)

ECJ 1 **V** B 1C 104 K

Packaging Code

3- 3.Marking on the Reel
The following items are described in the side of a reel in English at least.
1) Part Number
2) Quantity
3) Lot Number
4) Place of origin

Note ;

Panasonic Electronic Devices Co., Ltd.	APPROVAL	CHECK	DESIGN
	Y.Sakaguchi	S.Endoh	T.Shinriki

3- 4.Structure of Taping

1) The direction of winding of taping on the reel shall be in accordance with the following diagram.

Fig. 1 Paper Tape

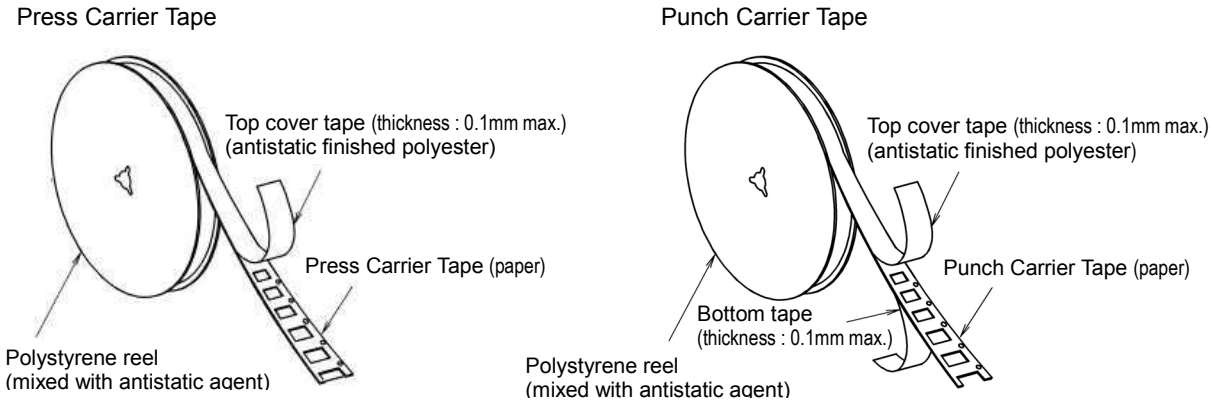
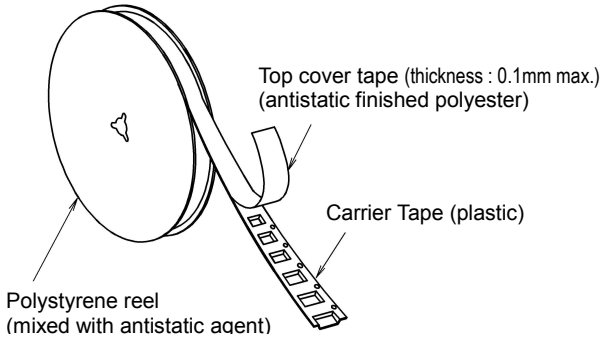
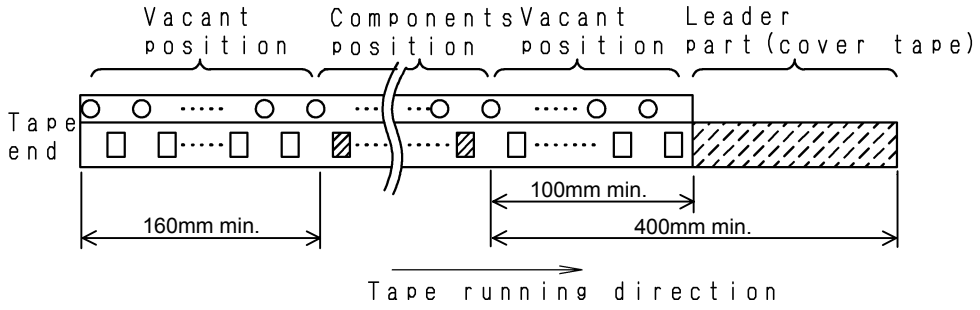


Fig. 2 Embossed Tape



2) The specification of the leader and empty portion shall be in accordance with the following diagram.

Fig. 3 Leader Part and Taped End



Note ;

4. Efficiency

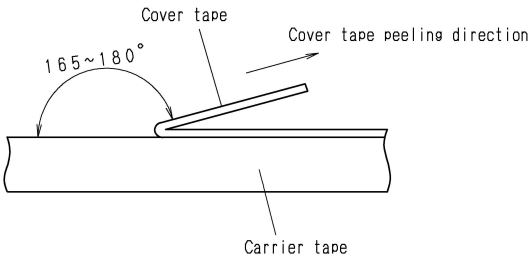
4- 1.Breakage strength of the tape : 10N or more.

4- 2.Peel strength of the cover tape (refer to the Fig.4, 5).

1) Peel angle : 165 to 180 degree from the tape adhesive face.
2) Peel velocity : 300mm per min.
3) Peel strength : 0.1 to 0.7N

Fig. 4 Paper Tape

Press Carrier Tape



Punch Carrier Tape

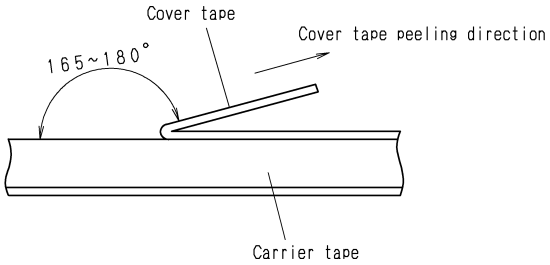
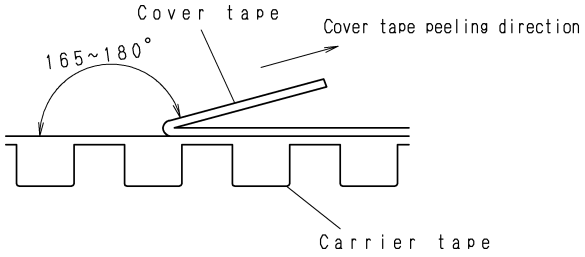


Fig. 5 Embossed Tape



4- 3.Barrs on tape

There shall be no barrs preventing suction when products are taken out.

4- 4.Missing of products

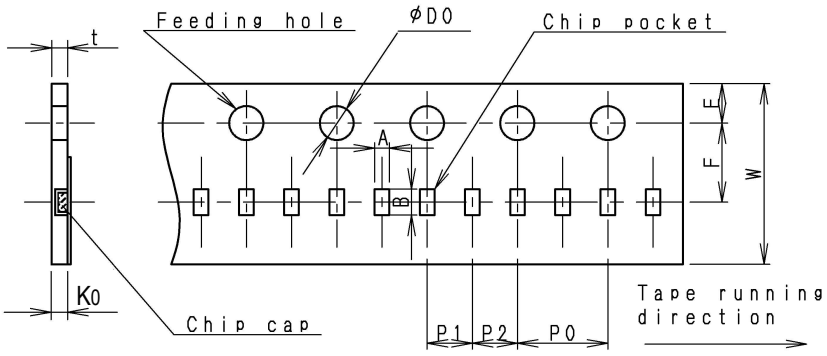
The missing of products shall be 0.1% or less per reel and there shall be no continuous missing of products.

4- 5.Adherence to the tape

Products shall not be stuck to the cover tape or bottom tape.

Fig. 6 Carrier Tape Dimension

(a) 06 type : 2mm pitch for Paper tape



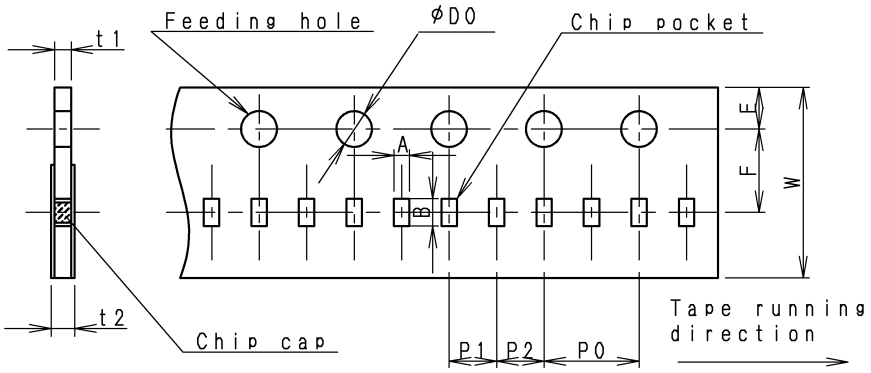
Code	Dimension
W	8.0 ± 0.2
F	3.50 ± 0.05
E	1.75 ± 0.10
P_1	2.00 ± 0.05
P_2	2.00 ± 0.05
P_0	4.0 ± 0.1
D_0	φ 1.5 +0.1/-0
t	0.55 max.
K_0	0.36 ± 0.03

Unit : mm

Code \ Type	06 (0201)
A	0.36 +/- 0.03
B	0.66 +/- 0.03

Note ;

(b) 10 type : 2mm pitch for Paper tape

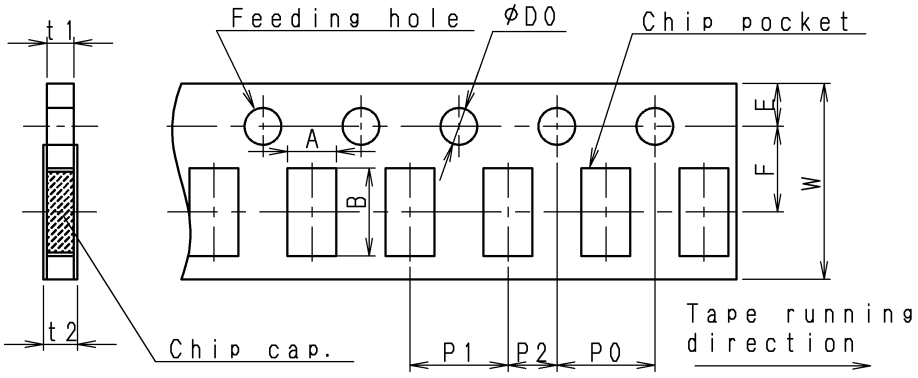


Code	Dimension
W	8.0 +/- 0.2
F	3.50 +/- 0.05
E	1.75 +/- 0.10
P_1	2.00 +/- 0.05
P_2	2.00 +/- 0.05
P_0	4.0 +/- 0.1
D_0	ϕ1.5 +0.1/-0
t_1	0.7 max.
t_2	1.0 max.

Unit : mm

Code \ Type	10 (0402)
A	0.62 +/- 0.05
B	1.12 +/- 0.05

(c) 11, 12 and 13 type : 4mm pitch for Paper tape



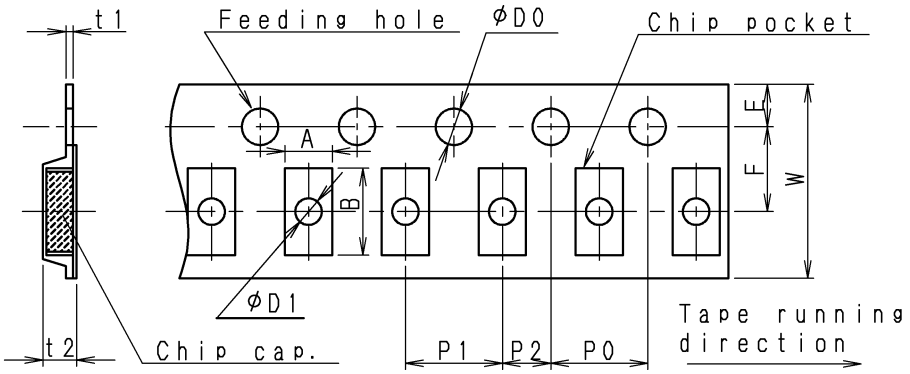
Code	Dimension
W	8.0 +/- 0.2
F	3.50 +/- 0.05
E	1.75 +/- 0.10
P_1	4.0 +/- 0.1
P_2	2.00 +/- 0.05
P_0	4.0 +/- 0.1
D_0	ϕ1.5 +0.1/-0
t_1	1.1 max.
t_2	1.4 max.

Unit : mm

Code \ Type	11 (0603)	12 (0805)	13 (1206)
A	1.0 +/- 0.1	1.65 +/- 0.20	2.0 +/- 0.2
B	1.8 +/- 0.1	2.4 +/- 0.2	3.6 +/- 0.2

Note ;

(d) 12 , 13 and 23 type : 4mm pitch for Embossed tape

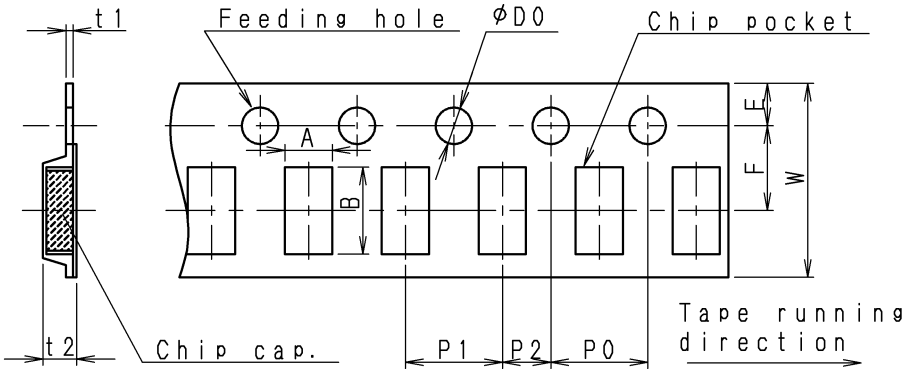


Code	Dimension	
W	8.0 +/- 0.2	
F	3.50 +/- 0.05	
E	1.75 +/- 0.10	
P_1	4.0 +/- 0.1	
P_2	2.00 +/- 0.05	
P_0	4.0 +/- 0.1	
D_0	ϕ1.5 +0.1/-0	
D_1	ϕ1.1+/- 0.1	
t_1	0.6 max.	
t_2	"12" "13" Type	2.5 max.
	"23" Type	3.5 max.

Unit : mm

Code \ Type	12 (0805)	13 (1206)	23 (1210)
A	1.55 +/- 0.20	1.90 +/- 0.20	2.8 +/- 0.2
B	2.35 +/- 0.20	3.5 +/- 0.2	3.5 +/- 0.2

(e) 34 type : 8mm pitch for Embossed tape



Code	Dimension
W	12.0 +/- 0.3
F	5.50 +/- 0.05
E	1.75 +/- 0.10
P_1	8.0 +/- 0.1
P_2	2.00 +/- 0.05
P_0	4.0 +/- 0.1
D_0	ϕ1.5 +0.1/-0
t_1	0.6 max.
t_2	4.0max.

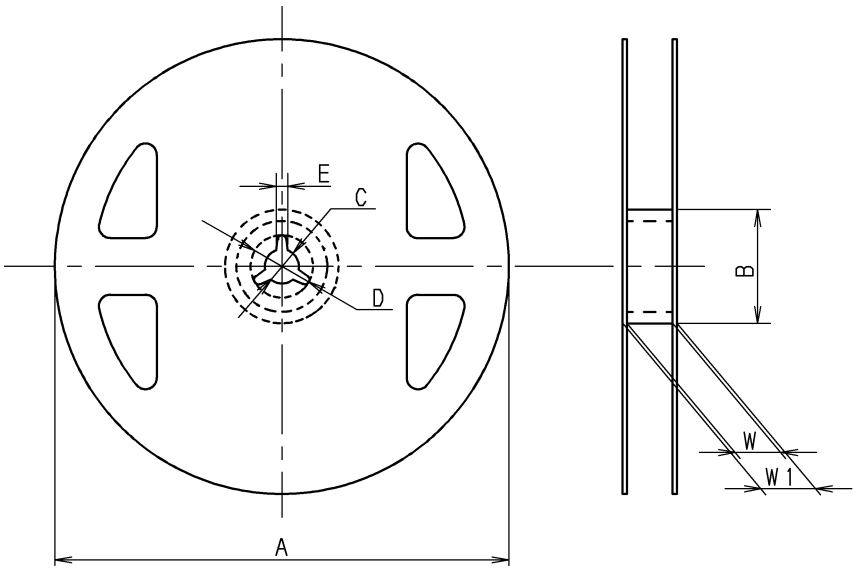
Unit:mm

Code \ Type	34 (1812)
A	3.6 +/- 0.3
B	4.9 +/- 0.3

Note ;

Fig. 7 Reel Dimension

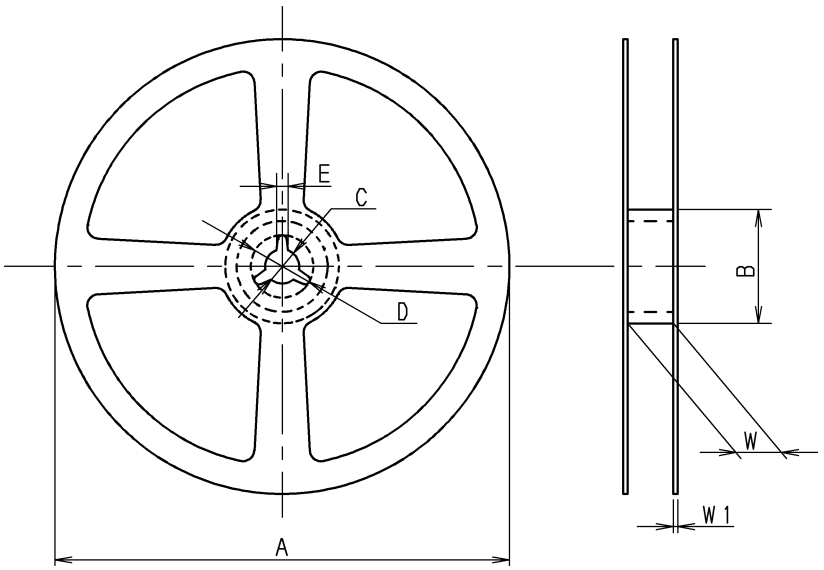
(a) ϕ180mm Reel (Standard Reel)



Code	Dimension	
A	ϕ180+0/-3.0	
B	ϕ60 +/- 0.5	
C	13.0 +/- 0.5	
D	21.0 +/- 0.8	
E	2.0 +/- 0.5	
W	Tape width : 8 mm	9.0 +/- 0.3
	Tape width : 12 mm	13.0 +/- 0.3
W_1	Tape width : 8 mm	11.4 +/- 1.0
	Tape width : 12 mm	15.4 +/- 1.0

Unit : mm

(b) ϕ330mm Reel (Large size Reel)



Code	Dimension
A	ϕ330 +/- 5.0
B	ϕ50 min.
C	13.0 +/- 0.5
D	20 min.
E	2.0 +/- 0.5
W	9.5 +/- 1.0
W_1	2.0 +/- 0.5

Unit : mm

Note ;

单击下面可查看定价，库存，交付和生命周期等信息

>>Panasonic(松下)