# Notification about the transfer of the semiconductor business

The semiconductor business of Panasonic Corporation was transferred on September 1, 2020 to Nuvoton Technology Corporation (hereinafter referred to as "Nuvoton"). Accordingly, Panasonic Semiconductor Solutions Co., Ltd. became under the umbrella of the Nuvoton Group, with the new name of Nuvoton Technology Corporation Japan (hereinafter referred to as "NTCJ").

In accordance with this transfer, semiconductor products will be handled as NTCJ-made products after September 1, 2020. However, such products will be continuously sold through Panasonic Corporation.

Publisher of this Document is NTCJ.

If you would find description "Panasonic" or "Panasonic semiconductor solutions", please replace it with NTCJ.

\* Except below description page

"Request for your special attention and precautions in using the technical information and semiconductors described in this book"

Nuvoton Technology Corporation Japan

# **Panasonic**

MOS FET FC6K3339ZL

Unit : mm

# FC6K3339ZL

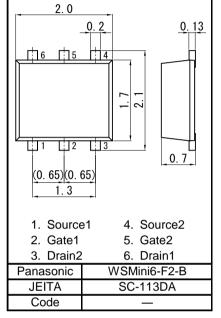
Resistors, Zener Diode installed separate type dual N-channel MOS FET

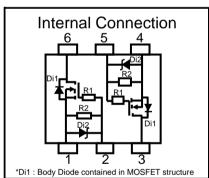
For passive cell balancing circuits

- Features
- Build in Gate Resistor, Gate-source Resistor and Zener Diode
- Drain-source ON-state Resistance : RDS(on) typ. = 200 mΩ (VGS = 4.5 V)
- AEC-Q101 qualified
- Halogen-free / RoHS compliant (EU RoHS / UL-94 V-0 / MSL : Level 1 compliant)
- Marking Symbol : 6J

#### Packaging

Embossed type (Thermo-compression sealing): 3 000 pcs / reel (standard)





#### ■ Absolute Maximum Ratings Ta = 25°C

Parameter	Symbol	Rating	Unit	
Drain to Source Voltage	VDS	30	V	
Gate to Source Voltage	VGS	+5 , -0.5	V	
Drain Current <sup>*1</sup>	ID	1.5	А	
Drain Current (Pulsed) *2	IDp	15	А	
Total Power Dissipation <sup>*1</sup>	PD	700	mW	
Channel Temperature	Tch	150	°C	
Storage Temperature Range	Tstg	-55 to +150	°C	

Note \*1 Mounted on FR4 board (25.4mm × 25.4mm × t1.0mm)

\*2 Pulse width = 10  $\mu$ s, Duty cycle  $\leq$  1 %



## MOS FET FC6K3339ZL

#### Electrical Characteristics $Ta = 25 \degree C \pm 3 \degree C$

	Parameter	Symbol	Conditions	Min	Тур	Max	Unit
Drai	n-source Breakdown Voltage	VDSS	ID = 1 mA , VGS = 0 V	30			V
Zero	Gate Voltage Drain Current	IDSS	VDS = 30 V, VGS = 0 V			1	μA
Gate	e-source Leakage Current	IGSS	VGS = 4.5 V , VDS = 0 V			30	μA
Gate	e-source Threshold Voltage	Vth	ID = 59 μA , VDS = 10 V	0.35		0.9	V
Drain-source ON-state Resistance		RDS(on)1	ID = 0.75 A , VGS = 4.5 V		200	280	mΩ
		RDS(on)2	ID = 0.75 A , VGS = 2.5 V		220	310	
		RDS(on)3	ID = 0.2 A , VGS = 1.5 V		300	900	
Di1	Body Diode Forward Voltage	VSD	ID = 0.75 A , VGS = 0 V		0.8	1.2	V
Di2	Zener Diode Forward Voltage	VF	IF = 100 μA			0.8	V
DIZ	Zener Diode Reverse Voltage	VZ	IZ = 1 mA	5.0			V
R1	Gate Resistance *3	Rg	-	1.0	1.5	3.0	kΩ
R2	Gate-source Resistance *3	Rgs	-	200	300	400	kΩ
Inpu	t Capacitance <sup>*3</sup>	Ciss	VDS = 15 V		95.0		
Output Capacitance *3		Coss	VGS = 0 V		17.5		pF
Rev	erse Transfer Capacitance *3	Crss	f = 1 kHz		10.5		
Turr	-on Delay Time <sup>*3 *4</sup>	td(on)	VDD = 15 V		50		
Rise	Time <sup>*3 *4</sup>	tr	VDD = 15 V VGS = 0 to 4 V		110		20
Turr	-off Delay Time <sup>*3 *4</sup>	td(off)	ID = 0.75 A		480		ns
Fall	Time *3 *4	tf	- 0.73 K		210		
Tota	I Gate Charge <sup>*3</sup>	Qg	VDD = 15 V		1.8		
Gate	e to Source Charge *3	Qgs	VGS = 4 V		0.3		nC
Gate	e to Drain Miller Charge *3	Qgd	ID = 0.75 A		0.4		

Note Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030 Measuring methods for transistors. \*3 Assured by design.

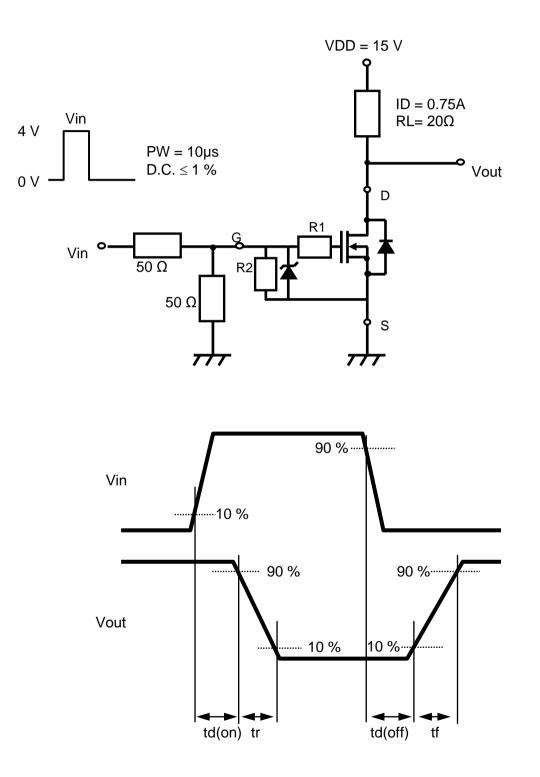
\*4 Refer to Figure 1, measurement circuit for Turn-on Delay Time / Rise Time / Turn-off Delay Time / Fall Time

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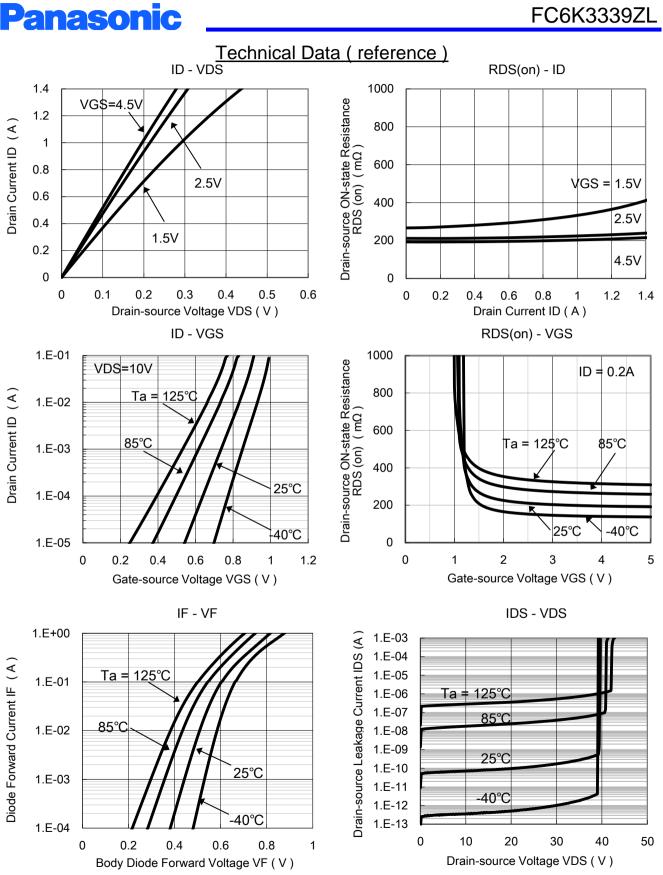


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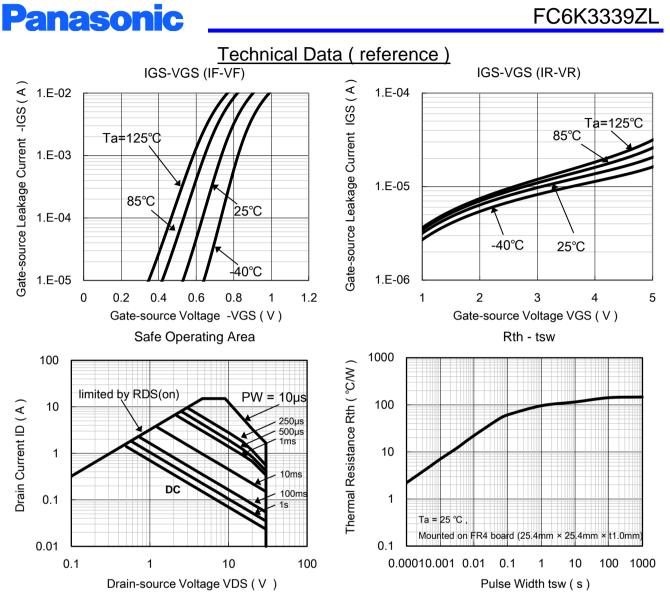
Figure1: Measurement circuit for Turn-on Delay Time / Rise Time / Turn-off Delay Time / Fall Time

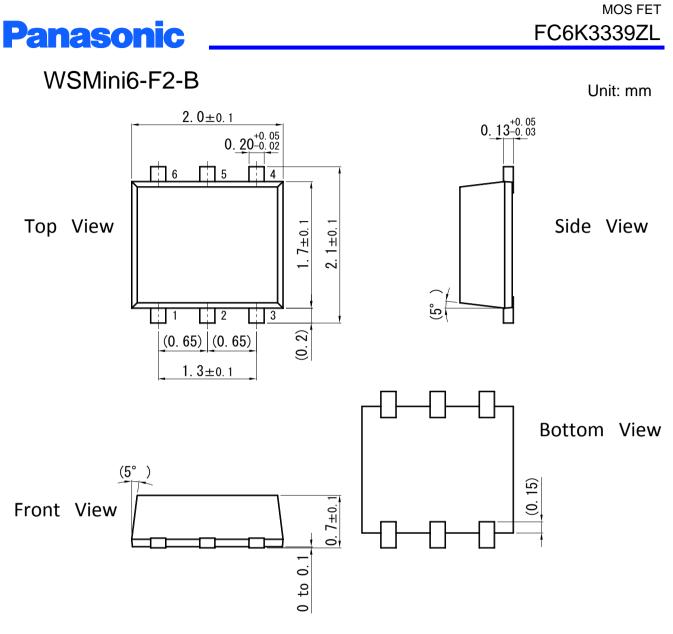


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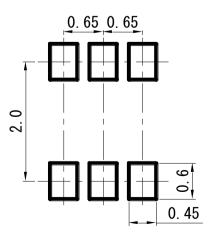


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Land Pattern (Reference) (Unit: mm)



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