

## **Notification about the transfer of the semiconductor business**

The semiconductor business of Panasonic Corporation was transferred on September 1, 2020 to Nuvoton Technology Corporation (hereinafter referred to as "Nuvoton"). Accordingly, Panasonic Semiconductor Solutions Co., Ltd. became under the umbrella of the Nuvoton Group, with the new name of Nuvoton Technology Corporation Japan (hereinafter referred to as "NTCJ").

In accordance with this transfer, semiconductor products will be handled as NTCJ-made products after September 1, 2020. However, such products will be continuously sold through Panasonic Corporation.

Publisher of this Document is NTCJ.

If you would find description "Panasonic" or "Panasonic semiconductor solutions", please replace it with NTCJ.

※ Except below description page

"Request for your special attention and precautions in using the technical information and semiconductors described in this book"

**Nuvoton Technology Corporation Japan**

## FCAB22710L Dual N-channel MOS FET

### ■ Features

- Source-source On-state Resistance :  $R_{SS(on)}$  typ. = 7.5 m $\Omega$  ( VGS = 3.8 V )
- CSP ( Chip Size Package )
- Halogen-free / RoHS compliant ( EU RoHS / UL-94 V-0 / MSL : Level 1 )

### ■ Marking Symbol : WJ

### ■ Packaging

Embossed type ( Thermo-compression sealing ) : 10 000 pcs / reel ( standard )

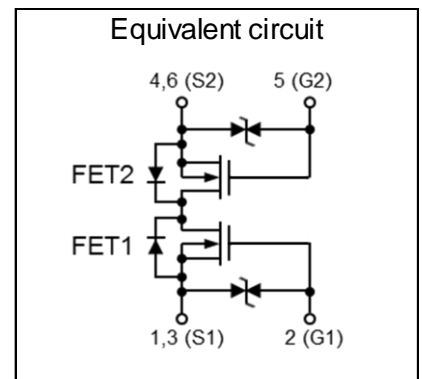
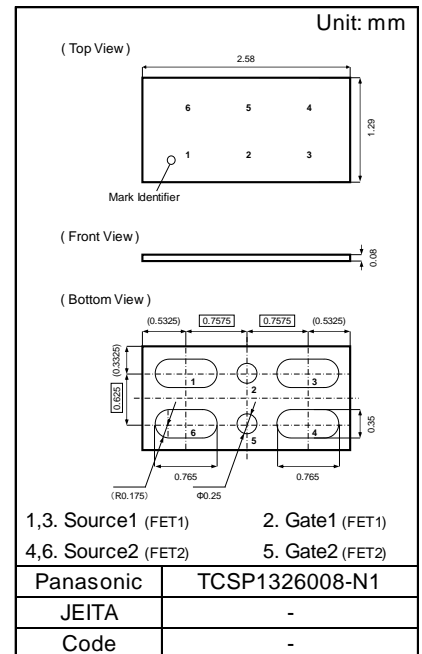
### ■ Absolute Maximum Ratings Ta = 25 °C

Parameter	Symbol	Rating	Unit
Source-source Voltage	VSS	20	V
Gate-source Voltage	VGS	$\pm 12$	V
Source Current	DC	IS1 <sup>*1</sup>	6.1
		IS2 <sup>*2</sup>	10.9
		IS3 <sup>*3</sup>	15.0
	Pulsed <sup>*4</sup>	ISp	61
Total Power Dissipation	DC	PD1 <sup>*1</sup>	0.51
		PD2 <sup>*2</sup>	1.6
		PD3 <sup>*3</sup>	3.0
Channel Temperature	Tch	150	°C
Storage Temperature Range	Tstg	-55 to +150	°C

### ■ Thermal Characteristics Ta = 25 °C

Parameter	Symbol	Rating	Unit
Thermal Resistance ( ch-a )	Rth1 <sup>*1</sup>	245	°C / W
	Rth2 <sup>*2</sup>	78	
	Rth3 <sup>*3</sup>	41	

- Note
- \*1 Mounted on FR4 board ( 25.4 mm × 25.4 mm × t1.0 mm ).  
FR4 board partially covered with copper pad ( 22 mm<sup>2</sup> area, 36  $\mu$ m thickness ).
  - \*2 Mounted on FR4 board ( 25.4 mm × 25.4 mm × t1.0 mm ).  
FR4 board fully covered with copper pad ( 602 mm<sup>2</sup> area, 36  $\mu$ m thickness ).
  - \*3 Mounted on ceramic board ( 70 mm × 70 mm × t1.0 mm ).
  - \*4 t = 10  $\mu$ s, Duty Cycle  $\leq$  1 %.



■ Electrical Characteristics Ta = 25 °C ± 3 °C

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Source-source Breakdown Voltage	VSSS	IS = 1 mA, VGS = 0 V	20			V
Zero Gate Voltage Source Current	ISSS	VSS = 20 V, VGS = 0 V			1.0	μA
Gate-source Leakage Current	IGSS1	VGS = ±8 V, VSS = 0 V			±10	μA
	IGSS2	VGS = ±5 V, VSS = 0 V			±1.0	
Gate-source Threshold Voltage	Vth	IS = 0.54 mA, VSS = 10 V	1.3	1.85	2.35	V
Source-source On-state Resistance	RSS(on)1	IS = 3.05 A, VGS = 4.5 V	3.9	5.5	7.5	mΩ
	RSS(on)2	IS = 3.05 A, VGS = 3.8 V	5.3	7.5	12.5	
	RSS(on)3	IS = 0.20 A, VGS = 3.1 V	5.4	16.5	70.0	
Body Diode Forward Voltage	VF(s-s)	IF = 3.05 A, VGS = 0 V		0.8	1.2	V
Turn-on Delay Time <sup>*1,2</sup>	td(on)	VDD = 10 V, VGS = 0 to 4 V		62		ns
Rise Time <sup>*1,2</sup>	tr	IS = 3.05 A		240		
Turn-off Delay Time <sup>*1,2</sup>	td(off)	VDD = 10 V, VGS = 4 to 0 V		155		ns
Fall Time <sup>*1,2</sup>	tf	IS = 3.05 A		140		
Total Gate Charge <sup>*1</sup>	Qg	VDD = 10 V		17.5		nC
Gate-source Charge <sup>*1</sup>	Qgs	VGS = 0 to 4 V		6.5		
Gate-drain Charge <sup>*1</sup>	Qgd	IS = 6.1 A		6.5		
Gate Resistance <sup>*1</sup>	Rg	f = 1 MHz		24.5		

(MOSFET : FET1)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input Capacitance <sup>*1</sup>	Ciss	VSS = 10 V, f = 1 kHz VGS1 = 0 V, VGS2 = 6 V		2320		pF
Output Capacitance <sup>*1</sup>	Coss			265		
Reverse Transfer Capacitance <sup>*1</sup>	Crss			205		

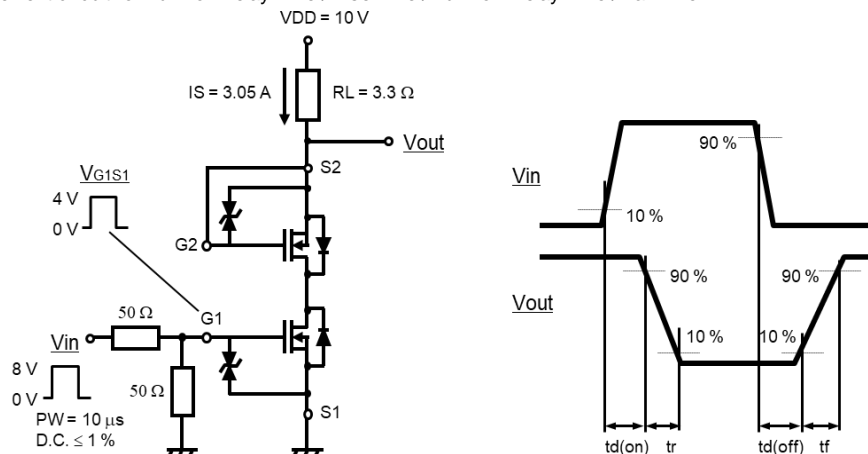
(MOSFET : FET2)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input Capacitance <sup>*1</sup>	Ciss	VSS = 10 V, f = 1 kHz VGS2 = 0 V, VGS1 = 6 V		2320		pF
Output Capacitance <sup>*1</sup>	Coss			265		
Reverse Transfer Capacitance <sup>*1</sup>	Crss			205		

Note Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030 Measuring methods for transistors.

\*1 Guaranteed by design, not subject to production testing.

\*2 Measurement circuit for Turn-on Delay Time / Rise Time / Turn-off Delay Time / Fall Time.

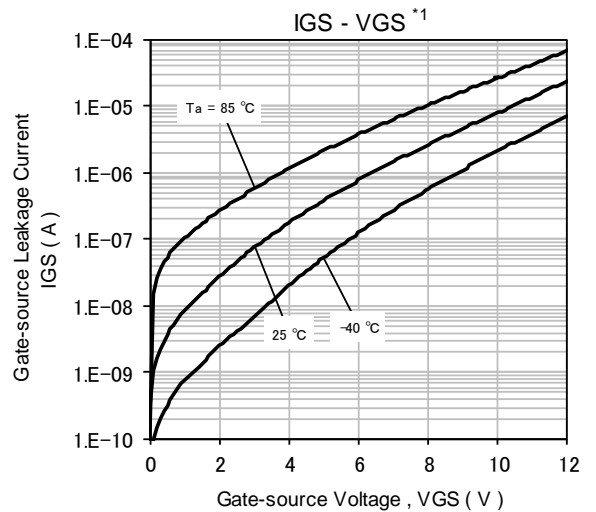
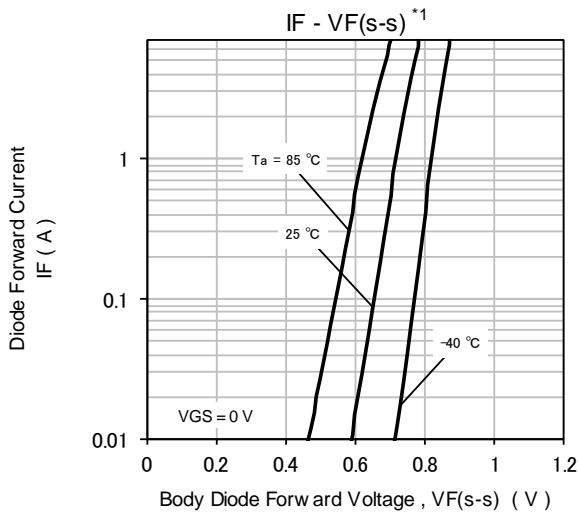
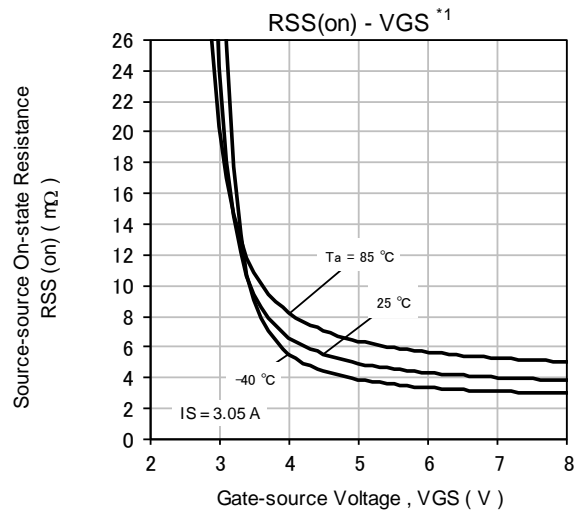
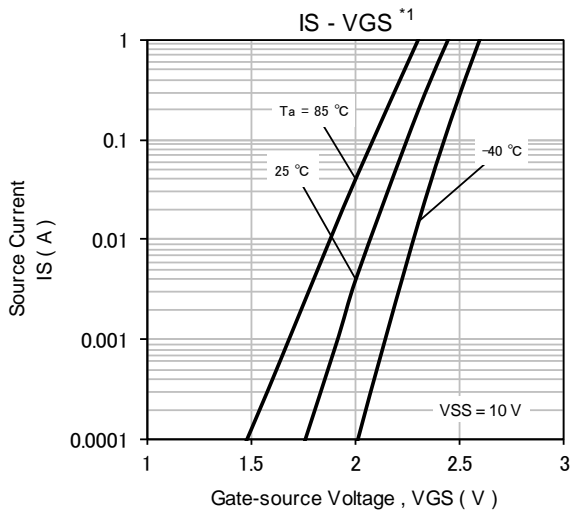
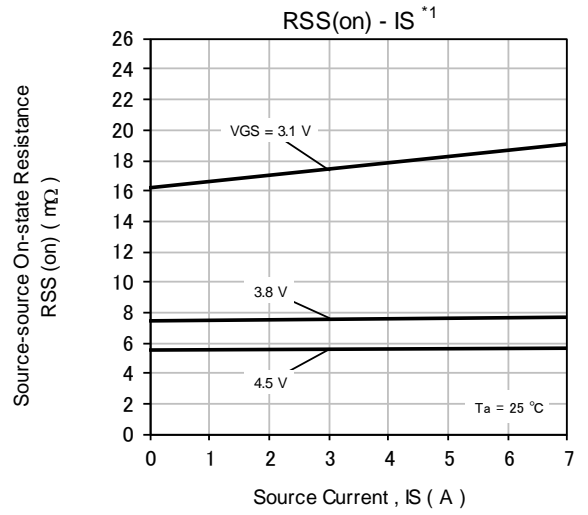
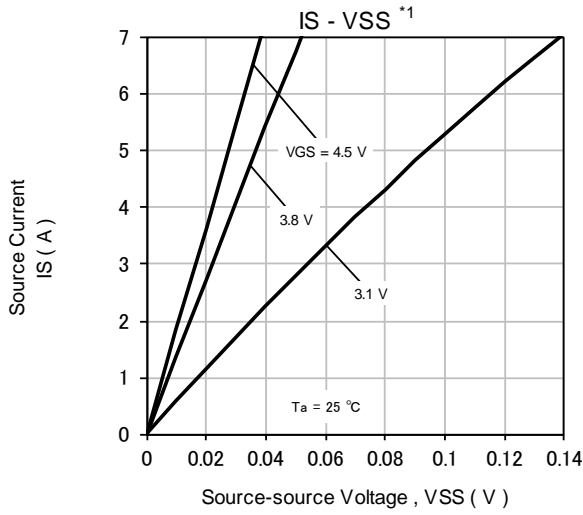


■ Electrostatic Discharge Characteristics Ta = 25 °C ± 3 °C

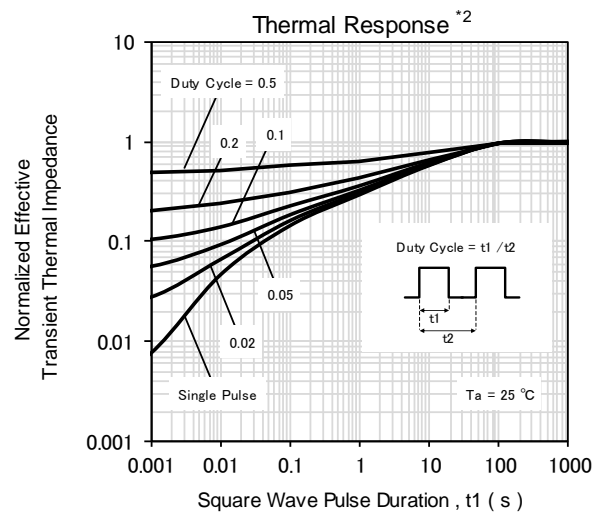
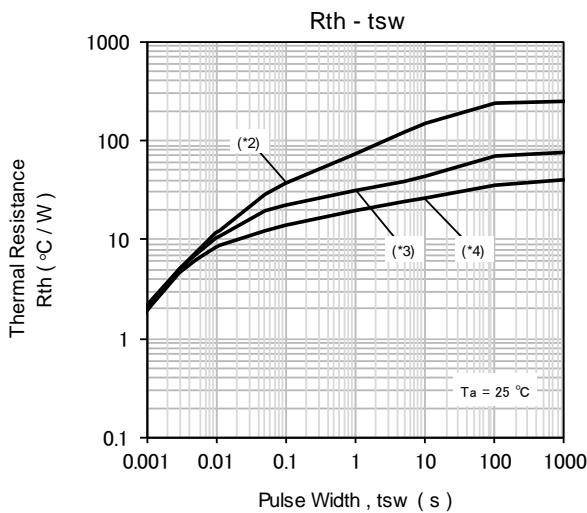
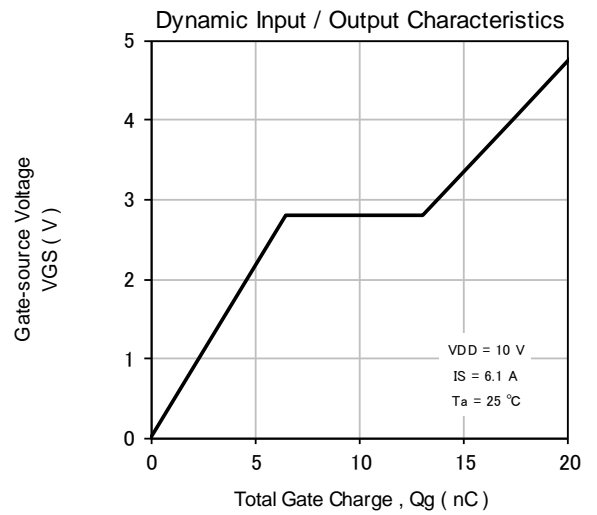
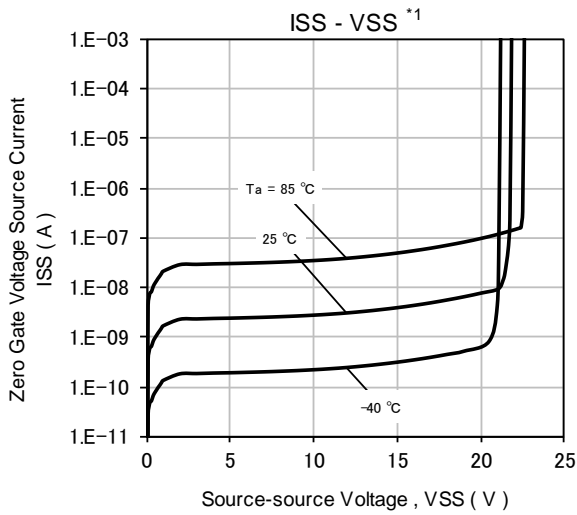
Standard	Test Type	Symbol	Conditions	Class	Value	Unit
AEC-Q101-001	Human Body Model	HBM	C = 100 pF, R = 1.5 kΩ	H1B	> 0.5 to ≤ 1	kV



Technical Data ( reference )



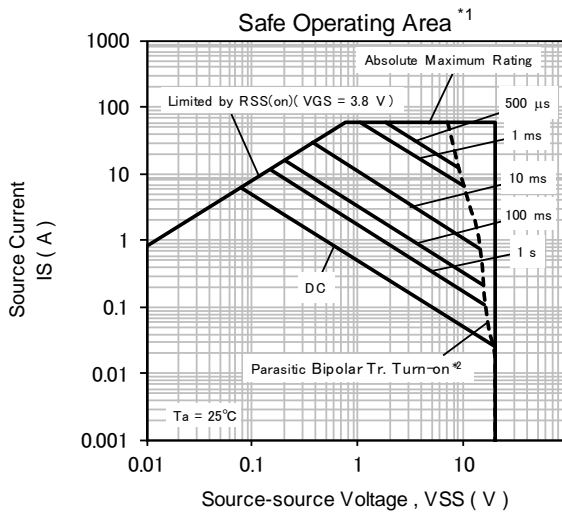
Technical Data ( reference )



Note

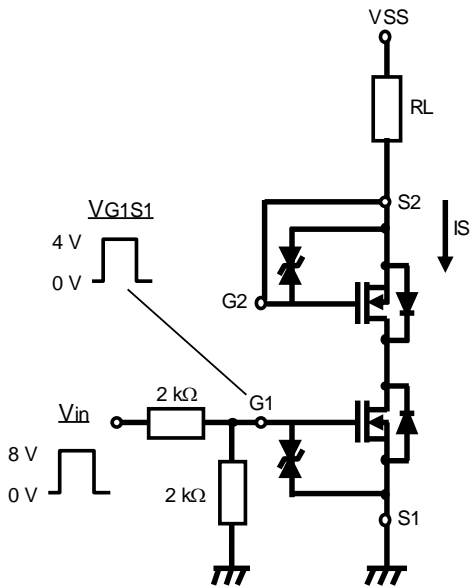
- \*1 Pulse measurement.
- \*2 Mounted on FR4 board ( 25.4 mm × 25.4 mm × t1.0 mm ).  
FR4 board partially covered with copper pad  
( 22 mm<sup>2</sup> area, 36 μm thickness ).
- \*3 Mounted on FR4 board ( 25.4 mm × 25.4 mm × t1.0 mm ).  
FR4 board fully covered with copper pad  
( 602 mm<sup>2</sup> area, 36 μm thickness ).
- \*4 Mounted on ceramic board ( 70 mm × 70 mm × t1.0 mm ).

Technical Data ( reference )



Note

- \*1 Mounted on FR4 board ( 25.4 mm × 25.4 mm × 1.0 mm ).  
 FR4 board partially covered w with copper pad  
 ( 22 mm<sup>2</sup> area, 36  $\mu\text{m}$  thickness ).
- \*2 Measurement circuit for Parasitic Bipolar Tr. Turn-on.



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