

Notification about the transfer of the semiconductor business

The semiconductor business of Panasonic Corporation was transferred on September 1, 2020 to Nuvoton Technology Corporation (hereinafter referred to as "Nuvoton"). Accordingly, Panasonic Semiconductor Solutions Co., Ltd. became under the umbrella of the Nuvoton Group, with the new name of Nuvoton Technology Corporation Japan (hereinafter referred to as "NTCJ").

In accordance with this transfer, semiconductor products will be handled as NTCJ-made products after September 1, 2020. However, such products will be continuously sold through Panasonic Corporation.

Publisher of this Document is NTCJ.

If you would find description "Panasonic" or "Panasonic semiconductor solutions", please replace it with NTCJ.

※ Except below description page

"Request for your special attention and precautions in using the technical information and semiconductors described in this book"

Nuvoton Technology Corporation Japan

FG6K42060L

Silicon N-channel MOSFET (FET1)

Silicon P-channel MOSFET (FET2)

For Switching

■ Features

- Low drain-source ON resistance:RDS(on)typ.
N-ch = 2 Ω (VGS = 4.0 V) P-ch:95 mΩ (VGS = -4.0 V)
- Halogen-free / RoHS compliant
(EU RoHS / UL-94 V-0 / MSL:Level 1 compliant)

■ Marking Symbol: Y7

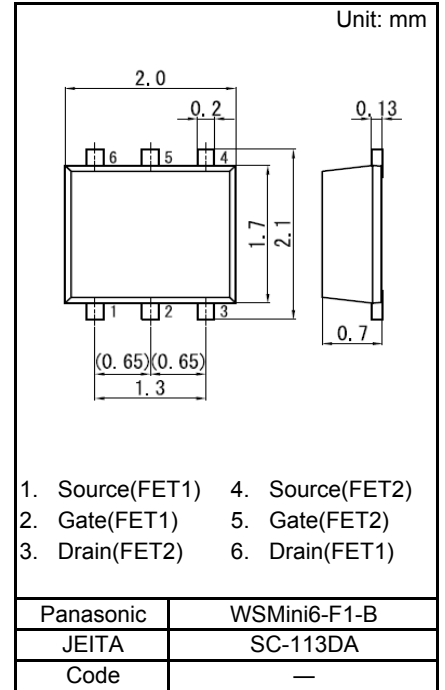
■ Packaging

FG6K42060L Embossed type (Thermo-compression sealing):
3 000 pcs / reel (standard)

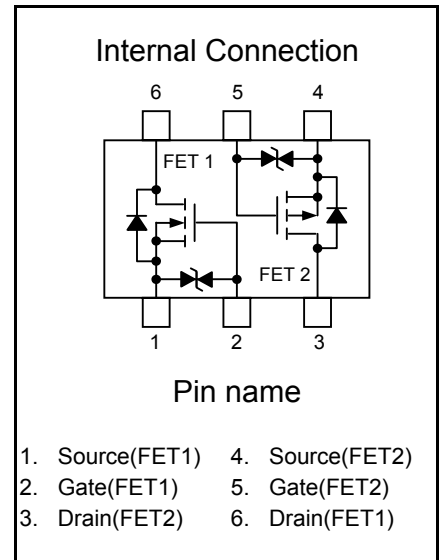
■ Absolute Maximum Ratings Ta = 25 °C

Parameter		Symbol	Rating	Unit
FET1 (Nch.)	Drain-source Voltage	VDS	30	V
	Gate-source Voltage	VGS	±12	V
	Drain Current	ID	100	mA
	Drain Current (Pulsed)	IDp	200	mA
FET2 (Pch.)	Drain-source Voltage	VDS	-20	V
	Gate-source Voltage	VGS	±10	V
	Drain Current	ID	-2	A
	Drain Current (Pulsed)	IDp	-8	A
Overall	Total Power Dissipation ^{*1}	PD	700	mW
	Channel Temperature	Tch	150	°C
	Storage Temperature	Tstg	-55 to +150	°C

Note: *1 Measuring on ceramic substrate at 40 mm × 38 mm × 0.1 mm.
PD absolute maximum rating Non-heat sink: 150 mW.



1. Source(FET1)
2. Gate(FET1)
3. Drain(FET2)
4. Source(FET2)
5. Gate(FET2)
6. Drain(FET1)



■ Electrical Characteristics Ta = 25 °C ± 3 °C
FET1(Nch.)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Drain-source Breakdown Voltage	VDSS	ID = 1 mA, VGS = 0 V	30			V
Zero Gate Voltage Drain Current	IDSS	VDS = 30 V, VGS = 0 V			1.0	μA
Gate-source Leakage Current	IGSS	VGS = ±10 V, VDS = 0 V			±10	μA
Gate-source Threshold Voltage	Vth	ID = 1.0 μA, VDS = 3.0 V	0.5	1	1.5	V
Drain-source On-state Resistance *1	RDS(on)1	ID = 10 mA, VGS = 2.5 V		3	6	Ω
	RDS(on)2	ID = 10 mA, VGS = 4.0 V		2	3	
Forward transfer admittance *1	Yfs	ID = 10 mA, VDS = 3.0 V	20	55		mS
Input Capacitance	Ciss	VDS = 3.0 V, VGS = 0 V, f = 1 MHz		12		pF
Output Capacitance	Coss			7		
Reverse Transfer Capacitance	Crss			3		
Turn-on Time *2	ton	VDD = 3.0 V, VGS = 0 to 3.0 V ID = 10 mA		100		ns
Turn-off Time *2	toff	VDD = 3.0 V, VGS = 3.0 to 0 V ID = 10 mA		100		ns

Note: Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030 Measuring methods for transistors.

*1 Pulse measurement

*2 See Test circuit.

FET2(Pch.)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Drain-source Breakdown Voltage	VDSS	ID = -1 mA, VGS = 0 V	-20			V
Zero Gate Voltage Drain Current	IDSS	VDS = -20 V, VGS = 0 V			-1.0	μA
Gate-source Leakage Current	IGSS	VGS = ±8 V, VDS = 0 V			±10	μA
Gate-source Threshold Voltage	Vth	ID = -1.0 mA, VDS = -10 V	-0.4	-0.75	-1.1	V
Drain-source On-state Resistance *3	RDS(on)1	ID = -0.5 A, VGS = -1.8 V		155	245	mΩ
	RDS(on)2	ID = -1 A, VGS = -2.5 V		115	185	
	RDS(on)3	ID = -1 A, VGS = -4.0 V		95	135	
Forward transfer admittance *3	Yfs	ID = -1.0 A, VDS = -10 V	3.0			S
Input Capacitance	Ciss	VDS = -10 V, VGS = 0 V, f = 1 MHz		300		pF
Output Capacitance	Coss			30		
Reverse Transfer Capacitance	Crss			35		
Turn-on Delay Time *4	ton	VDD = -10 V, VGS = 0 to -4.0 V ID = -1.0 A		14		ns
Turn-off Delay Time *4	toff	VDD = -10 V, VGS = -4.0 to 0 V ID = -1.0 A		112		ns

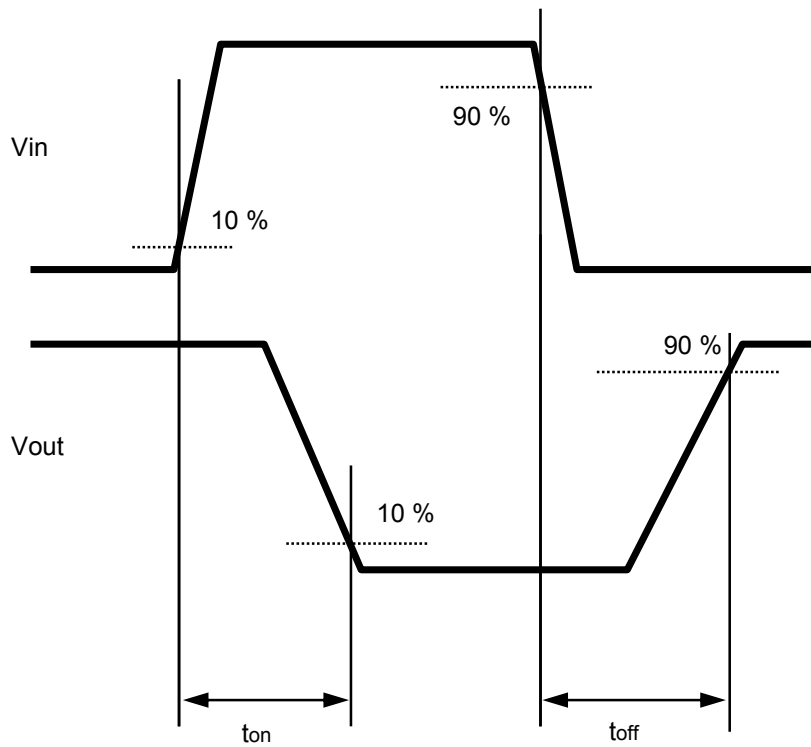
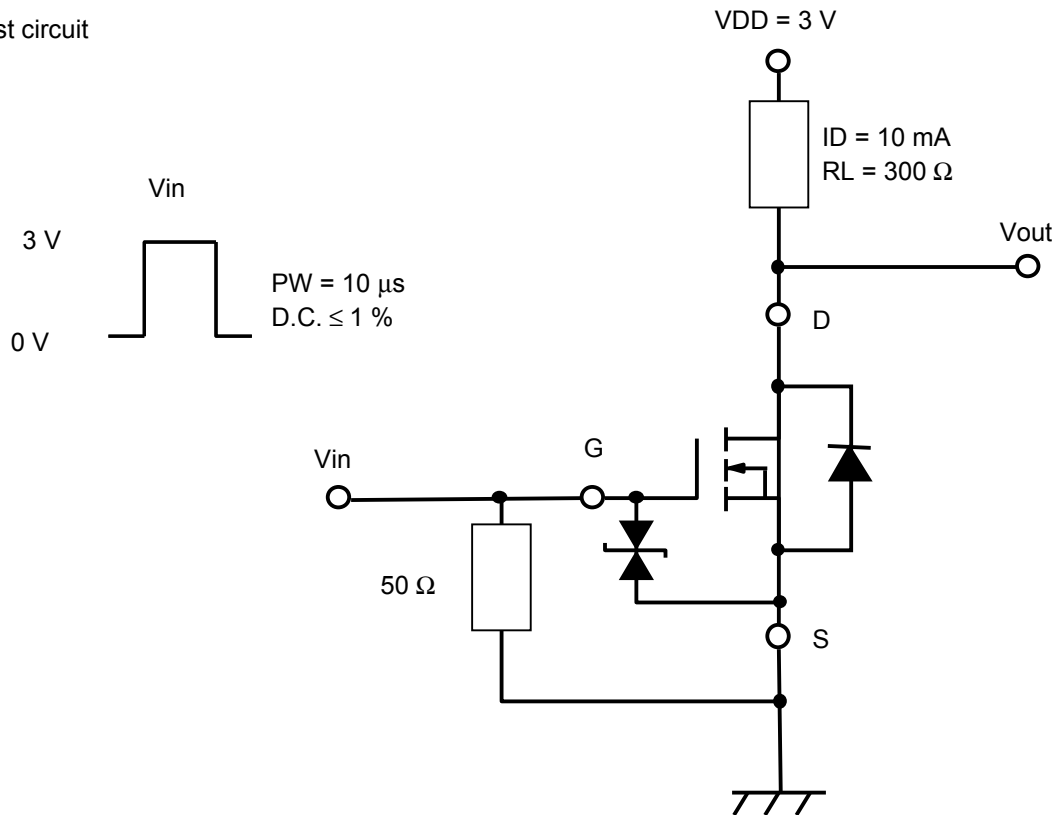
Note: Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030 Measuring methods for transistors.

*3 Pulse measurement

*4 See Test circuit.

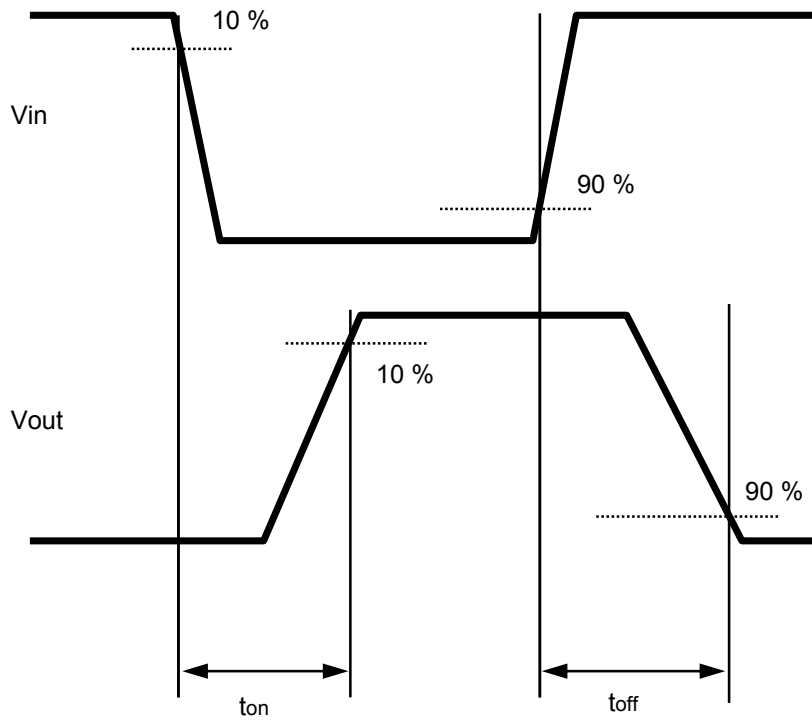
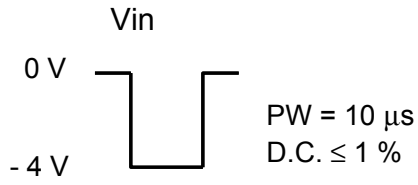
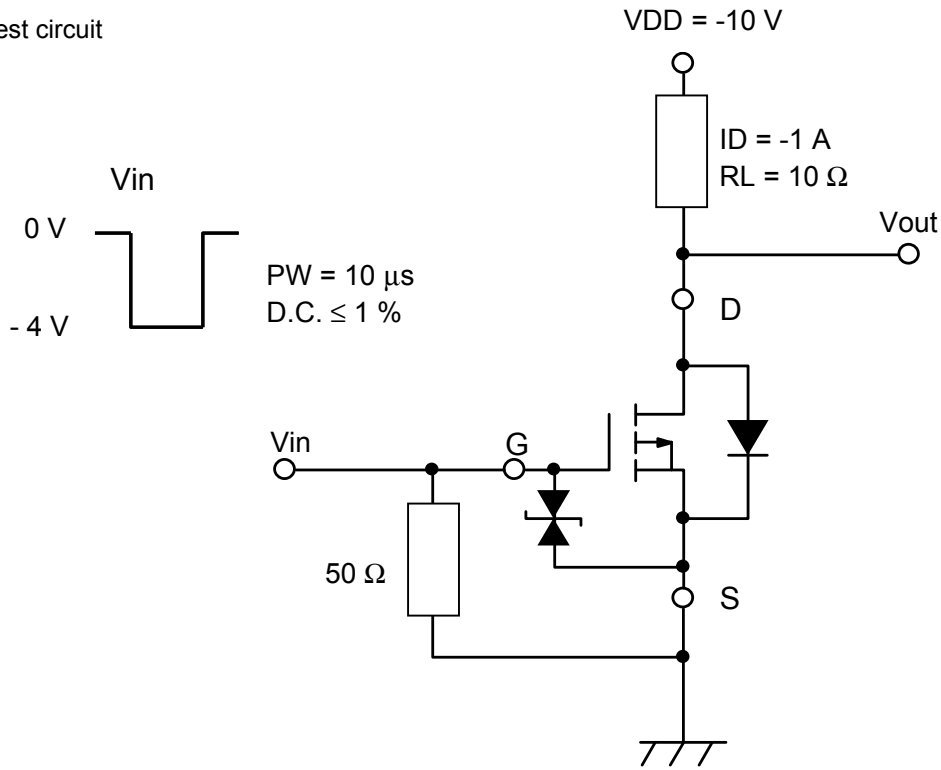
FET1(Nch.)

*2 Test circuit

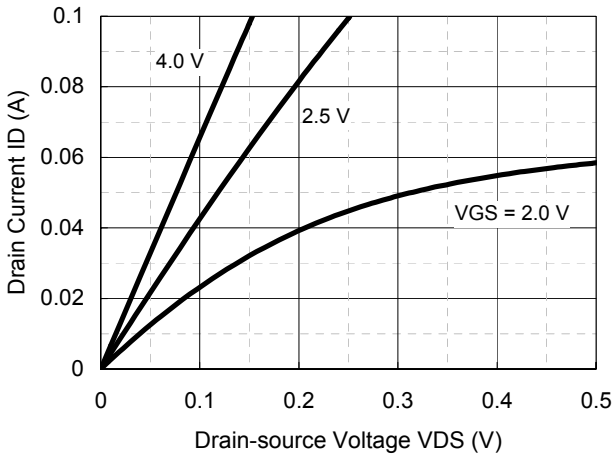


FET2(Pch.)

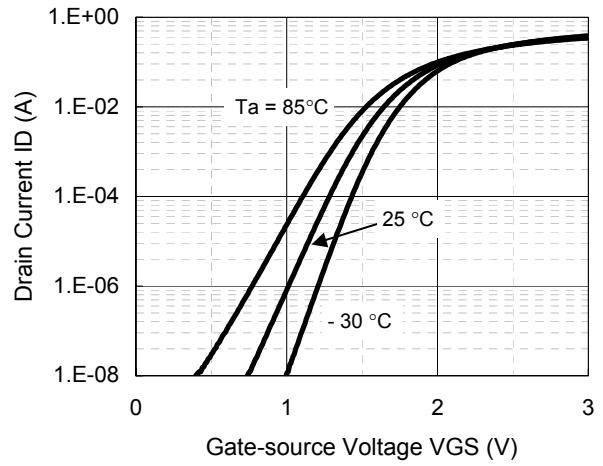
*4 Test circuit



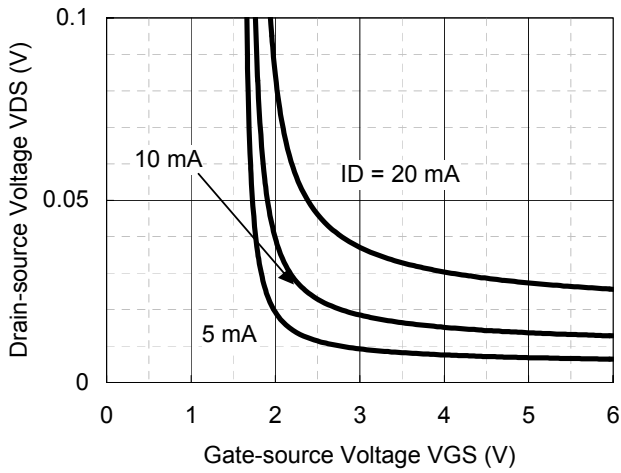
FET1(Nch.)



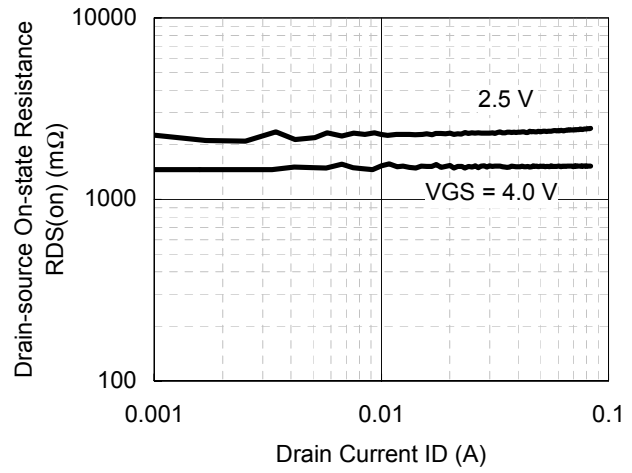
ID - VDS



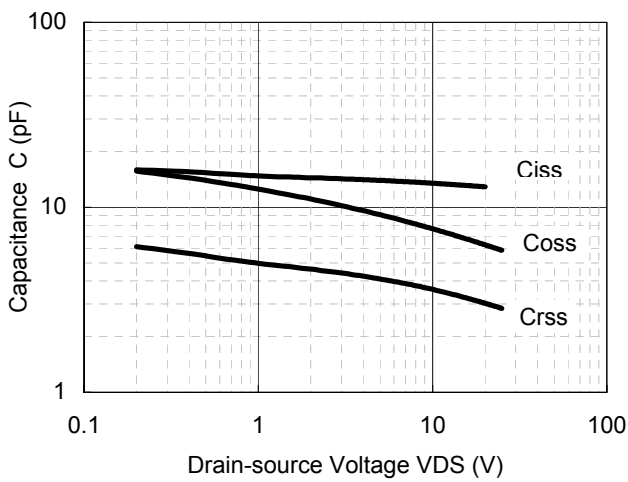
ID - VGS



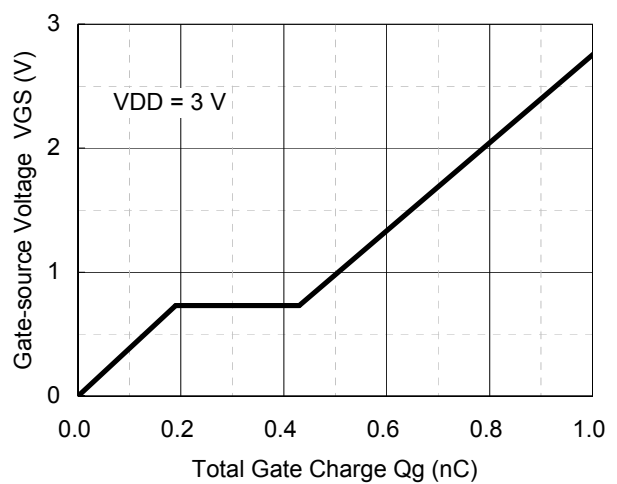
VDS - VGS



RDS(on) - ID

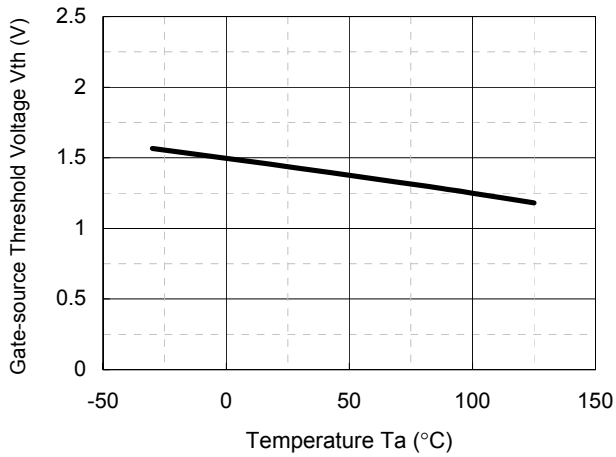


Capacitance - VDS

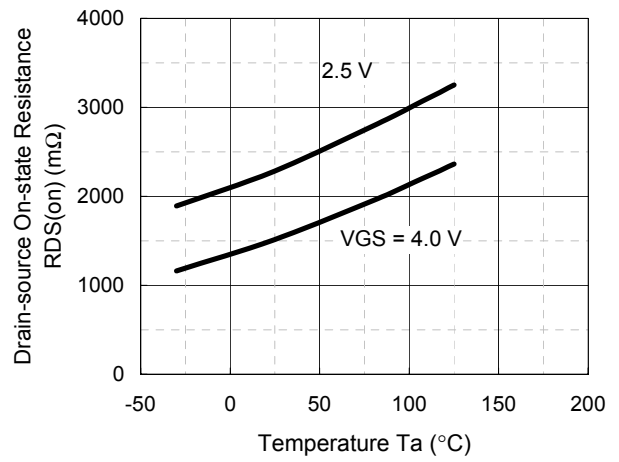


Dynamic Input/Output Characteristics

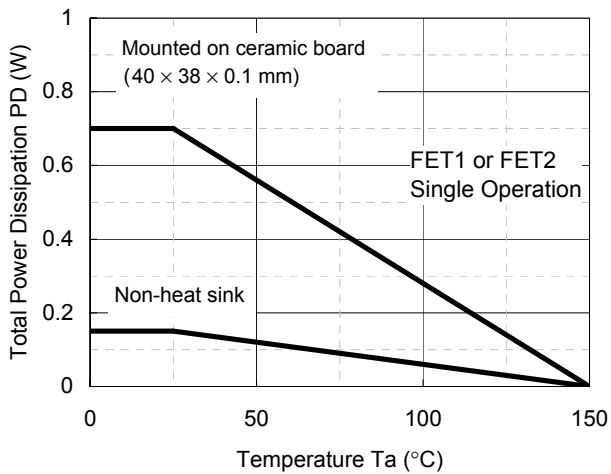
FET1(Nch.)



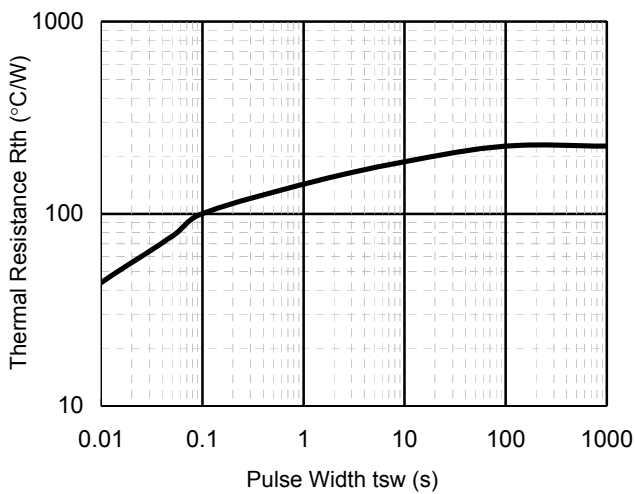
$V_{th} - T_a$



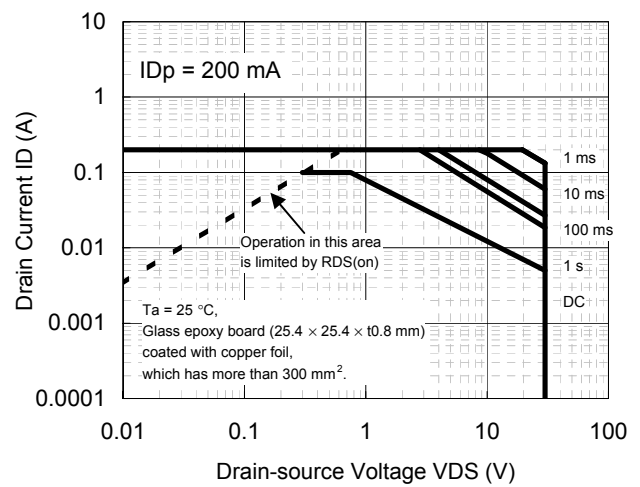
$R_{DS(on)} - T_a$



$P_D - T_a$

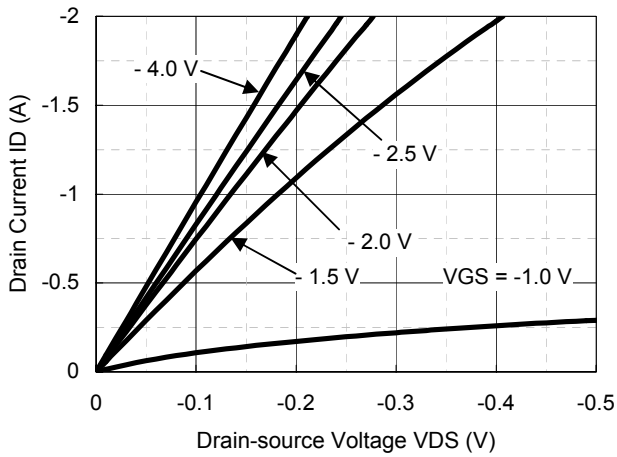


$R_{th} - t_{sw}$

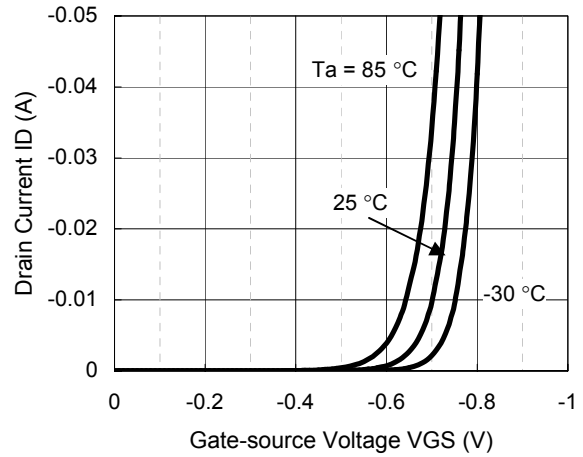


Safe Operating Area

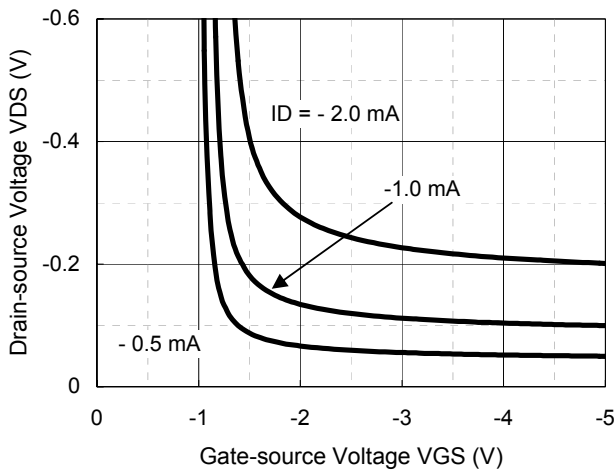
FET2(Pch.)



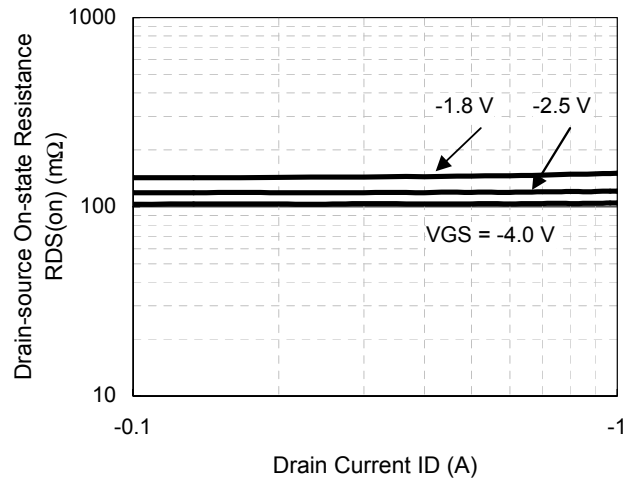
ID - VDS



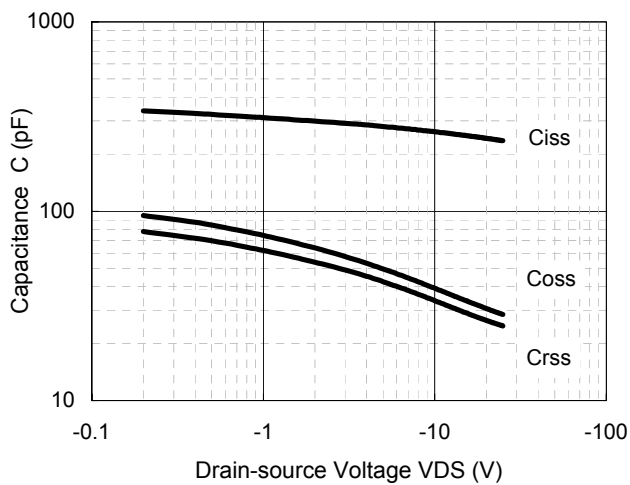
ID - VGS



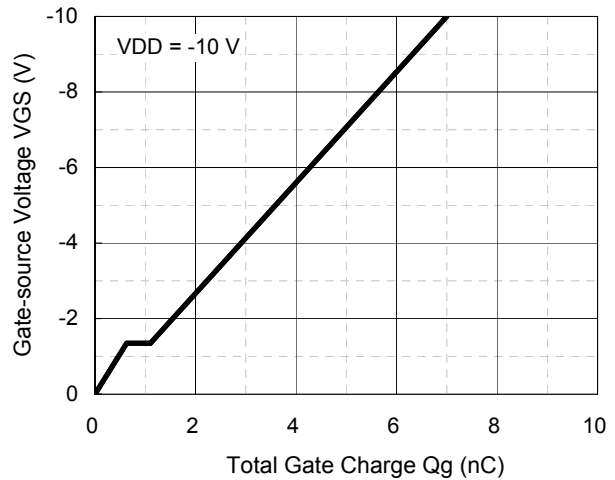
VDS - VGS



RDS(on) - ID

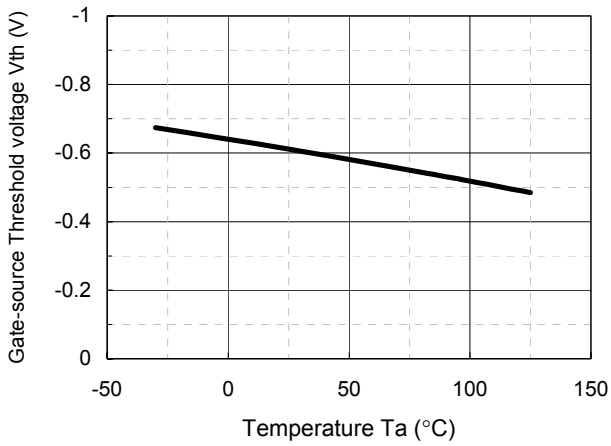


Capacitance - VDS

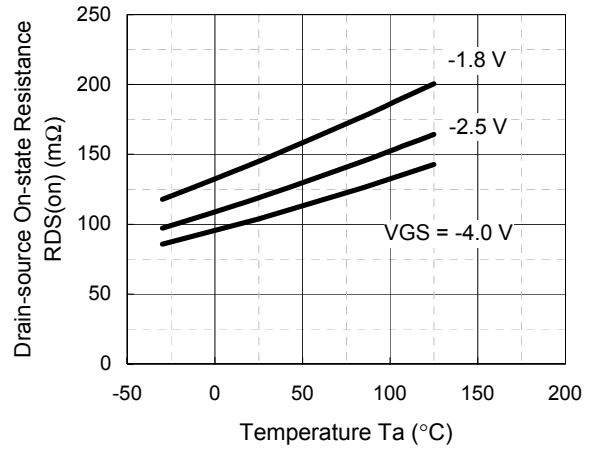


Dynamic Input/Output Characteristics

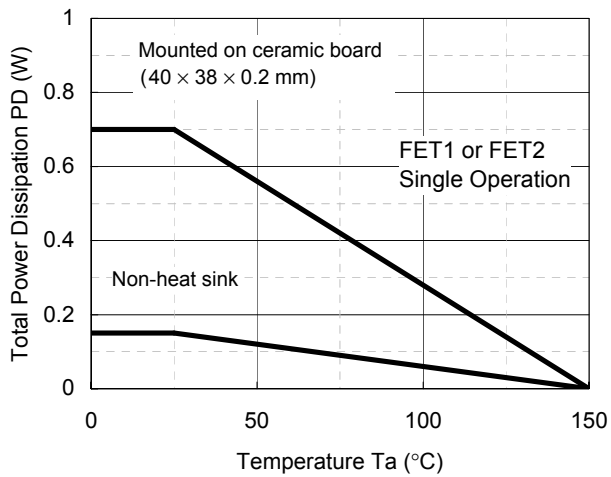
FET2(Pch.)



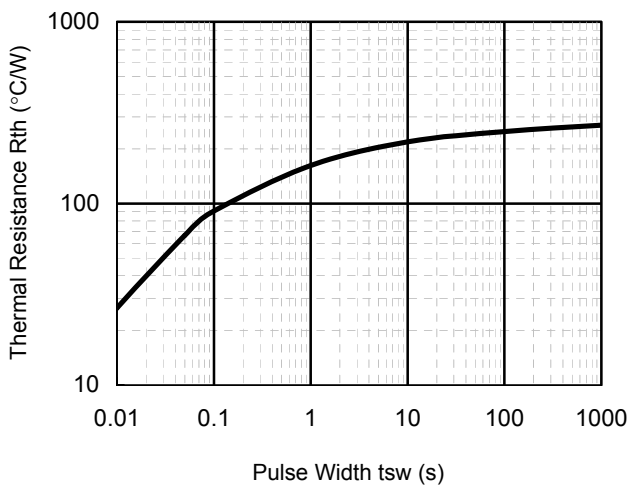
$V_{th} - T_a$



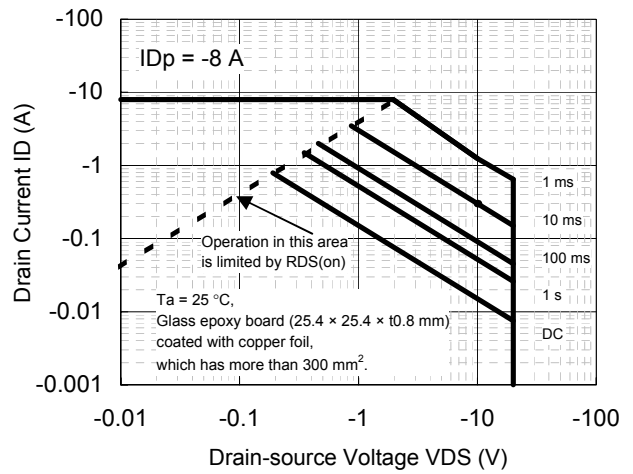
$R_{DS(on)} - T_a$



$P_D - T_a$



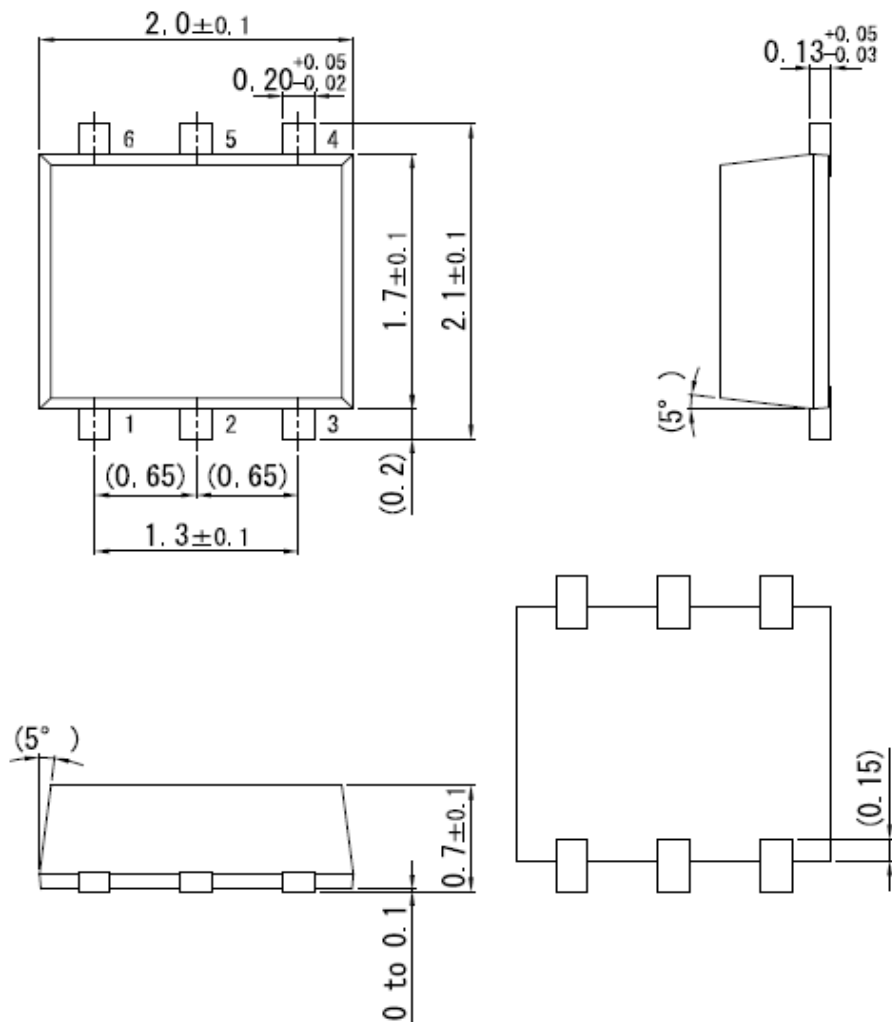
$R_{th} - t_{sw}$



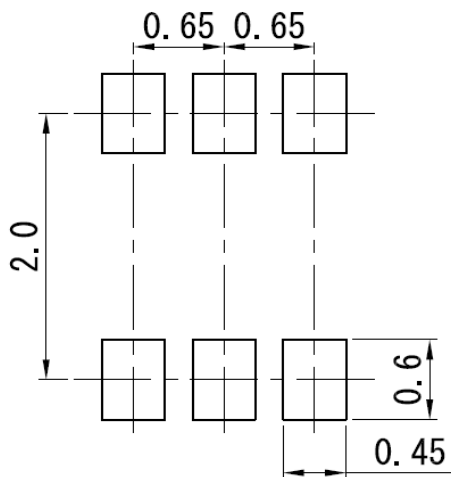
Safe Operating Area

WSMini6-F1-B

Unit: mm



■ Land Pattern (Reference) (Unit: mm)



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