

## FJ4B01110L1

## Single P-channel MOS FET

For Load switching circuits

### ■ Features

- Drain-source ON resistance:  $R_{ds(on)}$  typ. = 141 m $\Omega$  ( VGS = -2.5 V )
- CSP (Chip Size Package)
- RoHS compliant (EU RoHS / MSL:Level 1 compliant)

### ■ Marking Symbol: 1E

### ■ Packaging

Embossed type (Thermo-compression sealing) : 1 000 pcs / reel (standard)

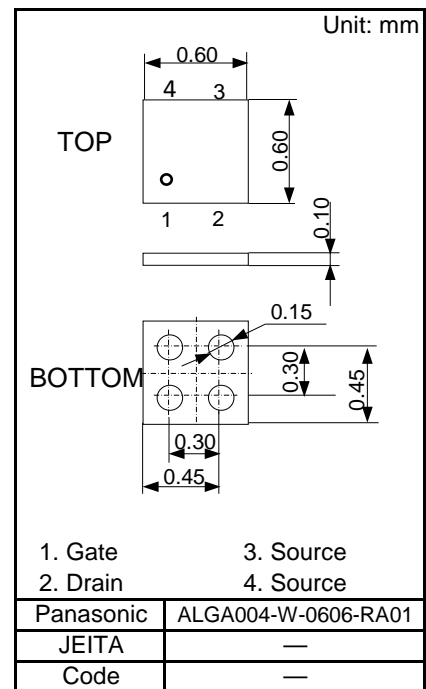
### ■ Absolute Maximum Ratings Ta = 25 °C

Parameter	Symbol	Rating	Unit
Drain-Source Voltage	VDS	-12	V
Gate-Source Voltage	VGS	$\pm 8$	V
Drain Current	ID1 <sup>*1</sup>	-1.4	A
	ID2 <sup>*2</sup>	-2.2	
	ID3 <sup>*3</sup>	-2.6	
Peak Drain Current	IDp1 <sup>*1*4</sup>	-11	A
	IDp2 <sup>*2*4</sup>	-17	
	IDp3 <sup>*3*4</sup>	-20	
Power Dissipation	PD1 <sup>*1</sup>	0.34	W
	PD2 <sup>*2</sup>	0.76	
	PD3 <sup>*3</sup>	1.1	
Channel Temperature	Tch	150	°C
Operating Ambient Temperature	Topr	-40 ~ +85	°C
Storage Temperature	Tstg	-55 ~ +150	°C

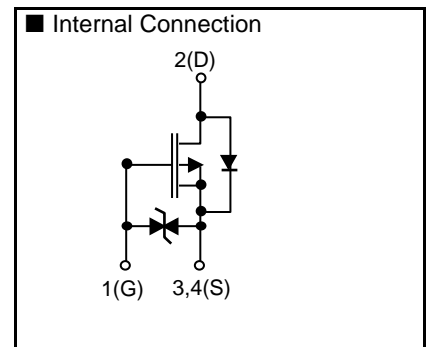
Note \*1 FR4 board (25.4mmx25.4mmx1.0mm), Min Cu 36mm<sup>2</sup> Copper

\*2 FR4 board (25.4mmx25.4mmx1.0mm), Full Cu

\*3 Ceramic substrate (70mmx70mmx1.0mm)

\*4 t = 10  $\mu$ s, Duty Cycle < 1%

### ■ Internal Connection



**■ Electrical Characteristics** Ta = 25 °C ± 3 °C

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	VDSS	ID = -1 mA, VGS = 0	-12			V
Zero Gate Voltage Drain Current	IDSS	VDS = -12 V, VGS = 0			-10	μA
Gate-Source Leakage Current	IGSS	VGS = ±8 V, VDS = 0 V			±10	μA
Gate Threshold Voltage	Vth	ID = -0.598 mA, VDS = -10 V	-0.3		-1.0	V
Drain-Source ON Resistance	RDS(on)	ID = -0.7 A, VGS = -4.5 V		118	153	mΩ
		ID = -0.7 A, VGS = -2.5 V		141	183	
		ID = -0.2 A, VGS = -1.8 V		169	287	
		ID = -0.1 A, VGS = -1.5 V		199	597	
Input Capacitance <sup>*1</sup>	Ciss	VDS = -10 V		226		pF
Output Capacitance <sup>*1</sup>	Coss	VGS = 0		62		
Reverse Transfer Capacitance <sup>*1</sup>	Crss	f = 1MHz		51		
Turn-on delay time <sup>*1,*2</sup>	td(on)	VDD = -6 V VGS = 0 to -4.5 V ID = -1.0 A		3.8		
Rise time <sup>*1,*2</sup>	tr			2.5		
Turn-off delay time <sup>*1,*2</sup>	td(off)			30		
Fall time <sup>*1,*2</sup>	tf			5.4		
Total Gate Charge <sup>*1</sup>	Qg	VDD = -6 V		3.3		nC
Gate to Source Charge <sup>*1</sup>	Qgs	VGS = -4.5 V		0.55		nC
Gate to Drain Miller Charge <sup>*1</sup>	Qgd	ID = -1.0 A		0.65		nC
Body Diode Forward Voltage	VF(D-S)	IF = -0.2A, VGS = 0V		-0.7	-1.2	V

Note Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030 Measuring methods for transistors.

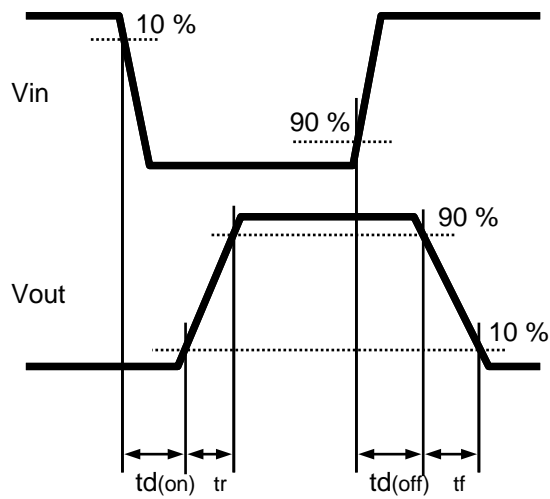
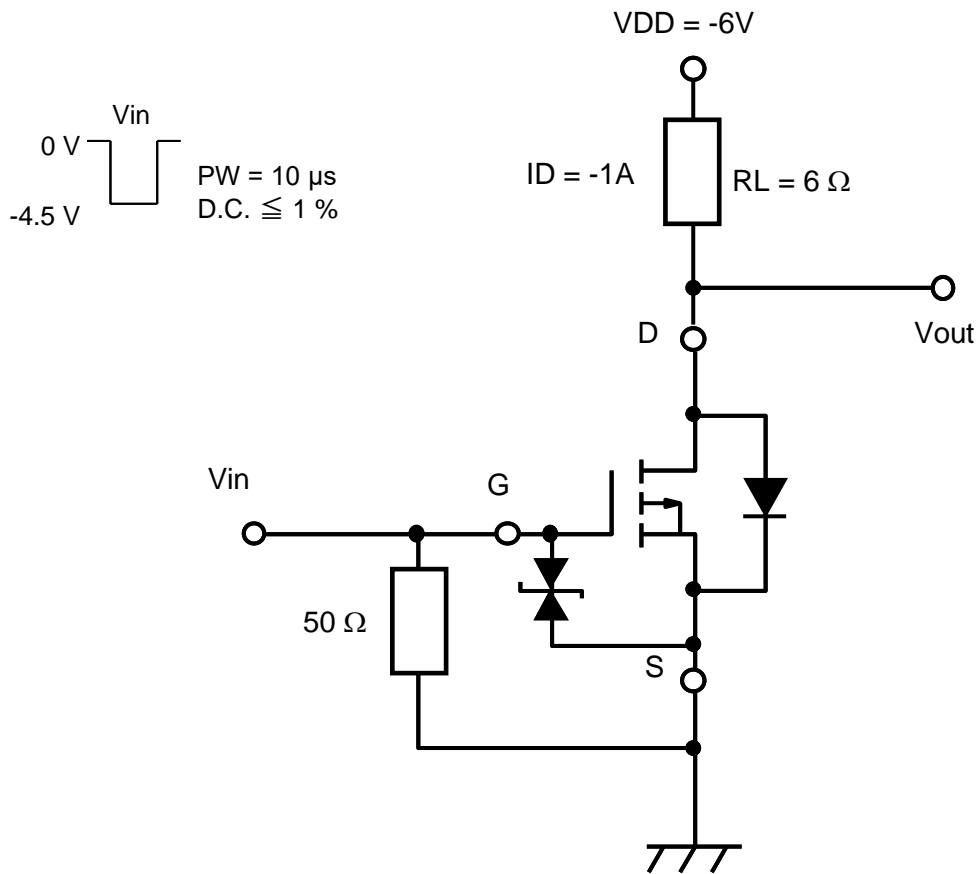
\*1 Guaranteed by design, not subject to production testing

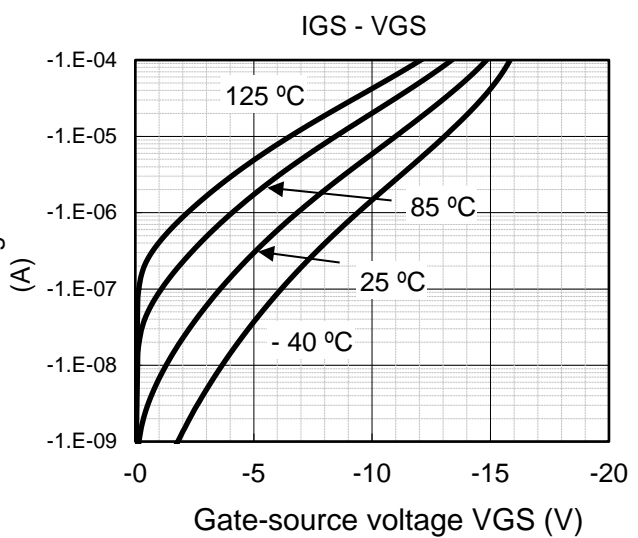
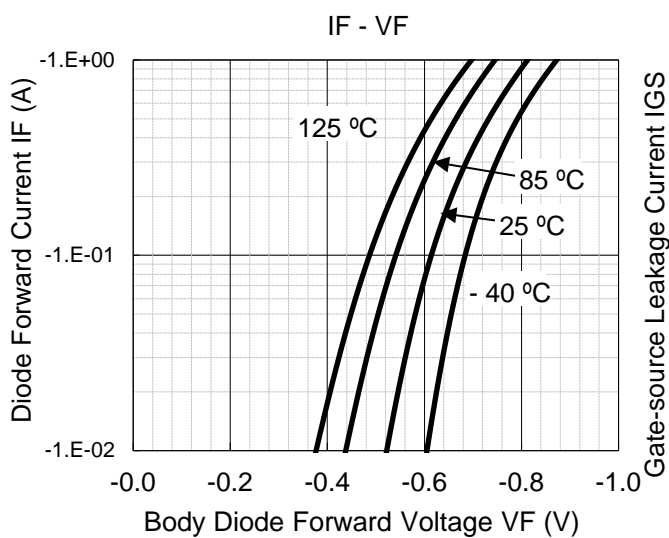
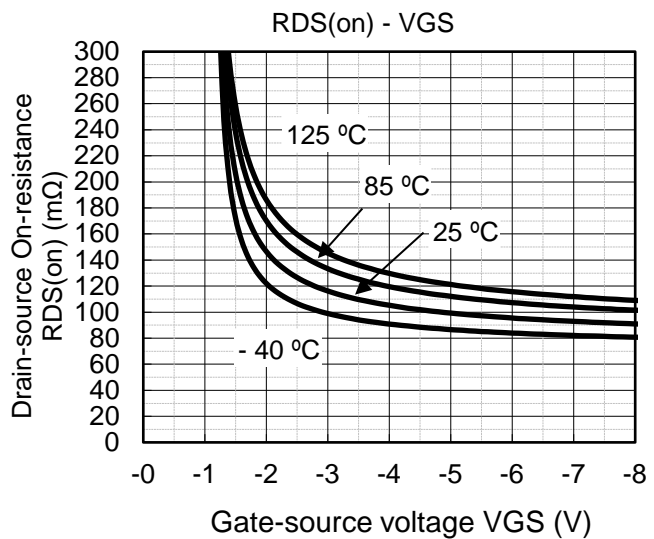
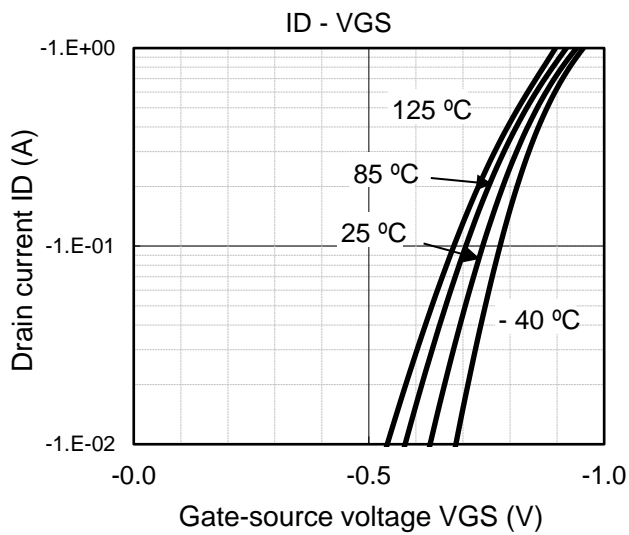
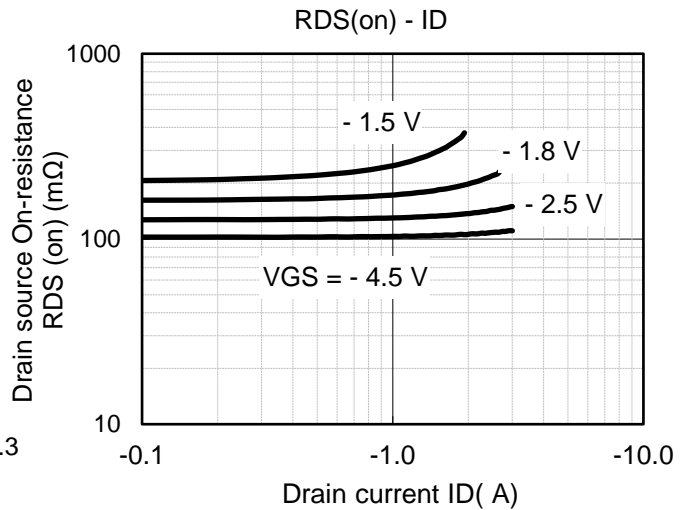
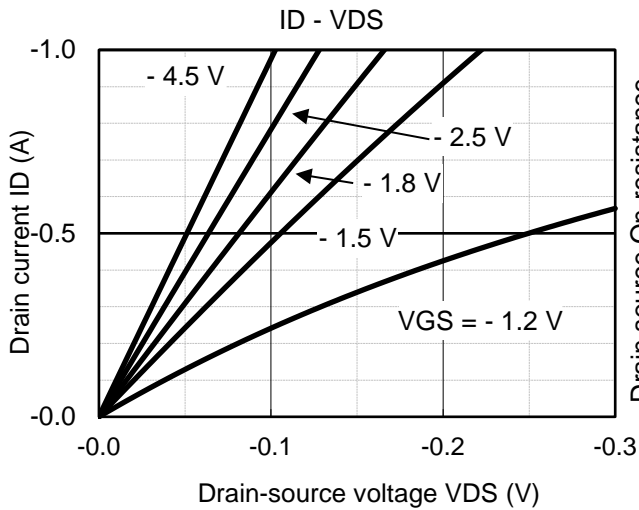
\*2 Measurement circuit for Turn-on delay time / Rise time / Turn-off delay time / Fall time

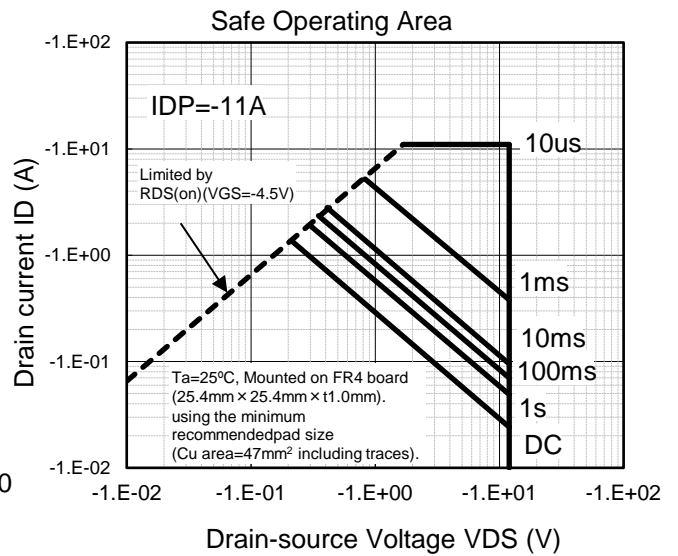
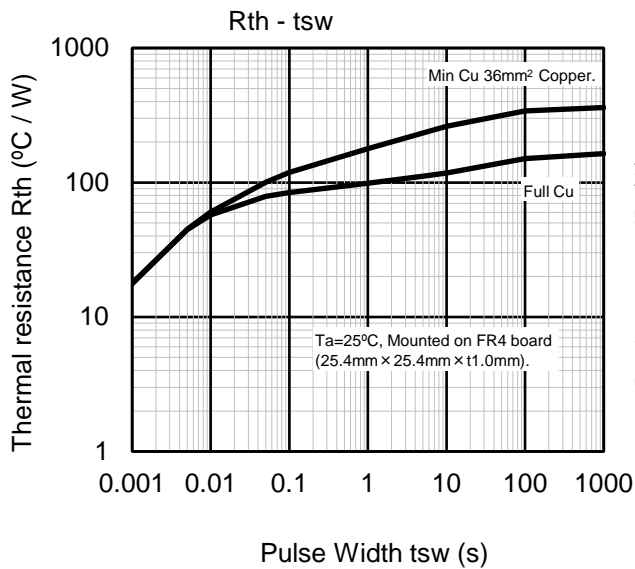
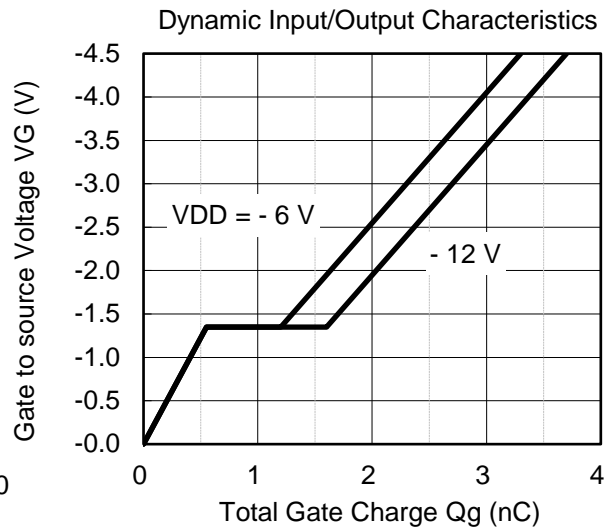
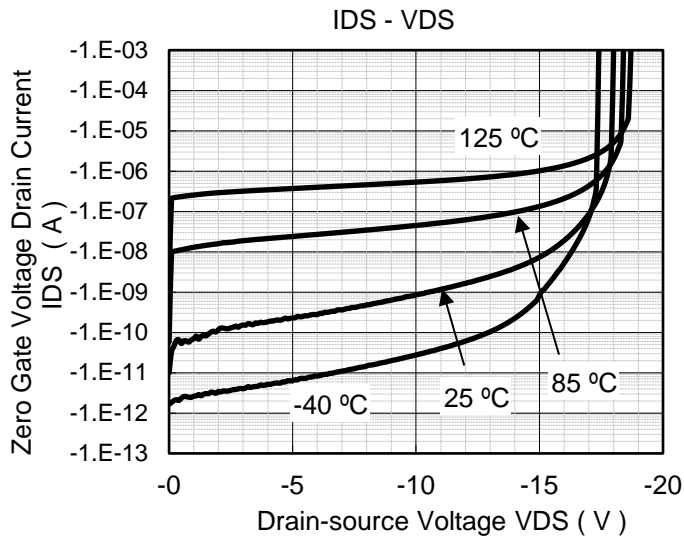
**■ Electrical State Discharge Characteristics**

Standard	Test Type	Symbol	Conditions	Class	Value	Unit
AEC-Q101-001	Human body model	HBM	C = 100 pF, R = 1.5 kΩ	H1B	>500 to ≤ 1k	V
	Machine model	MM	C = 200 pF, R = 0 Ω	M1B	>50 to ≤ 100	V

Note2: Measurement circuit

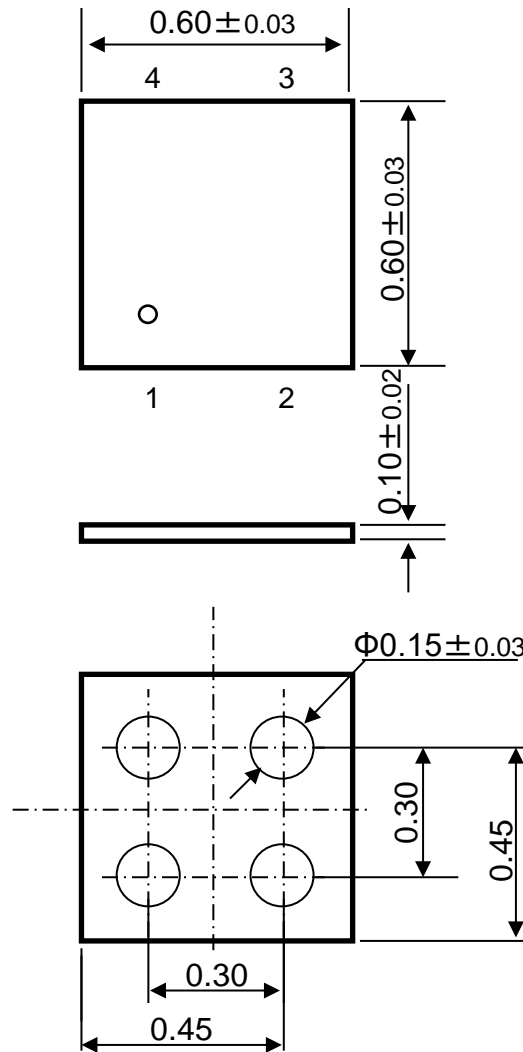




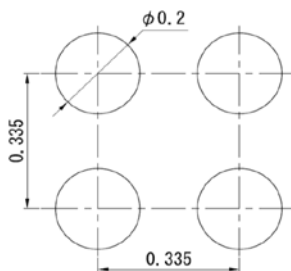


■ ALGA004-W-0606-RA01

Unit: mm



■ Land Pattern (Reference)



单击下面可查看定价，库存，交付和生命周期等信息

[>>Panasonic\(松下\)](#)