Notification about the transfer of the semiconductor business

The semiconductor business of Panasonic Corporation was transferred on September 1, 2020 to Nuvoton Technology Corporation (hereinafter referred to as "Nuvoton"). Accordingly, Panasonic Semiconductor Solutions Co., Ltd. became under the umbrella of the Nuvoton Group, with the new name of Nuvoton Technology Corporation Japan (hereinafter referred to as "NTCJ").

In accordance with this transfer, semiconductor products will be handled as NTCJ-made products after September 1, 2020. However, such products will be continuously sold through Panasonic Corporation.

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※ Except below description page
“Request for your special attention and precautions in using the technical information and semiconductors described in this book”

Nuvoton Technology Corporation Japan

Panasonic

MIP2P4HMTSCF

Type	Silicon MOSFET type Integrated Circuit		
Application	For Switching Power Supply Control		
Structure	Bi-CMOS type		
Equivalent Circuit	Figure 7		
Package	DIP7-A1-B	Marking	MIP2P4H

A. ABSOLUTE MAXIMUM RATINGS （Ta=25±3℃）

No.	Item	Symbol	Ratings	Unit	Note
1	Drain Voltage	VD	−0.3 ～ 700	V	
2	VCC Voltage	VCC	−0.3 ～ 45	V	
3	VDD Voltage	VDD	−0.3 ～ 8	V	
4	Feedback Voltage	VFB	−0.3 ～ 8	V	
5	LS Voltage	VLS	−0.3 ～ 8	V	
6	Output Peak Current	IDP	2.4 (※1)	A	※1: It is guaranteed within the Minimum-On Pulse Width[MIN(PW)]
7	Junction Temperature	Tj	150	℃	
8	Storage Temperature	Tstg	−55 ～ +150	℃	

B. RECOMMENDED OPERATING CONDITIONS

No.	Item	Symbol	Ratings	Unit	Note
1	Junction Temperature	Tj	−40 ～ +125	℃	

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C. ELECTRICAL CHARACTERISTICS Measurement Condition (Ta=25℃±3℃)

No.	Item	Symbol	Measurement Condition (Figure 1)	Typ.	Min.	Max.	Unit
【CONTROL FUNCTIONS】*Design Guaranteed Items, **Reference Items							
1	Output Frequency at heavy load pwm	f_pwm(H)	VCC=15 V, VDD=open, IFB=−20 μA, VLS =2 V, VD=5 V *Figure 5	100	93	107	kHz
2	Output Frequency at light load pwm	f_pwm(L)	VCC=15 V, VDD=open, IFB=IFB1+5 μA, VLS =2 V, VD=5 V *Figure 5	28	22	34	kHz
**3	Jitter Frequency Deviation at heavy load pwm	⊿f(H)	VCC=15 V, VDD=open, IFB=−20 μA, VLS =2 V, VD=5 V *Figure 2	5.5	−	−	kHz
**4	Jitter Frequency Deviation at light load pwm	⊿f(L)	VCC=15 V, VDD=open, IFB=IFB1+5 μA, VLS =2 V, VD=5 V *Figure 2	1.5	−	−	kHz
**5	Jitter Frequency Modulation Rate	fM	VCC=15 V, VDD=open, IFB=−20 μA, VLS =2 V, VD=5 V *Figure 2	450	−	−	Hz
6	Maximum Duty Cycle	MAXDC	VCC=15 V, VDD=open, IFB=−20 μA, VLS =2 V, VD=5 V	56	52	60	%
7	DRAIN−VDD Charging Stop VCC Voltage	VCC1	VDD=VDD(ON)−0.1 V, VLS=2 V, VD=30 V	8.2	7.45	8.95	V
**8	DRAIN−VDD Charging Stop/Start VCC Voltage Hysteresis	D_VCC1	VDD=VDD(ON)−0.1 V, VLS=2 V, VD=30 V	0.65	−	−	V
9	VDD Start Voltage	VDD(ON)	IFB=−20 μA, VLS=2 V, VD=5 V	5.9	5.4	6.4	V
10	VDD Stop Voltage	VUV	IFB=−20 μA, VLS=2 V, VD=5 V	4.4	3.9	4.9	V
11	VDD Start/Stop Hysteresis	D_VDD	VDD(ON) − VUV	1.5	1	2	V
12	VDD Current before start	IDD(SB)	VDD=VDD(ON)−0.1 V, VLS=2 V	350	260	440	μA
13	VDD Current at standby mode	IDD(STB)	VDD=VDD(ON)+0.1 V, IFB=IFB1−2 μA, VLS =2 V, VD=5 V	550	400	700	μA
14	VDD Current at heavy load pwm	IDD(OP)H	VDD=VDD(ON)+0.1 V, IFB=−20 μA, VLS =2 V, VD=5 V	550	400	700	μA
15	VDD Current at light load pwm	IDD(OP)L	VDD=VDD(ON)+0.1 V, IFB=IFB1+5 μA, VLS =2 V, VD=5 V	590	470	700	μA
16	VDD Current at Over Load Protection	IDD(OLP)	VDD=VDD(ON)+0.1 V, VFB=VFB(OLP)+0.1 V, VLS=2 V, VD=5 V	360	270	450	μA
17	VCC Internal Circuit Current	ICC	VCC=15 V, VDD=VDD(ON)+0.6 V	27	14	40	μA
**18	Minimum VCC Voltage for VDD Supply	VCC(MIN)	VLS=2 V, VD=5 V	6.8	−	−	V

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No.	Item	Symbol	Measurement Condition (Figure 1)	Typ.	Min.	Max.	Unit
19	DRAIN-VDD Charging Current	Ich1	VCC=open, VDD=0 V, VLS =2 V, VD=50 V	−3.8	−5.7	−1.9	mA
		Ich2	VCC=open, VDD=VDDreset−0.1 V, VLS =2 V, VD=50 V	−2.8	−4.5	−1.4	mA
		Ich3	VCC=open, VDD=VDDreset+0.1 V, VLS =2 V, VD=50 V	−8.6	−13.5	−4.3	mA
		Ich4	VCC=open, VDD=VDD(ON)−0.5 V, VLS =2 V, VD=50 V	−6.5	−11	−3.25	mA
20	Feedback Threshold Current	IFB1	ON→OFF, VCC=15 V, VDD=open, VLS =2 V, VD=5 V	−140	−200	−80	μA
**21	Feedback Current Hysteresis	IFBHYS	OFF→ON, VCC=15 V, VDD=open, VLS =2 V, VD=5 V	5	−	−	μA
**22	Feedback Current at light load pwm	IFB2	VCC=15 V, VDD=open, VLS =2 V, VD=5 V	−90	−	−	μA
**23	Feedback Current at heavy load pwm	IFB3	VCC=15 V, VDD=open, VLS =2 V, VD=5 V	−45	−	−	μA
**24	Feedback Current at ILIMIT(H)	IFB4	VCC=15 V, VDD=open, VLS =2 V, VD=5 V	−30	−	−	μA
25	FB Voltage	VFB	VCC=15 V, VDD=open, IFB=−20 μA, VLS =2 V, VD=5 V	1.9	1.6	2.2	V
26	FB Voltage at light load	VFB1	VCC=15 V, VDD=open, IFB=IFB1+5 μA, VLS =2 V, VD=5 V	1.75	1.45	2.05	V
27	FB Discharge Pull-Down Resistance	RFB(OFF)	VCC=15 V, VDD=open, VFB=VFB(OLP)	480	380	580	Ω
28	FB Grounded Current	IFB(GND)	VCC=15 V, VDD=open, VFB=0 V(FB pin direct)	−460	−644	−276	μA
*29	Frequency Soft Start Time	Tsoft	VCC=15 V, VDD=open, IFB=−20 μA, VLS =2 V	5	1.5	10	ms

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No.	Item	Symbol	Measurement Condition (Figure 1)	Typ.	Min.	Max.	Unit
【CIRCUIT PROTECTIONS】 *Design Guaranteed Items, **Reference Items							
30	Self Protection Current Limit	ILIMIT(H)	VCC=15 V, VDD=open, IFB=−20 μA, VLS=2 V, Ton=3 μs *Figure 4	0.7	0.651	0.749	A
**31	ILIMIT(H) Compensation Slope	R_slope	VCC=15 V, VDD=open, IFB=−20 μA, VLS=2 V, Ton=3 μs/2 μs *Figure 4	8	−	−	mA/μs
**32	Drain Current at PFM	ILIMIT(L)	VCC=15 V, VDD=open, IFB=IFB2+20 μA, VLS=2 V, Ton=3 μs *Figure 5	0.52	−	−	A
**33	Drain Current at light load	ID(OFF)	VDD=VDD(ON)+0.1 V, IFB=IFB1+5 μA, VLS=2 V, Ton=3 μs *Figure 5	160	−	−	mA
**34	Jitter Drain Current Deviation at light load	D_ID(OFF)	VDD=VDD(ON)+0.1 V, IFB=IFB1+5 μA, VLS=2 V, Ton=3 μs *Figure 5	30	−	−	mA
35	Minimum On-Pulse Width	MIN(PW)		620	−	730	ns
*36	Leading Edge Blanking Delay	ton(BLK)		420	350	510	ns
**37	Over Current Protection Delay	td(OCL)		200	−	−	ns
38	VCC Over Voltage Latch Stop Voltage	VCC(OV)	VDD=open, IFB=−20 μA, VLS =2 V, VD=5 V	29	26	32	V
39	VDD Over Voltage Latch Stop Voltage	VDD(OV)	IFB=−20 μA, VLS =2 V, VD=5 V	6.5	5.8	7.2	V
40	VDD Over Voltage Latch Stop Voltage Hysteresis	D_VDD(OV)	VDD(OV)−VDD(ON)	0.6	0.1	1.1	V
41	VDD Over Voltage Latch Stop Current	IDD(OV)	IFB=−20 μA, VLS =2 V, VD=5 V	3.4	2.3	4.6	mA
**42	Latch Stop Filter Time	Td(LAT)		150	−	−	μs
**43	OLP Internal Filter Time	Td(OLP)		10	−	−	μs
44	VDD Clamp Current	IDD(CLP)	VDD=8 V, VLS =2 V, VD=5 V	32	25	47	mA
45	FB Over Load Protection detect Current	IFB(OLP)	VCC=15 V, VDD=open, VFB=3 V, VLS =2 V, VD=5 V	−8	−10	−6	μA
46	FB Over Load Protection detect Voltage	VFB(OLP)	VCC=15 V, VDD=open, VLS =2 V, VD=5 V	4.4	3.9	4.9	V
47	OLP VDD Oscillation Count	OLP_CNT	VDD=VUV ⇔ VDD(ON), IFB=−20 μA, VLS =2 V, VD=5 V * Figure 3	8			−

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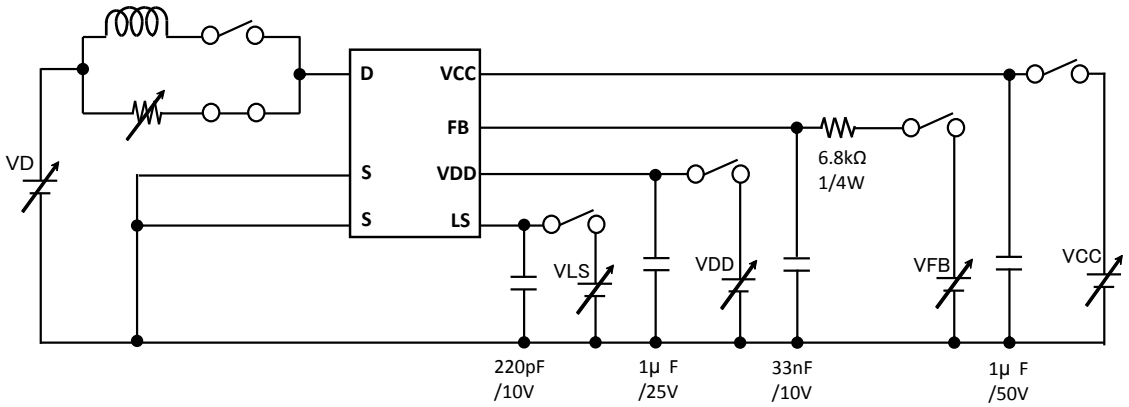
No.	Item	Symbol	Measurement Condition (Figure 1)	Typ.	Min.	Max.	Unit
48	LS Start Voltage	VLS(UV)H	VCC=15 V, VDD=open, IFB=−20 μA, VD=5 V	1.25	1.14	1.36	V
49	LS Stop Voltage	VLS(UV)L	VCC=15 V, VDD=open, IFB=−20 μA, VD=5 V	0.9	0.82	0.98	V
**50	LS Start/Stop Voltage Hysteresis	D_VLS(UV)	VLS(UV)H − VLS(UV)L	0.35	−	−	V
51	LS Stop Filter Time	Td(LS)	VCC=15 V, VDD=open, VFB=3 V, VLS < VLS(UV)L, VD=5 V	32	22	50	ms
*52	Thermal Shutdown Temperature	TOTP		140	130	150	℃
**53	Thermal Shutdown Temperature Hysterisis	D_TOTP		45	−	−	℃
54	Reset VDD Threshold Voltage	VDDreset		2.7	1.8	3.5	V
【OUTPUT】 **Reference Items							
55	ON−State Resistance	RDS(ON)	VCC=15 V, VDD=open, IFB=−20 μA, VLS=2 V, ID=300 mA	5.8	−	7.0	Ω
56	Drain OFF−State Leakage Current	IDSS	VCC=VCC(OV)→15 V, VDD=open, VLS=2 V, VD=650 V	5	−	20	μA
57	Drain Breakdown Voltage	VDSS	VCC=VCC(OV)→15 V, VDD=open, VLS=2 V, ID=100 μA	−	700	−	V
**58	Rise Time	tr	VCC=15 V, VDD=open, IFB=−20 μA, VLS=2 V, VD=5 V *Figure 6	110	−	−	ns
**59	Fall Time	tf	VCC=15 V, VDD=open, IFB=−20 μA, VLS=2 V, VD=5 V *Figure 6	25	−	−	ns
【SUPPLY VOLTAGE】							
60	Minimum Drain Supply Voltage	VD(MIN)	VCC=open, VDD=open, IFB=−20 μA, VLS=2 V ※VD for starting operation	10	−	18	V

【Figure 1: Measurement Circuit】



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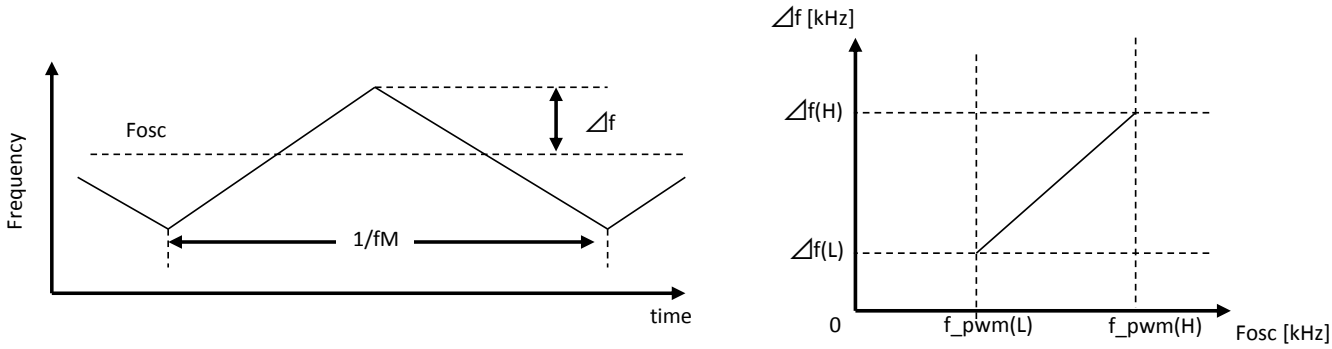
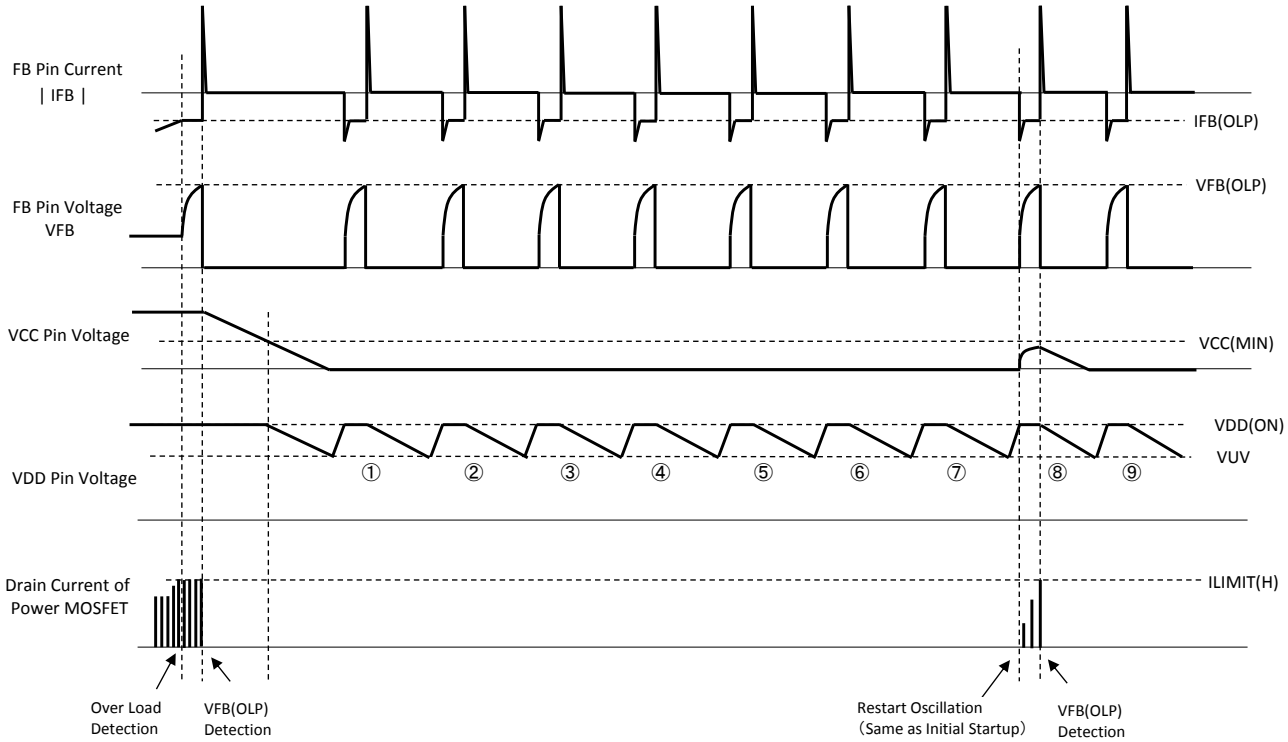
【Figure 2: Δf, fM Measurement】



【Figure 3: Terminal Waveforms during Over-Load Protection】



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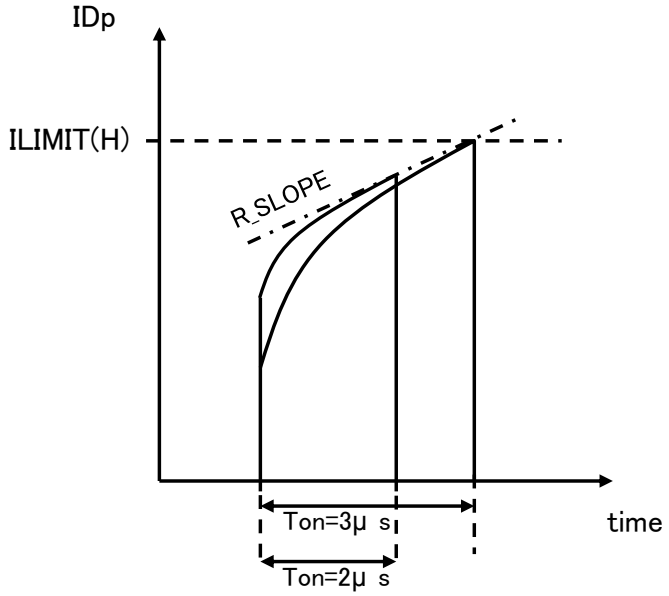
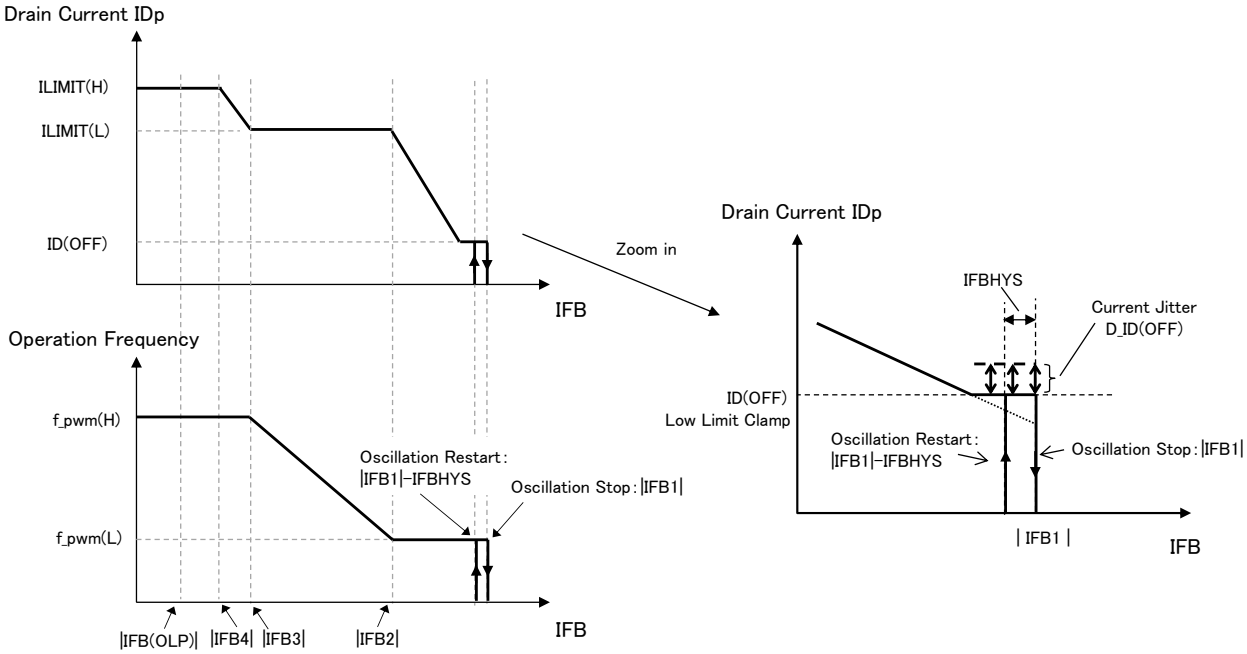
【Figure 4: ILIMIT、R_slope Measurement】

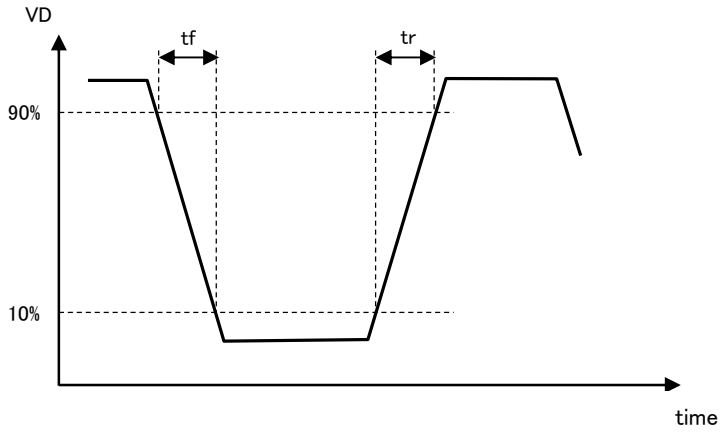


R_slope ; {(ILIMIT(H) at Ton=3μs) − (ILIMIT(H) at Ton=2μs)} / {(Ton=3μs) − (Ton=2μs)}

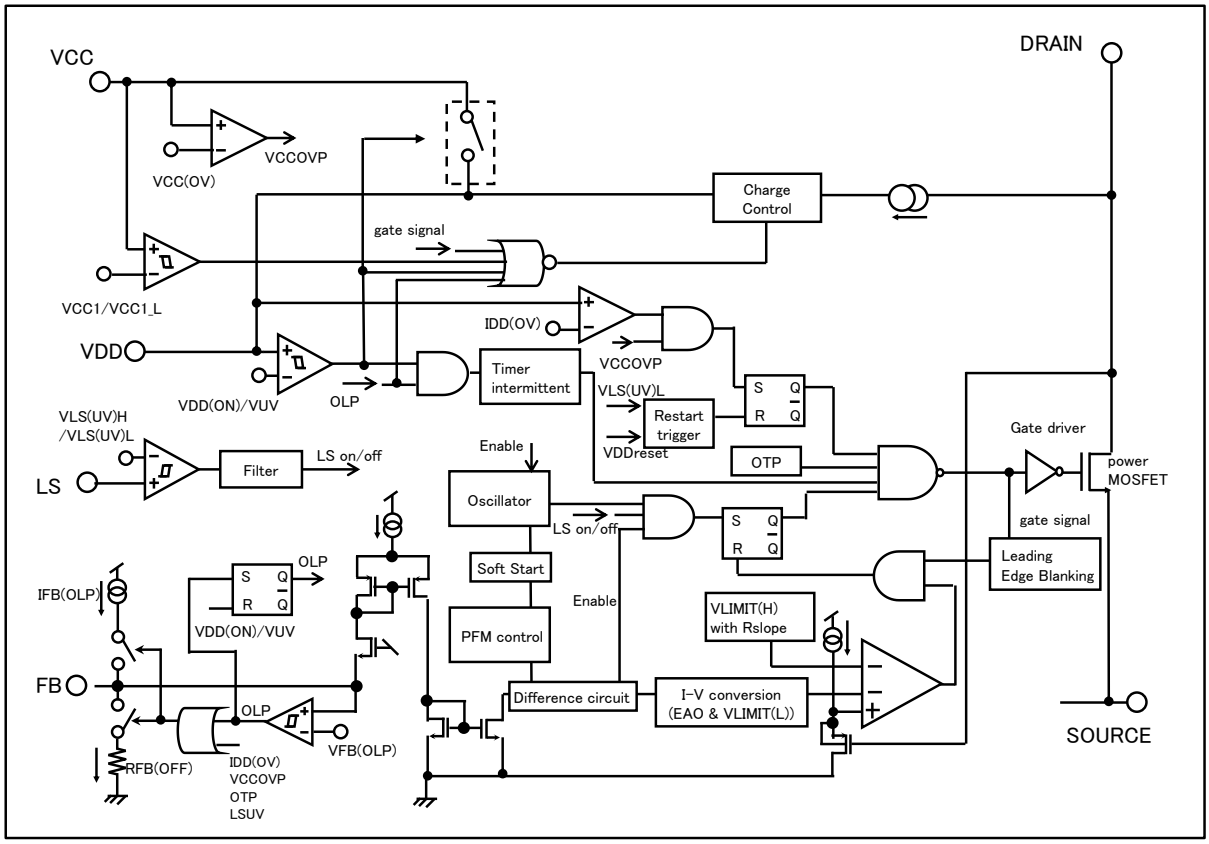
【Figure 5: IFB-ILIMIT, IFB-FOSC Characteristics】



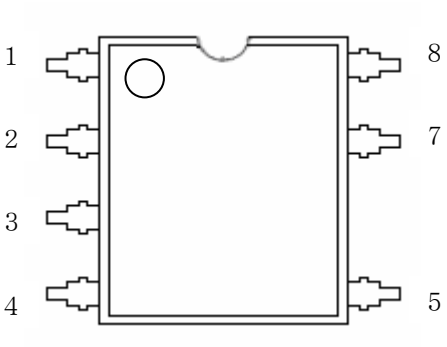
【Figure 6: tr, tf Measurement】



【Figure 7: Block Diagram】



【Figure 8: Pin Layout】



No.	Pin Name
1	LS
2	VDD
3	FB
4	VCC
5	DRAIN
6	—
7	SOURCE
8	SOURCE

【Precautions for Use 1】

Connect a ceramic capacitor (over 0.1 μF) between VDD pin and SOURCE pin.

【Precautions for Use 2】

Do pay attention to below as IPD has risks of smoking or igniting when subjected to below abnormal conditions especially during regulatory Safety Standard testing.

An example of safety measure to avoid smoking or ignition is adding fuse at the input side or connect zener diode between control pin and GND as a precaution.

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(1) DRAIN Pin and LS Pin invert insertion in power supply board.
(2) DRAIN pin short to LS pin.
(3) DRAIN pin short to VDD pin.
(4) DRAIN pin short to FB pin.
(5) DRAIN pin short to VCC pin.
(6) VCC pin short to LS pin.
(7) VCC pin short to VDD pin.
(8) VCC pin short to FB pin.

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