Notification about the transfer of the semiconductor business

The semiconductor business of Panasonic Corporation was transferred on September 1, 2020 to Nuvoton Technology Corporation (hereinafter referred to as "Nuvoton"). Accordingly, Panasonic Semiconductor Solutions Co., Ltd. became under the umbrella of the Nuvoton Group, with the new name of Nuvoton Technology Corporation Japan (hereinafter referred to as "NTCJ").

In accordance with this transfer, semiconductor products will be handled as NTCJ-made products after September 1, 2020. However, such products will be continuously sold through Panasonic Corporation.

Publisher of this Document is NTCJ.
If you would find description “Panasonic” or “Panasonic semiconductor solutions”, please replace it with NTCJ.

※ Except below description page
“Request for your special attention and precautions in using the technical information and semiconductors described in this book”

Nuvoton Technology Corporation Japan

Panasonic

MIP3550MTSCF

Type	Silicon MOSFET type Integrated Circuit		
Application	For Switching Power Supply Control		
Structure	CMOS type		
Equivalent Circuit	See Fig. 9		
Package	DIP7-A1-B	Marking	MIP355

A. ABSOLUTE MAXIMUM RATINGS (Ta=25℃±3℃)

NO.	Item	Symbol	Ratings	Unit	Note
1	DRAIN Voltage	VD	−0.3 ～ 700	V	※1 : It is guaranteed within the pulse as below. Leading Edge Blanking Pulse + Current Limit Delay ton(BLK)+td(OCL)
2	VDD Voltage	VDD	−0.3 ～ 8	V	
3	Feedback Voltage	VFB	−0.3 ～ 6	V	
4	Feedback Current	IFB	500	uA	
5	f Voltage	Vf	−0.3 ～ 8	V	
6	CL Voltage	VCL	−0.3 ～ 8	V	
7	Output Peak Current	IDP	3(※1)	A	
8	Channel Temperature	Tch	150	℃	
9	Storage Temperature	Tstg	−55 ～ +150	℃	

B. ELECTRICAL CHARACTERISTICS

Measure Condition (TC=25℃±3℃)

No.	Item	Symbol	Measure Condition (See Fig. 1)	Typ.	Min.	Max.	Unit
【CONTROL FUNCTIONS】*Design Guarantee Item							
1	Output Frequency	fosc	VD=5V, VDD=VDD(ON)+0.1V, IFB=30uA, Vf=VDD, VCL=0V, after dis_OLP *Refer Fig.3	43.5	39	48	kHz
2	Jitter Frequency Deviation	Δf	VD=5V, VDD=VDD(ON)+0.1V, IFB=30uA, Vf=VDD, VCL=0V, after dis_OLP *Refer Fig.3	3	1.2	4.8	kHz
*3	Jitter Frequency Modulation Rate	fM	VD=5V, VDD=VDD(ON)+0.1V, IFB=30uA, Vf=VDD, VCL=0V, after dis_OLP *Refer Fig.3	150	–	–	Hz
4	Maximum Duty Cycle	MAXDC	VD=5V, VDD=VDD(ON)+0.1V, IFB=30uA, Vf=VDD, VCL=0V, after dis_OLP	70	65	75	%
5	VDD Start Voltage	VDD(ON)	VD=5V, IFB=30uA, VCL=0V, Vf=VDD	5.9	5.4	6.4	V
6	VDD Stop Voltage	VDD(OFF)	VD=5V, IFB=30uA, VCL=0V, Vf=VDD	4.9	4.4	5.4	V
7	VDD Hysteresis	VDDHYS	VDD(ON)-VDD(OFF)	1.0	0.5	1.5	V

No.	Item	Symbol	Measure Condition (See Fig. 1)	Typ.	Min.	Max.	Unit
8	VDD Clamp Voltage	VDD(CLP)	IDD=10mA	7.4	6.9	7.9	V
9	Feedback Threshold Current	IFB1	ON⇒OFF, VD=5V, VDD=VDD(ON)+0.1V, Vf=VDD, VCL=0V	97	57	137	uA
10	Feedback Hysteresis Current	IFBHYS	VD=5V, VDD=VDD(ON)+0.1V, Vf=VDD, VCL=0V	2.5	–	–	uA
11	Feedback Pin Voltage	VFB1	VD=5V, VDD=VDD(ON)+0.1V, IFB=IFB1, Vf=VDD, VCL=0V	1.9	1.6	2.2	V
		VFB	VD=5V, VDD=VDD(ON)+0.1V, IFB=80uA, Vf=VDD, VCL=0V	1.8	1.5	2.1	V
12	Supply Current before start-up	IDD(SB)	VD=5V, VDD=VDD(ON)−0.2V, Vf=VDD, VCL=0V, FB:OPEN	350	170	530	uA
13	Supply Current	IDD	VD=5V, VDD=VDD(ON)+0.1V, IFB=30uA, Vf=VDD, VCL=0V	510	250	750	uA
14	Supply Current at light load	IDD(OFF)	VD=5V, VDD=VDD(ON)+0.1V, IFB=IFB1+5uA, Vf=VDD, VCL=0V	550	300	800	uA
15	VDD Charging Current	Ich1	VDD=0V, VD=40V, FB, CL, f:OPEN	−8.5	−13.6	−4.1	
		Ich2	VDD=5V, VD=40V, FB, CL, f:OPEN	−5.3	−8.5	−2.1	mA
16	f Pin Threshold Voltage	Vf1	VDD=VDD(ON)+0.1V, fosc:foscL ⇒ foscH	1.25	0.65	1.85	V
17	f Pin current before start-up	If1	VDD=VDD(ON)−0.1V, Vf=0V	−50	−70	−30	uA
18	f Pin threshold current	If2	VDD=VDD(ON)+0.1V, fosc:fosc ⇒ foscH	−29	−44	−14	uA
19	f Pin Voltage for foscH change	Vf2	VDD=VDD(ON)+0.1V, If=If2	2.3	2	2.6	V
20	f Pin Short current	If_GND	VDD=VDD(ON)+0.1V, Vf=0V	−22	−37	−7	uA
21	f Pin Voltage	Vf	VDD=VDD(ON)+0.1V, If=−50uA	2.25	1.55	2.85	V
22	CL Pin Threshold Voltage	VCL1	VDD=VDD(ON)+0.1V, ILIMIT:ILIMIT ⇒ ILIMIIT_M	1.35	0.75	1.95	V
23	CL Pin current before start-up	ICL1	VDD=VDD(ON)−0.4V, VCL=0V	−50	−70	−30	uA
24	CL Pin threshold current	ICL2	VDD=VDD(ON)+0.1V, ILIMIT:ILIMIT_L ⇒ ILIMIT_M	−29	−44	−14	uA
25	CL Pin Voltage for ILIMIT_M change	VCL2	VDD=VDD(ON)+0.1V, ICL=ICL2	2.35	1.75	2.95	V
26	CL Pin Short current	ICL_GND	VDD=VDD(ON)+0.1V, VCL=0V	−22	−37	−7	uA
27	CL Pin Voltage	VCL	VDD=VDD(ON)+0.1V, ICL=−50uA	2.3	1.6	2.9	V
28	Output Frequency High	foscH	VD=5V, VDD=VDD(ON)+0.1V, IFB=30uA, If=−50uA,VCL=0V, after dis_OLP *Refer Fig.3	64	57.5	70.5	kHz
29	Jitter Freq deviation at foscH	⊿fH	VD=5V, VDD=VDD(ON)+0.1V, IFB=30uA, If=−50uA,VCL=0V, after dis_OLP *Refer Fig.3	4	1.6	6.4	kHz

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No.	Item	Symbol	Measure Condition (See Fig. 1)	Typ.	Min.	Max.	Unit
*30	Jitter Freq Modulation Rate at foscH	fMH	VD=5V, VDD=VDD(ON)+0.1V, IFB=30uA, If=−50uA,VCL=0V, after dis_OLP *Refer Fig.3	250	–	–	Hz
31	Output Frequency Low	foscL	VD=5V, VDD=VDD(ON)+0.1V, IFB=30uA, Vf=0V, VCL=0V, after dis_OLP *Refer Fig.3	24	22	26	kHz
32	Jitter Freq deviation at foscL	⊿fL	VD=5V, VDD=VDD(ON)+0.1V, IFB=30uA, Vf=0V, VCL=0V, after dis_OLP *Refer Fig.3	1.5	0.6	2.4	kHz
*33	Jitter Freq Modulation Rate at foscL	fML	VD=5V, VDD=VDD(ON)+0.1V, IFB=30uA, Vf=0V, VCL=0V, after dis_OLP *Refer Fig.3	100	–	–	Hz
【CIRCUIT PROTECTIONS】							
34	Self Protection Current Limit	ILIMIT	VDD=VDD(ON)+0.1V, *Refer Fig.7 Vf=VDD, VCL=0V, FB:OPEN, DUTY=30%	1	0.92	1.08	A
*35	Drain current at Light Load	ID(OFF)	VDD=VDD(ON)+0.1V, IFB=IFB1−IFBHYS, Vf=VDD, VCL=0V, DUTY =30% *Refer Fig.4	200	80	320	mA
*36	OLP Detection Blanking Time	dis_OLP	VD=30V, Vf=VDD, VCL=0V, VDD, FB:OPEN	16	8	25	ms
37	Self Protection Current ILIMIT_M	ILIMIT_M	VDD=VDD(ON)+0.1V, *Refer Fig.4 Vf=VDD, ICL=−50uA, FB:OPEN, DUTY=30%	0.8	0.724	0.876	A
*38	Drain current at Light Load of ILIMIT_M	ID(OFF)_M	VDD=VDD(ON)+0.1V, IFB=IFB1−IFBHYS, Vf=VDD, ICL=−50uA, DUTY =30% *Refer Fig.4	145	55	235	mA
39	Self Protection Current ILIMIT_L	ILIMIT_L	VDD=VDD(ON)+0.1V, *Refer Fig.4 Vf=VDD, VCL=VDD, FB:OPEN, DUTY=30%	0.58	0.525	0.635	A
*40	Drain current at Light Load_L	ID(OFF)_L	VDD=VDD(ON)+0.1V, IFB=IFB1−IFBHYS, Vf=VDD, VCL=VDD, DUTY =30% *Refer Fig.4	100	40	160	mA
41	VDD current at latch stop	IDD(OV)	VD=5V, IFB=30uA, VCL=0V, Vf=0V	32	22	42	mA
42	FB current at detecting OLP	IFB(OLP)	VD=20V, VCL=0V, Vf=VDD, VDD:OPEN	11.5	6	17	uA
43	Timer intermittent function	TIMER	VDD(ON)⇔VDD(OFF) *Refer Fig.5 VD=45V, IFB<IFB(OLP)	8	–	–	–
44	Timer intermittent function disabled at MAXDC	TIMER2	VDD(ON)⇔VDD(OFF) *Refer Fig.6 IFB<IFB(OLP), DUTY=MAXDC	1	–	–	–
45	Power−up Reset Threshold Voltage	VDDreset		2.6	1.8	3.5	V
*46	Over Temperature Protection	OTP		140	130	150	℃
*47	OTP Hysteresis	Δ OTP		70	–	–	℃
【OUTPUT】							
*48	Leading Edge Blanking Delay	ton(BLK)	VDD=VDD(ON)+0.1V, IFB=30uA, Vf=VDD, VCL=0V	300	240	360	ns
*49	Current Limit Delay	td(OCL)		70	20	120	ns
50	ON−State Resistance	RDS(ON)	IDS=100mA	4.6	–	5.8	Ω

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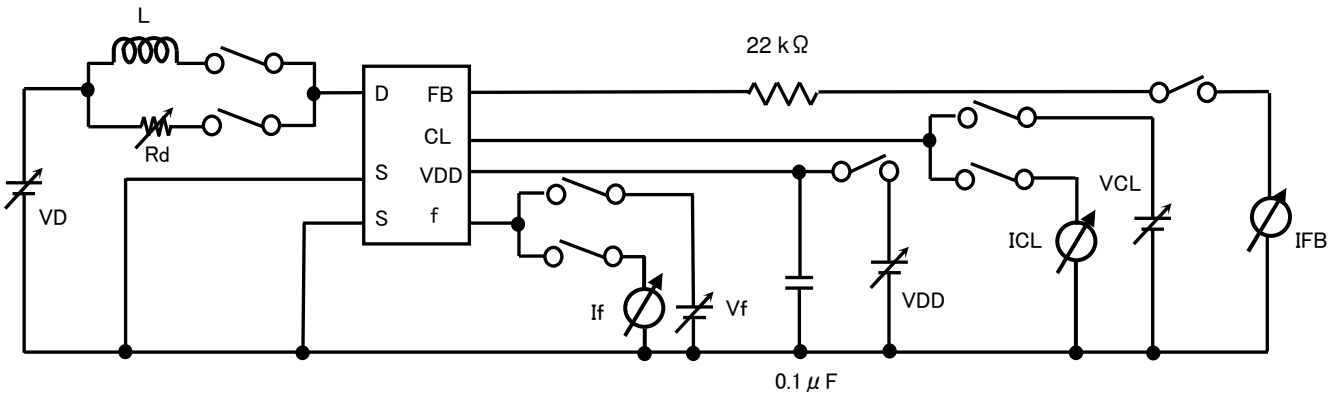
No.	Item	Symbol	Measure Condition (See Fig. 1)	Typ.	Min.	Max.	Unit
51	Breakdown Voltage	VDSS	VDD:VDD(ON)+0.1V⇒VDD(OFF)−0.1V⇒ VDD(ON)+0.1V, ID=100uA, VFB=0V	−	700	−	V
52	OFF−State Current	IDSS	VDD:VDD(ON)+0.1V⇒VDD(OFF)−0.1V⇒ VDD(ON)+0.1V, VDS=650V, VFB=0V	10	−	20	uA
53	Rise Time	tr	VD=5V, VDD=VDD(ON)+0.1V, IFB=30uA, Vf=VDD, VCL=0V *Refer Fig.8	110	−	−	ns
54	Fall Time	tf	VD=5V, VDD=VDD(ON)+0.1V, IFB=30uA, Vf=VDD, VCL=0V *Refer Fig.8	40	−	−	ns
【SUPPLY】							
55	Drain Supply Voltage	VD(MIN)	IFB=30uA, Vf=VDD, VCL=0V, VDD:OPEN	10	−	35	V
【CONTROL FUNCTIONS during VDD=VDD(CLAMP)】							
56	Output Frequency at CLAMP	foscC	VD=5V, VDD=VDD(CLP)−0.1V, IFB=30uA, Vf=VDD, VCL=0V *Refer Fig.3	46	40	52	kHz
57	Jitter Freq Deviation at CLAMP	Δ fC	VD=5V, VDD=VDD(CLP)−0.1V, IFB=30uA, Vf=VDD, VCL=0V *Refer Fig.3	4.8	1.92	7.68	kHz
*58	Jitter Freq Modulation Rate at CLAMP	fMC	VD=5V, VDD=VDD(CLP)−0.1V, IFB=30uA, Vf=VDD, VCL=0V *Refer Fig.3	100	−	−	Hz
【CIRCUIT PROTECTIONS during VDD=VDD(CLAMP)】							
59	Self Protection Current Limit at Clamp	ILIMIT_C	VDD=VDD(CLP)−0.1V, Vf=VDD, VCL=0V, FB:OPEN, DUTY=30%	1.06	0.95	1.17	A
【OUTPUT during VDD=VDD(CLAMP)】							
*60	Leading Edge Blanking Delay at CLAMP	ton(BLK)_C	VDD=VDD(CLP)−0.1V, IFB=30uA, Vf=VDD, VCL=0V	360	290	430	ns

【Fig. 1： Measure Circuit】



【Fig. 2： fosc, ILIMIT setting method through f, CL pins】

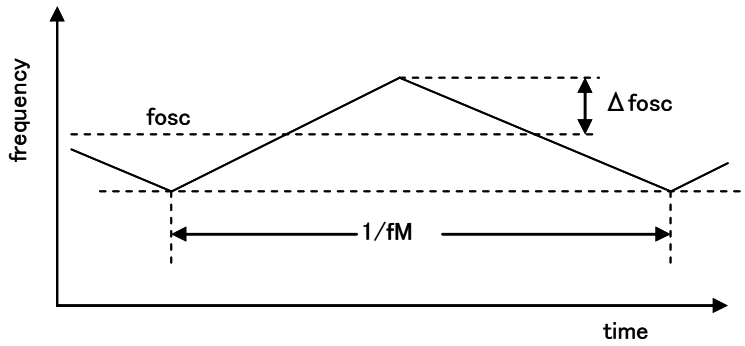
Depending upon the selection at f pin and CL pin according to description ①~③ below, output frequency (fosc) and overcurrent protection detection (ILIMIT) are set based on the below-mentioned table.

① Connection to Source pin
② Resistor (47kΩ) connected between Source pin(*)
③ Connection to VDD pin
(*) ②Please use resistor of 47kΩ (tolerance: within ±5%)

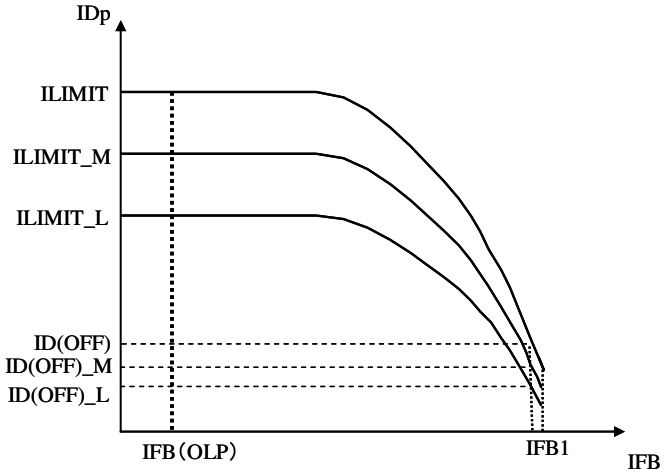
	f	fosc (kHz)
①	Source	foscL
②	resistor (47kΩ)	foscH
③	VDD	fosc

	CL	ILIMIT (A)
①	Source	ILIMIT
②	resistor (47kΩ)	ILIMIT_M
③	VDD	ILIMIT_L

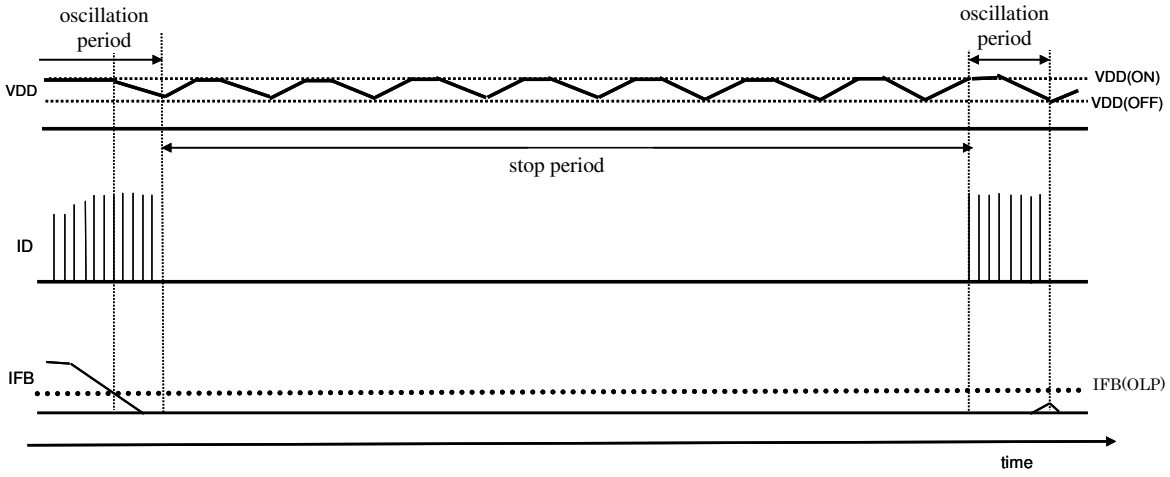
【Fig. 3： fosc, Δf, fM measurement】



【Fig. 4： FB current IFB vs Drain peak current IDp characteristic】

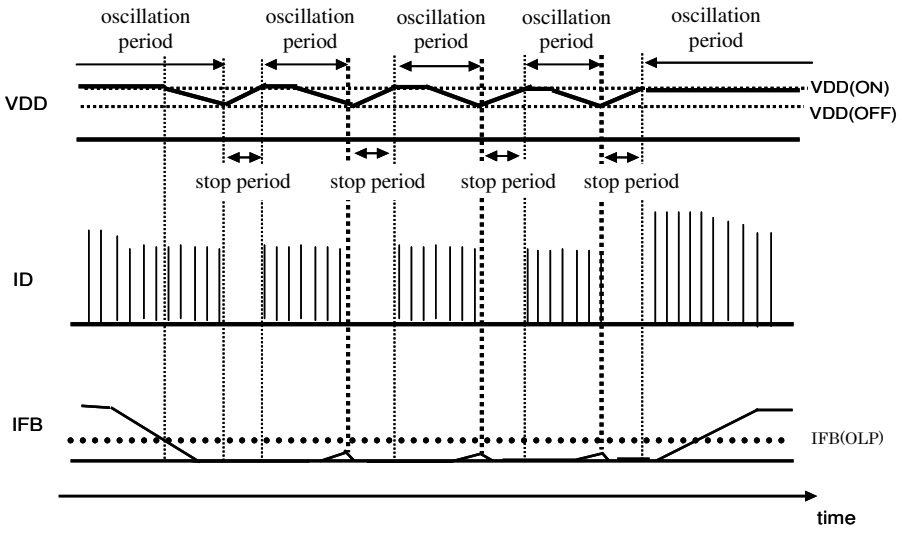


【Fig. 5: Pin waveforms during timer intermittent operation due to the overload protection】

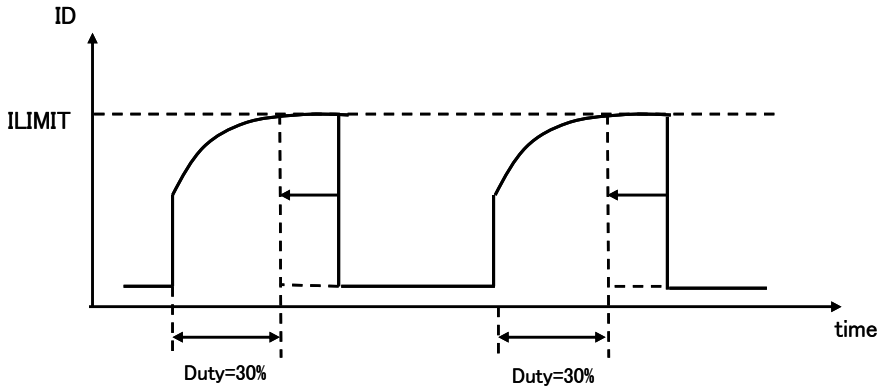


【Fig. 6: Pin waveforms when MAXDC is detected which makes timer intermittent operation becomes invalid】

Though FB current is below IFB(OLP) which indicates the detection of overload state, if the ON duty of the Drain current is operating at MAXDC, Drain oscillation will occur in every rise and fall cycle of the VDD pin.

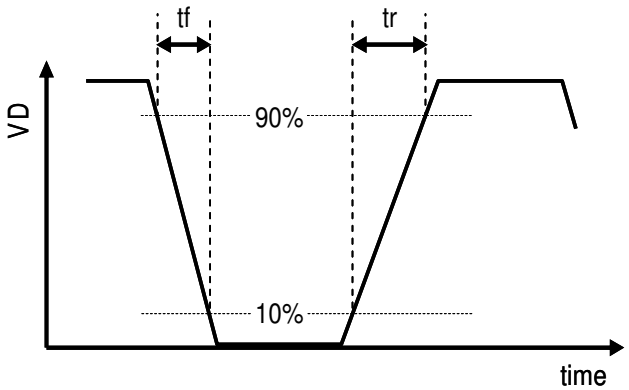


【Fig. 7: ILIMIT measurement】

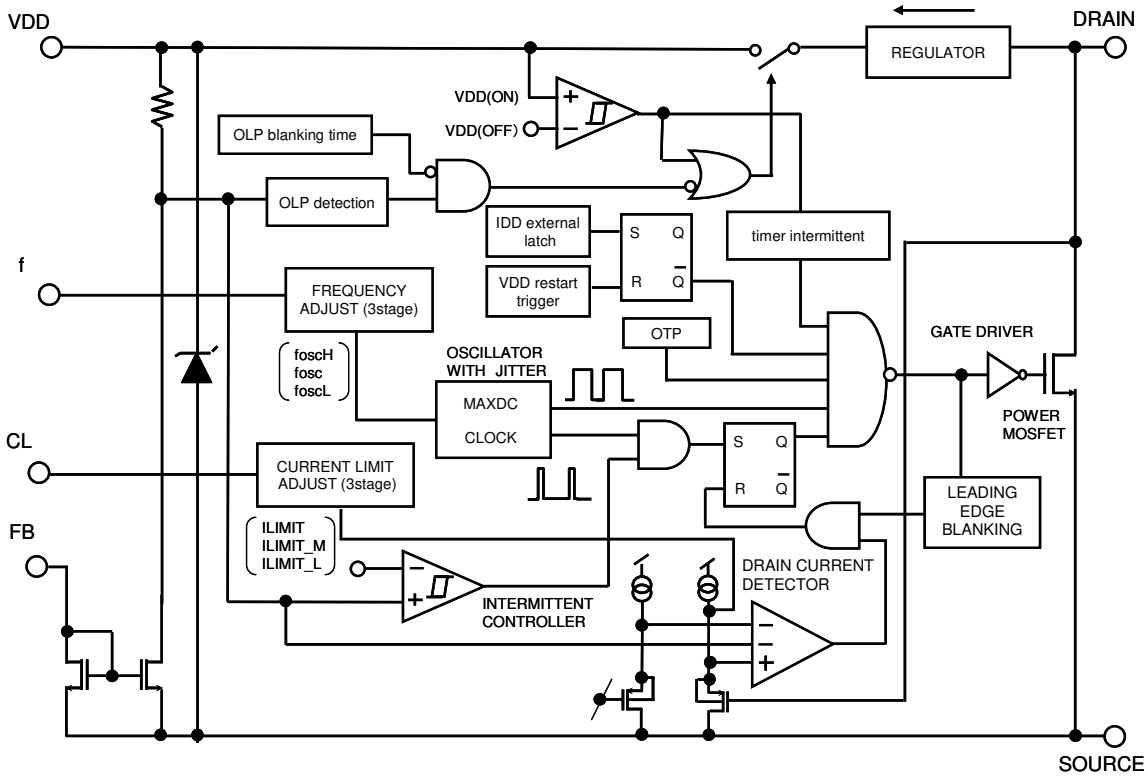


* Load L, R during the ILIMIT measurement are: L=100 μ H, Rd=130Ω

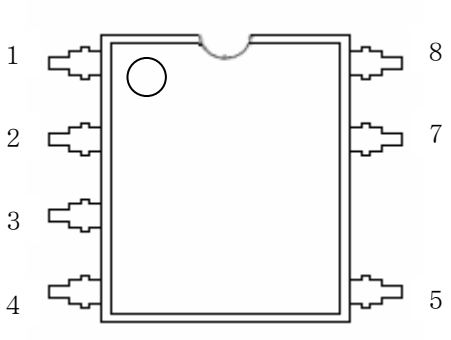
【Fig. 8 : tr, tf measurement】



【Fig. 9： Block Diagram】



【Fig. 10： Pin Layout】



Pin No.	Pin Name
1	f
2	VDD
3	CL
4	FB
5	Drain
6	—
7	Source
8	Source

【Usage Precaution 1】
Connect a ceramic capacitor with value >0.1 μF between VDD pin and Source.

【Usage Precaution 2】
Please use resistor of 47kΩ (tolerance: within ±5%) when using external variable pin function (CL pin, f pin).

【Usage Precaution 3】
The IPD has risks for break-down or burst or giving off smoke in following conditions. Avoid the following use.
Fuse should be added at the input side or connect zener diode between control pins and GND, etc as a countermeasure to pass regulatory Safety Standard. Concrete countermeasure could be provided individually. However, customer should make the final judgment.

（1） Reverse the DRAIN pin and f pin connection to the power supply board.

（2） DRAIN pin short to VDD pin.

（3） DRAIN pin short to FB pin.

（4） DRAIN pin short to CL pin.

（5） DRAIN pin short to f pin.

（6） VDD pin short to FB pin.

（7） FB pin short to CL pin.

（8） FB pin short to f pin.

（9） CL pin short to f pin.

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