Notification about the transfer of the semiconductor business

The semiconductor business of Panasonic Corporation was transferred on September 1, 2020 to Nuvoton Technology Corporation (hereinafter referred to as "Nuvoton"). Accordingly, Panasonic Semiconductor Solutions Co., Ltd. became under the umbrella of the Nuvoton Group, with the new name of Nuvoton Technology Corporation Japan (hereinafter referred to as "NTCJ").

In accordance with this transfer, semiconductor products will be handled as NTCJ-made products after September 1, 2020. However, such products will be continuously sold through Panasonic Corporation.

Publisher of this Document is NTCJ.
If you would find description “Panasonic” or “Panasonic semiconductor solutions”, please replace it with NTCJ.

※ Except below description page
“Request for your special attention and precautions in using the technical information and semiconductors described in this book”

Nuvoton Technology Corporation Japan

Panasonic

MIP3610MFL

Type	Silicon MOSFET type Integrated Circuit		
Application	For Switching Power Supply Control		
Structure	Bi-CMOS type		
Equivalent Circuit	Figure 6		
Package	SO8-G2-B	Marking	MIP361

A. ABSOLUTE MAXIMUM RATINGS (Ta=25±3℃)

No.	Item	Symbol	Ratings	Unit	Note
1	Drain Voltage	VD	−0.3 ～ 700	V	*1: It is guaranteed within the MIN(PW)
2	VDD Voltage	VDD	−0.3 ～ 8	V	
3	Feedback Voltage	VFB	−0.3 ～ 8	V	
4	Output Peak Current	IDP	1.0 (*1)	A	
5	Junction Temperature	Tj	150	℃	
6	Storage Temperature	Tstg	−55 ～ +150	℃	

B. RECOMMENDED OPERATING CONDITIONS

No.	Item	Symbol	Ratings	Unit	Note
1	Junction Temperature	Tj	−40 ～ +125	℃	

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C. ELECTRICAL CHARACTERISTICS (Measurement Condition: Ta=25±3℃)

No.	Item	Symbol	Measurement Condition (Figure 1)	Typ.	Min.	Max.	Unit
【CONTROL FUNCTIONS】 ∗∗Reference items							
1	Output Frequency	fosc	VD=5 V, VDD=VDD(ON) + 0.1 V, IFB=20 μA ∗Figure 2	66	59.4	72.6	kHz
2	Jitter Frequency Deviation	Δf	VD=5 V, VDD=VDD(ON) + 0.1 V, IFB=20 μA ∗Figure 2	3	1.5	4.5	kHz
∗∗3	Jitter Frequency Modulation Rate	fM	VD=5 V, VDD=VDD(ON) + 0.1 V, IFB=20 μA ∗Figure 2	250	–	–	Hz
4	Maximum Duty Cycle	MAXDC	VD=5 V, VDD=VDD(ON) + 0.1 V, IFB=20 μA	69	64	74	%
5	VDD Start Voltage	VDD(ON)	VD=5 V, IFB=20 μA ∗Figure 3	6.0	5.5	6.5	V
6	VDD Stop Voltage	VDD(OFF)	VD=5 V, IFB=20 μA ∗Figure 3	4.9	4.4	5.4	V
7	VDD Charging Start Voltage during Over Load Protection	VDD(CHG)	VD=40 V, IFB=20 μA ∗Figure 3	4.0	3.5	4.5	V
8	VDD Hysteresis: Start／Stop	VDDHYS1	VDD(ON) - VDD(OFF)	1.1	0.6	1.6	V
9	VDD Difference Start／Charging Start during OLP	VDDHYS2	VDD(ON) - VDD(CHG)	2.0	1.5	2.5	V
10	VDD Difference Stop／Charging Start during OLP	VDDHYS3	VDD(OFF) - VDD(CHG)	0.9	0.4	1.4	V
11	VDD Clamp Voltage	VDD(CLP)	IDD=3 mA	6.3	5.7	6.9	V
12	Feedback Threshold Current	IFB1	OFF→ON, VD=5 V	45	25	65	μA
13	Feedback Pin Voltage	VFB1	VD=5 V, VDD=VDD(ON) + 0.1 V, IFB=IFB1	2.5	2.2	2.8	V
14	VDD current before start up	IDD (SB)	VD=5 V, VDD=VDD(ON) - 0.3 V, FB : OPEN	140	70	210	μA
15	VDD current at operating	IDD(OP)	VD=5 V, VDD=VDD(ON) + 0.1 V, IFB=20 μA	200	120	280	μA
16	VDD current at light-load operation	IDD (OFF)	VD=5 V, VDD=VDD(ON) + 0.1 V, IFB=IFB1 + 5 μA	150	70	230	μA
17	VDD Charging Current	Ich1	VDD=0 V, VD=40 V, FB : OPEN	-3.70	-5.55	-1.85	mA
		Ich2	VDD=5 V, VD=40 V, FB : OPEN	-2.10	-3.15	-1.05	mA
∗∗18	Soft start duration	Tsoft	VDD=VDD(OFF) → VDD(ON), IFB=20 μA	6	–	–	ms

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No.	Item	Symbol	Measurement Condition (Figure 1)	Typ.	Min.	Max.	Unit
【CIRCUIT PROTECTIONS】 ∗Design guaranteed items, ∗∗Reference items							
19	Self Protection Current Limit	ILIMIT	VDD=VDD(ON) + 0.1 V, IFB = 20 μA, DUTY=30 % ∗Figure 4	0.260	0.234	0.286	A
20	Jitter Maximum of Self Protection Current Limit	ILIMITmax	VDD=VDD(ON) + 0.1 V, IFB = 20 μA, DUTY=30 % ∗Figure 4	0.265	–	0.300	A
21	Jitter Minimum of Self Protection Current Limit	ILIMITmin	VDD=VDD(ON) + 0.1 V, IFB = 20 μA, DUTY=30 % ∗Figure 4	0.255	0.220	–	A
∗∗22	Jitter Deviation of Self Protection Current Limit	ΔILIMIT	ΔILIMIT=(ILIMITmax - ILIMITmin)/2 ∗Figure 4	0.005	–	–	A
∗23	OLP Detection Delay Time at start up	dis_OLP	VD=40 V, VDD : OPEN, FB : OPEN	40	25	55	ms
24	VDD Current at latch stop	IDD(OV)	VD=5 V, IFB=20 μA	12	7	18	mA
25	Feedback Current at detecting OLP	IFB(OLP)	VD=40 V, VDD : OPEN	12	6	18	μA
26	Power-up Reset Threshold Voltage	VDDreset		2.6	1.8	3.5	V
∗27	Thermal Shutdown Temperature	OTP		140	130	150	℃
∗∗28	Thermal Shutdown Temperature Hysteresis	ΔOTP		70	–	–	℃
【OUTPUT】 ∗∗Reference items							
∗∗29	Leading Edge Blanking Delay	ton(BLK)		300	–	–	ns
∗∗30	Over Current Protection Delay	td(OCL)		170	–	–	ns
31	Minimum On-Pulse Width	MIN(PW)	VD=35 V	340	–	460	ns
32	Drain ON-State Resistance	RDS(ON)	ID=100 mA	18.5	–	23.5	Ω
33	Drain Breakdown Voltage	VDSS	VDD=VDD(ON)+0.1 V, ID=100 μA, FB : OPEN	–	700	–	V
34	Drain OFF-State Leakage Current of Drain pin	IDSS	VDD=VDD(ON)+0.1 V, VDS=630 V, FB : OPEN	5	–	20	μA
∗∗35	Rise Time	tr	VD=5 V, VDD=VDD(ON)+0.1 V, IFB=20 μA ∗Figure 5	70	–	–	ns
∗∗36	Fall Time	tf	VD=5 V, VDD=VDD(ON)+0.1 V, IFB=20 μA ∗Figure 5	40	–	–	ns
【SUPPLY】							
37	Minimum Drain Supply Voltage	VD(MIN)	IFB=20 μA, VDD : OPEN ∗Drain Voltage for Starting Oscillation	10	–	18	V

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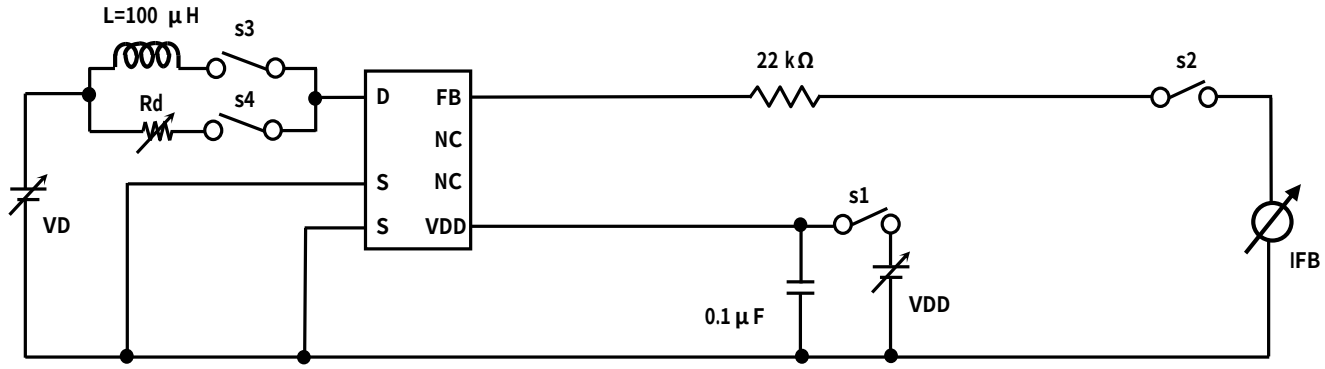
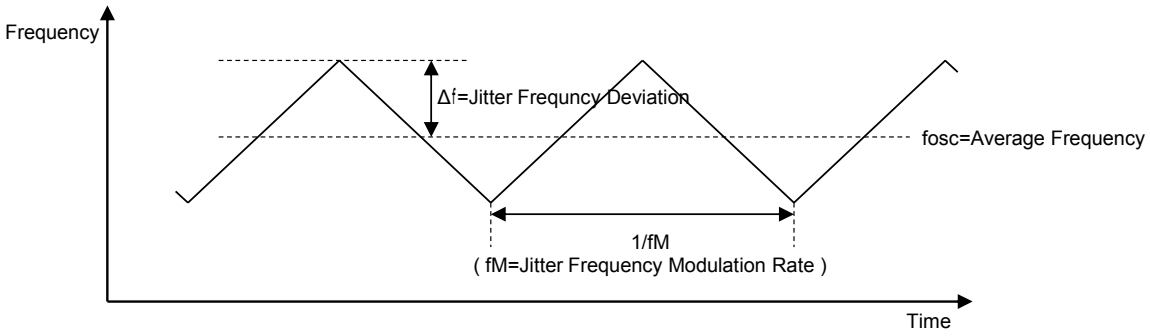
【Figure 1： Measuring Circuit】



【Figure 2： fosc, Δf, fM measurement】



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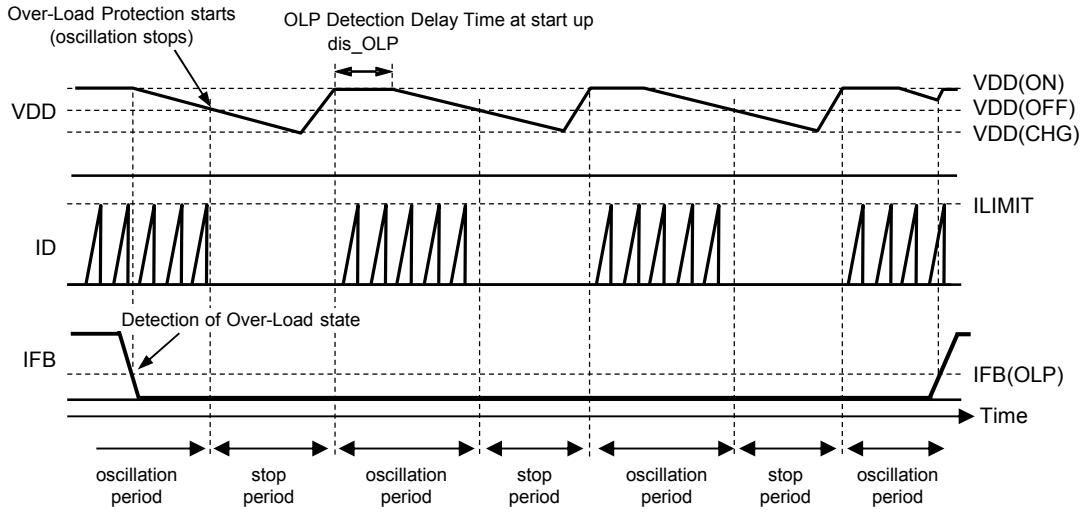
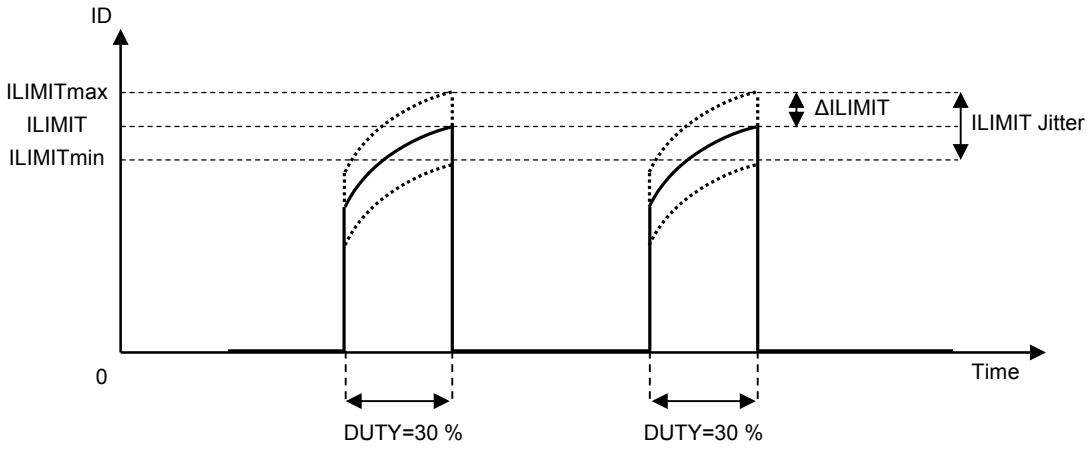
[Figure 3: Terminal waveforms during the over-load protection]



[Figure 4: ILIMIT measurement]



∗ Load condition of ILIMIT measurement: L=100μH, Rd=51Ω

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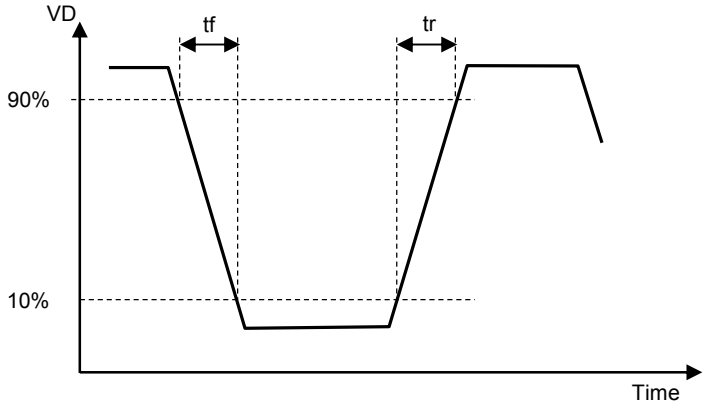
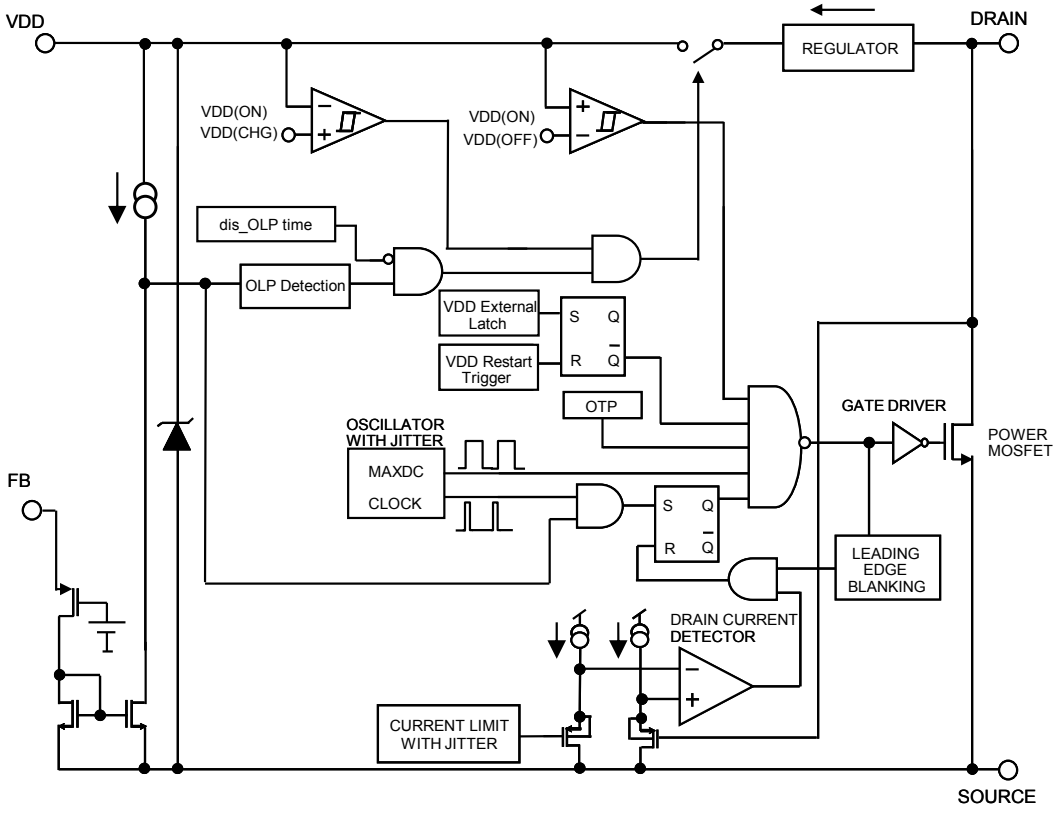
[Figure 5: tr, tf measurement]



[Figure 6: Block Diagram]



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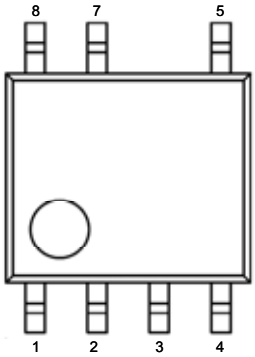
[Figure 7: Pin layout]



Pin No.	Pin Name
1	VDD
2	NC
3	NC
4	FB
5	Drain
6	–
7	Source
8	Source

∗ NC: No Connection

[Precautions for Use 1]
Connect a ceramic capacitor with value >0.1μF between VDD pin and Source pins.

[Precautions for Use 2]
The IPD has risks for break-down or burst or giving off smoke in following conditions. Avoid the following use.
Fuse should be added at the input side or connect Zener diode between control pins and Source pins, etc. as a countermeasure to pass regulatory Safety Standard. Concrete countermeasure could be provided individually. However, customer should make the final judgment.

(1) Reverse the DRAIN pin and VDD pin connection to the power supply board

(2) DRAIN pin short to VDD pin.

(3) DRAIN pin short to FB pin.

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