Notification about the transfer of the semiconductor business

The semiconductor business of Panasonic Corporation was transferred on September 1, 2020 to Nuvoton Technology Corporation (hereinafter referred to as "Nuvoton"). Accordingly, Panasonic Semiconductor Solutions Co., Ltd. became under the umbrella of the Nuvoton Group, with the new name of Nuvoton Technology Corporation Japan (hereinafter referred to as "NTCJ").

In accordance with this transfer, semiconductor products will be handled as NTCJ-made products after September 1, 2020. However, such products will be continuously sold through Panasonic Corporation.

Publisher of this Document is NTCJ.
If you would find description “Panasonic” or “Panasonic semiconductor solutions”, please replace it with NTCJ.

※ Except below description page
“Request for your special attention and precautions in using the technical information and semiconductors described in this book”

Nuvoton Technology Corporation Japan

Panasonic

MIP5310MFL

Type	Silicon MOSFET type Integrated Circuit		
Application	For Switching Power Supply Control		
Structure	CMOS type		
Equivalent Circuit	See Figure 7		
Package	SO8-G2-B	Marking	MIP531

A. ABSOLUTE MAXIMUM RATINGS (Ta=25℃±3℃)

No.	Item	Symbol	Ratings	Unit	Note
1	DRAIN Voltage	VD	−0.3 ～ 700	V	※1: It is guaranteed within the pulse as below. Leading Edge Blanking Pulse + Current Limit Delay ton(BLK)+td(OCL)
2	VIN Voltage	VIN	-0.3 ～ 650	V	
3	VDD Voltage	VDD	-0.3 ～ 8	V	
4	VDD current	IDD	30	mA	
5	Feedback Voltage	VFB	−0.3 ～ 8	V	
6	Output Peak Current	IDP	1.25(※1)	A	
7	Junction Temperature	Tj	150	℃	
8	Storage Temperature	Tstg	−55 ～ +150	℃	

B. Recommended Operating Conditions

No.	Item	Symbol	conditions	Unit	Note
1	Junction Temperature	Tj	−40 ～ +125	℃	

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C. ELECTRICAL CHARACTERISTICS Measure condition (Ta=25℃±3℃)

No.	Item	Symbol	Measure Condition (Figure 1)	Typ.	Min.	Max.	Unit
【CONTROL FUNCTIONS】* Design Guarantee Item ** Reference Value Item							
1	Output Frequency	fosc	※ Figure 6 VDD=VDD(ON), IFB=−20 μA,VD=ILIMIT condition,	100	90	110	kHz
2	Jitter Frequency Deviation	d_fosc	※ Figure 6 VDD=VDD(ON), IFB=−20 μA,VD=ILIMIT condition,	5.5	−	−	kHz
**3	Jitter Frequency Modulation Rate	fM	※ Figure 6 VDD=VDD(ON), IFB=−20 μA,VD=ILIMIT condition,	200	−	−	Hz
4	Maximum On-state Time	MAX(ON)	VDD=VDD(ON), IFB=−20 μA, VD=5 V,	13	9.4	16.6	μs
5	VDD start Voltage	VDD(ON)	VD=5 V, IFB=−20 μA,	5.9	5.4	6.4	V
6	VDD stop Voltage	VDD(UV)	VD=5 V, IFB=−20 μA,	4.9	4.4	5.4	V
7	VDD start/stop Voltage Hysteresis	⊿VDD	VDD(ON) − VDD(UV)	1.0	0.5	1.5	V
8	VDD clamp Voltage	VDD(CLP)	IDD=3 mA	6.2	5.6	6.8	V
9	Delta VDD clamp	D_VDD(CLP)	VDD(CLP)−VDD(ON)	0.3	0.05	0.7	V
10	Feedback Current	IFB_STB	ON→OFF VDD=VDD(ON),VD=ILIMIT condition,	−100	−155	−45	μA
11	Feedback Current Hysteresis	IFB(HYS)	OFF→ON VDD=VDD(ON),VD=ILIMITcondition,	4	−	−	μA
12	FB Pin Voltage	VFB	VDD=VDD(ON), IFB=−20 μA, VD=ILIMIT condition,	2	1.65	2.35	V
13	FB Pin Voltage at light load	VFB_STB	VDD=VDD(ON), IFB=IFB_STB, VD=ILIMIT condition,	1.75	1.4	2.1	V
14	FB Pin Grounded Current	IFB_GND	VDD=VDD(ON), VFB=0 V, VD=ILIMIT condition,	−360	−500	−240	μA
15	Pre-start Consuming Current	IDD(SB)	VDD=VDD(ON)−0.3 V, IFB=−20 μA, VD=5 V,	0.22	0.16	0.28	mA
16	Operating Circuit Consuming Current	IDD	VDD=VDD(ON), IFB=−20 μA, VD=ILIMIT condition,	0.38	0.24	0.52	mA
17	Operating Circuit Consuming Current at light load	IDD(OFF)	VDD=VDD(ON), IFB=IFB_STB, VD=ILIMIT condition,	0.38	0.20	0.56	mA
18	VDD Charging Current	Ich1 Ich2	VDD=0 V, VIN=40 V, VDD=5 V, VIN=40 V,	−11 −8	−16.5 −12	−5.5 −4	mA mA

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No.	Item	Symbol	Measure Condition (Figure 1)	Typ.	Min.	Max.	Unit
【CIRCUIT PROTECTIONS】 * Design Guarantee Item ** Reference Value Item							
19	Self Protection Current Limit	ILIMIT	※Figure 4 ton=30 % duty cycle, VDD=VDD(ON),VFB=3 V, VD=adjust,	0.35	0.315	0.385	A
**20	When OCP Detected Oscillation Off-state Time	Tdet(OC)	VDD=VDD(ON), VFB=3 V, VD=adjusted,	1	–	–	μs
**21	Light-load Output Current	ID(OFF)	※Figure 4 ton=30 % duty cycle, VDD=VDD(ON),IFB=IFB_STB+5 μA, VD=adjust,	140	–	–	mA
22	FB Pin Over Load Charging Current	IFBch	VDD=VDD(ON), VFB=3 V, VD=ILIMIT condition,	−8	−11	−5	μA
23	FB Pin Over Load Protection Voltage	VFB(OLP)	VDD=VDD(ON), VD=ILIMIT condition,	4.3	3.7	4.8	V
24	VFB Hysteresis	⊿VFB	VFB(OLP)−VFB	2.3	1.45	3.15	V
25	OLP VDD Oscillation Count	OLP_CNT	※Figure 3 VDD=VDD(ON)⇔VDD(UV), VD=ILIMIT condition, FB=Open,	8			–
*26	Leading Edge Blanking Delay	ton(BLK)		330	260	400	ns
*27	Current Limit Delay	td(OCL)		100	65	135	ns
28	VDD current at latch stop	IDD(OV)	ON→OFF IFB=−20 μA, VD=5 V,	14	9	21	mA
*29	Thermal Shutdown Temperature	TOTP		140	130	150	℃
	Thermal Shutdown Temperature Hysteresis	⊿TOTP		70	–	–	℃
30	Power-up Reset Threshold Voltage	VDDreset		2.4	1.5	3.3	V

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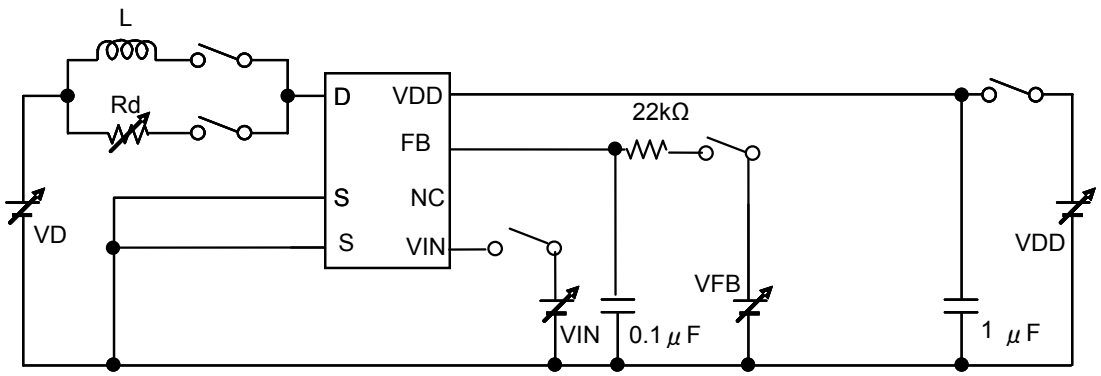
No.	Item	Symbol	Measure Condition (Figure 1)	Typ.	Min.	Max.	Unit
【High Voltage Input】 * Design Guarantee Item ** Reference Value Item							
31	Off-state VIN Pin Leakage Current	IIN(LEAK)	VIN=600 V, IDD=IDD(OV)	10	–	20	μA
32	VIN Pin Voltage	BVVIN	IIN=100 μA, IDD=IDD(OV)	–	650	–	V
33	Minimum VIN Voltage	VIN(MIN)	IFB=−20 μA, VD=5 V,	–	50	–	V
【Output】 * Design Guarantee Item ** Reference Value Item							
34	ON-State Resistance	RDS(ON)	VDD=VDD(ON), IFB=−20 μA, IDS=100 mA,	16	–	22	Ω
35	OFF-State Current	IDSS	IDD=IDD(OV), IFB=−20 μA, VD=650 V,	2	–	20	μA
36	Breakdown Voltage	VDSS	IDD=IDD(OV), IFB=−20 μA, ID=100 μA,	–	700	–	V
**37	Rise Time	tr	※Figure 5 VDD=VDD(ON), IFB=−20 μA, VD=5 V,	50	–	–	ns
**38	Fall Time	tf	※Figure 5 VDD=VDD(ON), IFB=−20 μA, VD=5 V,	50	–	–	ns

【Figure 1： Measure Circuit】



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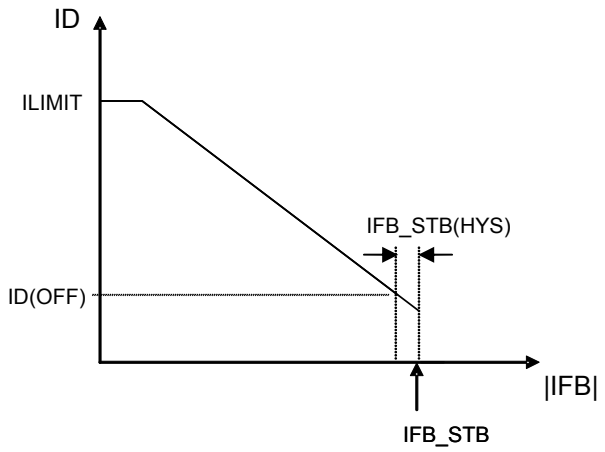
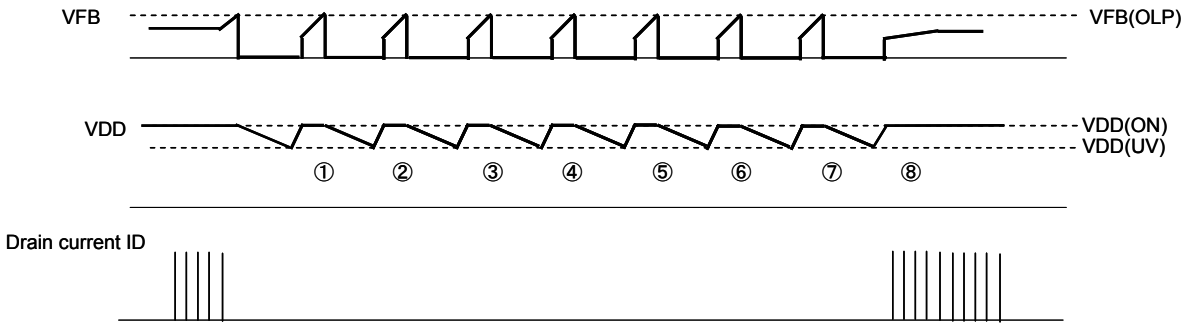
【Figure 2 : ID vs IFB Measurement】



【Figure 3 : Over-Load Detected Measurement】



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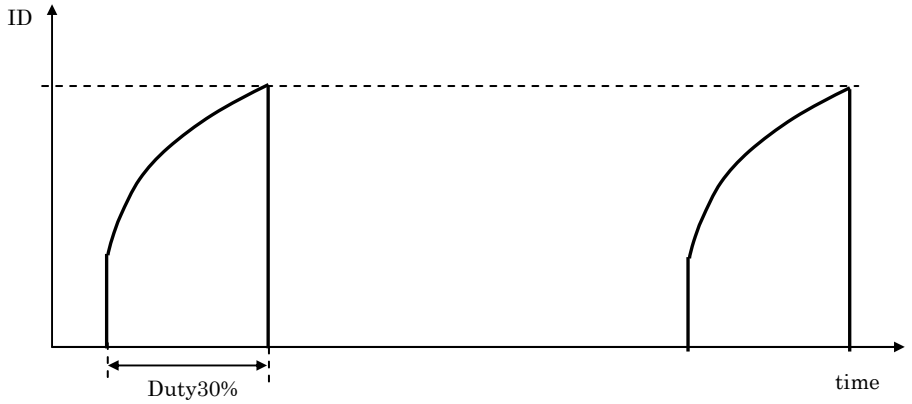
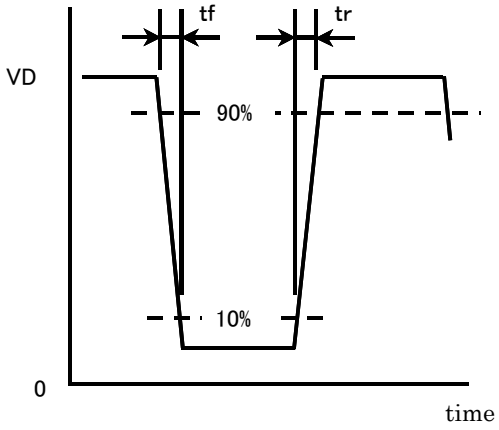
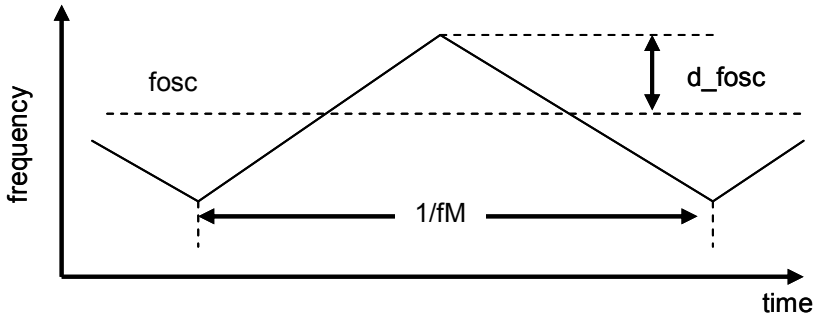
【Figure 4 : ILIMIT, ID(OFF) Measurement】



【Figure 5 : tr, tf Measurement】



【Figure 6 : d_fosc, fM Measurement】



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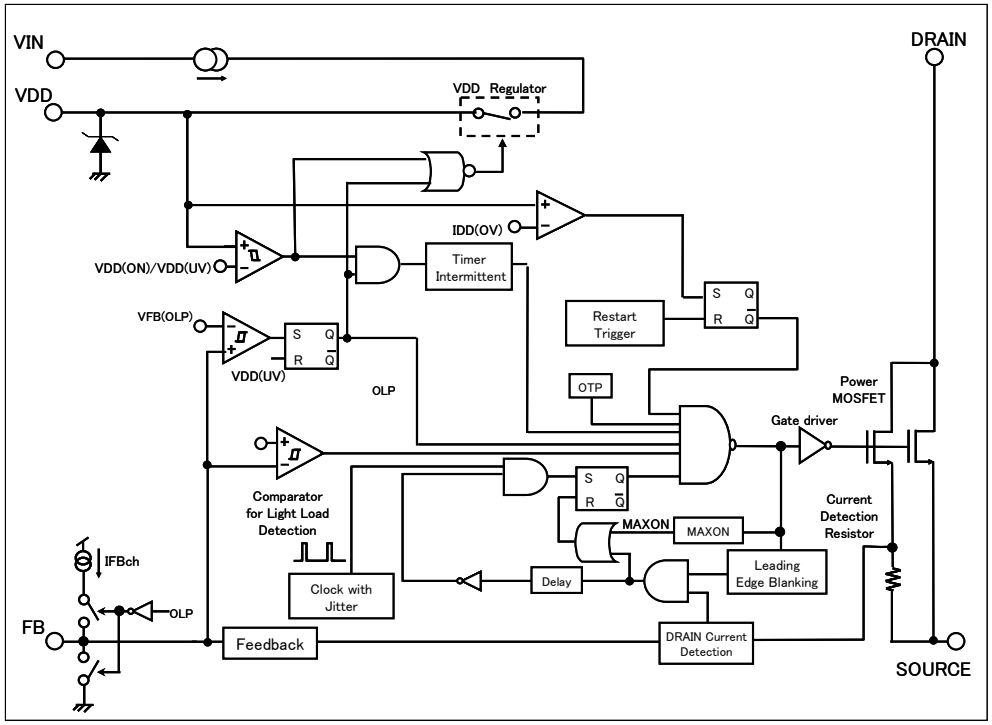
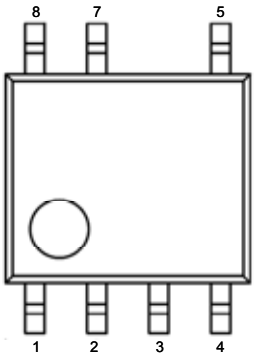
【Figure 7 : Block Diagram】



【Figure 8 : Pin Layout】



Pin No.	Terminal Name
1	VIN
2	NC
3	FB
4	VDD
5	DRAIN
6	—
7	SOURCE
8	SOURCE

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【Precautions for Use 1】
Connect a Ceramic Capacitor (over 1 μF) between VDD Pin and SOURCE.

【Precautions for Use 2】
The IPD has risks for break-down or burst or giving off smoke in following conditions. Avoid the following use.
Fuse should be added at the input side or connect zener diode between control pin and GND, etc as a countermeasure to pass regulatory Safety Standard. Concrete countermeasure could be provided individually. However, customer should make the final judgment.

(1) DRAIN Pin and VIN Pin reversely connect into power board.

(2) DRAIN Pin and VIN Pin short circuit.

(3) DRAIN Pin and FB Pin short circuit.

(4) DRAIN Pin and VDD Pin short circuit.

(5) VIN Pin and FB Pin short circuit.

(6) VIN Pin and VDD Pin short circuit.

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