Notification about the transfer of the semiconductor business

The semiconductor business of Panasonic Corporation was transferred on September 1, 2020 to Nuvoton Technology Corporation (hereinafter referred to as "Nuvoton"). Accordingly, Panasonic Semiconductor Solutions Co., Ltd. became under the umbrella of the Nuvoton Group, with the new name of Nuvoton Technology Corporation Japan (hereinafter referred to as "NTCJ").

In accordance with this transfer, semiconductor products will be handled as NTCJ-made products after September 1, 2020. However, such products will be continuously sold through Panasonic Corporation.

Publisher of this Document is NTCJ.

If you would find description "Panasonic" or "Panasonic semiconductor solutions", please replace it with NTCJ.

Except below description page
 "Request for your special attention and precautions in using the technical information and semiconductors described in this book"

Nuvoton Technology Corporation Japan

Doc No. TD4-EA-01829 Revision. 2

Panasonic

MIP5610MSSCF

Type	Silicon MOSFET type Integrated Circuit					
Application	For Green Lighting driving	For Green Lighting driving				
Structure	CMOS type					
Block diagram	Figure 5					
Out Line	DIP7-A1	Marking	MIP561			

A. ABSOLUTE MAXIMUM RATINGS (Ta=25°C±3°C)

A . AL	SOLUTE MAXIMUM RATINGS (1	a=25 C士、	3 C)	•	
NO.	Item	Symbol	Ratings	Unit	Note
1	DRAIN Voltage	VD-S	−0.3 ~ 700	٧	
2	VIN Voltage	VIN-S	−0.3 ~ 550	٧	
3	VDD Voltage	VDD-S	−0.3 ~ 9.5	٧	
4	FB Voltage	VFB-S	−0.3 ~ 7.0	٧	
5	FB Current	IFB	-200	μΑ	
6	Output Peak Current	IDP	2.0 (※1)	Α	※1: IDP is guaranteed at
7	Junction Temperature	Тj	150	°C	the pulse width narrower than MIN(PW).
8	Storage Temperature	Tstg	−55 ~ +150	°C	11 (1 11 / .

B. RECOMMENDED OPERATING CONDITIONS

NO.	Item	Symbol	Ratings	Unit	Note
1	Junction Temperature	Тj	−40 ~ +125	°C	

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C. ELECTRICAL CHARACTERISTICS

[CONTROL FUNCTIONS]

Measure condition(Ta=25°C±3°C, Figure1)

*Design Guarantee Item, **Reference Item

[CON I	IRUL FUNCTIONS]	*Design G	uarantee Item, **Reference Item				
No.	Item	Symbol	Measure Condition (Figure 1)	Тур.	Min	Max	Unit
	VDD Start Voltage		VD=5 V, VFB=0 V				
1		VDD (ON)	,	6.0	5. 5	6. 5	٧
	VDD Stop Voltage		VD=5 V, VFB=0 V				
2	, -	VDD (UV)		5.0	4. 5	5. 5	٧
	Circuit Current before start		VDD=VDD (ON) -0. 1 V, VD=5 V				
3		IS1	VFB=VFB-Io-5 mV	0.57	0.37	0. 77	mΑ
	Circuit Current under switching		VDD=VDD (ON) +O. 1 V, VD=5 V				
4		IS2	VFB=VFB-Io-5 mV	0.72	0.47	0. 97	mA
	Maximum output frequency		VFB=VFB_hi+5 mV ※Figure3				
5		fPFM-hi	VD=5 V, VDD=VDD(ON)+0.1 V,	128. 5	120.8	_	kHz
	Minimum output frequency		VFB=VFB_lo-5 mV ※Figure3				
6		fPFM-lo	VD=5 V, VDD=VDD (ON) +0. 1 V,	19. 3	_	27	kHz
	Output frequency at skip mode		VD=5 V, VDD=VDD (ON) +0. 1 V,				
7		fskip	Ton <skip(pw),< td=""><td>13</td><td>9. 1</td><td>16. 9</td><td>kHz</td></skip(pw),<>	13	9. 1	16. 9	kHz
	Maximum on duty		VFB=VFB_hi+5 mV				
8	·	MAXDC	VD=5 V, VDD=VDD(ON)+0.1 V	70	63	77	%
**	Feedback pin reference voltage						
9		VFB-c	VFB-c=(VFB-hi + VFB-lo)/2	15	_	_	mV
**	FB voltage at fPFM-hi						
10	_	VFB-hi		25	_	_	mV
**	FB voltage at fPFM-lo						
11	_	VFB-1o		5	_	_	mV
**	Gain of fosc-VFB		GainFB=(fPFM-hi - fPFM-lo)/(VFB-hi - VFB-lo)				
12		GainFB		5. 46	_	_	kHz/m\
**	The feedback dummy maximum current						
13		IFBdm(max)		-100	_	_	μA
	Output current accuracy		-(VFB-c + 3.15 × IFBdm(max))/300 × 100 -100				
14		Ιο		_	-3. 5	3. 5	%

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[PRO	TECT FUNCTION]	*Design G	uarantee Item, **Reference Item				
No.	Item	Symbol	Measure Condition (Figure 1)	Тур.	Min	Max	Unit
	Maximum Peak Current Limit		VDD=VDD(ON)+0.1 V, VFB=VFB-Io-30 mV				
15		ILIMITmax	Duty=30 % ※Figure2	0.4	0.364	0.436	Α
	Power-up Reset Threshold Voltage						
16		VDDrst		2. 6	1.6	3.6	٧
	VDD latch stop voltage		ON→0FF				
17		VDD (OV)	VD=5 V, VFB=0 V	7. 4	6.4	8. 4	٧
	VDD latch stop current		ON→0FF				
18		IDD (OV)	VD=5 V, VFB=0 V	3. 7	2. 2	5. 2	mA
	VFB latch stop voltage		ON→0FF				
19		VFB (0V)	VD=5 V, VDD=VDD (ON) +0. 1 V	3. 5	3. 0	4. 0	٧
**	Leading Edge Blanking Delay						
20		ton (BLK)		200	_	_	ns
**	Peak Current Limit Delay						
21		td (OCL)		200	_	_	ns
	Minimum on-pulse width		VIN=50 V, VD=35 V				
22		MIN(PW)		320	_	440	ns
	Skip detect on-pulse width		VIN=50 V, VD=35 V				
23		Skip(PW)		450	_	570	ns
*	Thermal Shutdown Junction						
24	Temperature	TOTPJ		140	130	150	ွပ
*	Thermal Shutdown Hysteresis						
25		TOTP. Ihvs		70	_	_	°C

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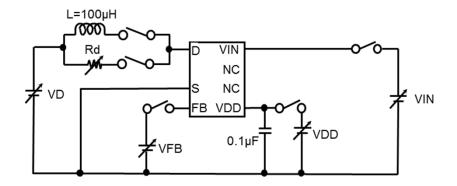
【OUTI	PUT】	*Design G	uarantee Item, **Reference Item				
No.	Item	Symbol	Measure Condition (Figure 1)	Тур.	Min	Max	Unit
	ON-State Resistance		VDD=VDD (ON) +0. 1 V				
26		RDS (ON)	IDS=300 mA	6. 9	_	8. 6	Ω
	OFF-State leakage Current of DRAIN Pin		VDD=VDD (ON) +0. 1 V, VFB= 4 V				
27		IDSS	VD=630 V	1.0	_	10	μ A
	Breakdown Voltage of DRAIN Pin		VDD=VDD (ON) +0. 1 V, VFB= 4 V				
28		VDSS	IDS=20 μ A	_	700	_	٧
**	Rise Time		VDD=VDD (ON) +0. 1 VIN=50 V				
29		tr	VD=5 V ※Figure4	80	_	_	ns
**	Fall Time		VDD=VDD (ON) +0. 1 VIN=50 V				
30		tf	VD=5 V ※Figure4	25	_	_	ns

[HIGH VOLTAGE INPUT]

TIII MII	I VOLIMAL INI OIZ						
	OFF-State leakage Current of VIN Pin		VDD=VDD (ON) +0. 1 V, VFB= 4 V				
31		IIN (LEAK)	VIN=500 V	48	_	80	μA
	Breakdown Voltage of VIN Pin		VDD=VDD (0N) +0. 1 V, VFB= 4 V				
32		BVVIN	IIN=100 μA	_	550	1	٧
	VDD Charging Current 1		VIN=40 V, VDD=0 V, FB: open				
33		CHRG10		-10.6	-15. 9	-5.3	mA
	VDD Charging Current 2		VIN=40 V, VDD=5 V, FB: open				
34		CHRG15		-7. 2	-10.8	-3.6	mA
	VIN start Voltage		VDD: open, VD=5 V				
35		VIN(MIN)		10	_	20	٧

[Figure1 : Measure circuit]

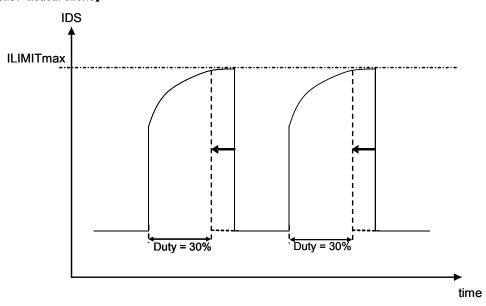
 $\ensuremath{\mbox{\ensuremath{\mbox{\sc MThe}}}\xspace}$ the characteristic is measured by a SORCE pin as a reference pin.



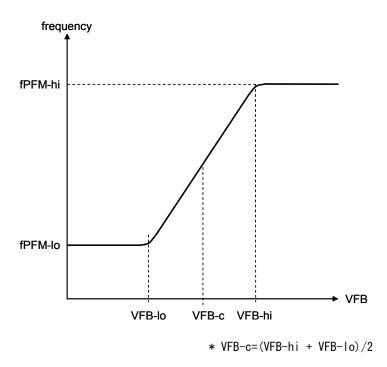
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[Figure2 : ILIMIT measurement]



[Figure3: frequency vs VFB characteristic]

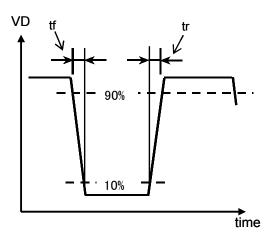


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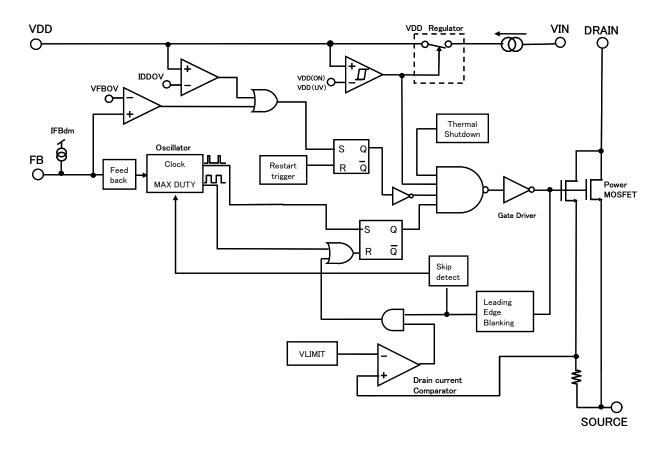
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[Figure4:tr, tf characteristic]



[Figure5:Block Diagram]



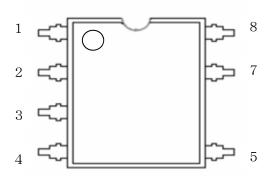
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[Figure6: Pin Layout]



Pin No.	Terminal Name
1	VDD
2	NC
3	NC
4	VIN
5	Drain
6	_
7	Source
8	FB

[Precautions for Use 1]

Connect a ceramic capacitor with value $>0.1 \mu$ F between VDD pin and SOURCE.

[Precautions for Use 2]

The IPD has risks for break-down or burst or giving off smoke in following conditions. Avoid the following use. Fuse should be added at the input side or connect zener diode between control pin and GND, etc as a countermeasure to pass regulatory Safety Standard. Concrete countermeasure could be provided individually. However, customer should make the final judgment.

- (1) DRAIN pin short to low voltage pin (VDD, FB).
- (2) VIN pin short to low voltage pin (VDD, FB).
- (3) VIN pin short to DRAIN pin under switching.
- (4) DRAIN pin short to SOURCE pin.
- (5) DRAIN Pin and VDD Pin reversely connect into power board.

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