# Notification about the transfer of the semiconductor business

The semiconductor business of Panasonic Corporation was transferred on September 1, 2020 to Nuvoton Technology Corporation (hereinafter referred to as "Nuvoton"). Accordingly, Panasonic Semiconductor Solutions Co., Ltd. became under the umbrella of the Nuvoton Group, with the new name of Nuvoton Technology Corporation Japan (hereinafter referred to as "NTCJ").

In accordance with this transfer, semiconductor products will be handled as NTCJ-made products after September 1, 2020. However, such products will be continuously sold through Panasonic Corporation.

Publisher of this Document is NTCJ.
If you would find description "Panasonic" or "Panasonic semiconductor solutions", please replace it with NTCJ.
　　※ Except below description page
　　　　"Request for your special attention and precautions in using the technical information and semiconductors described in this book"

<div style="text-align:center">Nuvoton Technology Corporation Japan</div>

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# 1.1 Overview

## 1.1.1 Overview

The MN103S is a 32-bit microcontroller combining ease of use intended for programs development in the C language with a simple, high-performance architecture made possible through pursuit of cost performance.

Built around a compact 32-bit CPU with a basic instruction word length of 1 byte, this LSI includes internal memory for instructions and data, a clock generator, bus controller, interrupt controller, watchdog timer, standard peripheral circuitry such as timers and serial interfaces, PWM circuit best suited to controlling 3-phase motors and A/D converters for motor position control. The MN103S Series' high-speed CPU coupled with abundance of peripheral features provides an easy means of developing low-cost, high-performance and multifunctional system on chip for motor and power control applications requiring fast response - a feature previously unavailable with conventional microcontrollers.

## 1.1.2 Product Summary

This manual describes the following model.

Table:1.1.1 Product Summary

| Model | ROM Size | RAM Size | Classification |
|---|---|---|---|
| MN103SFM8K | 256 K | 8 K | Flash EEPROM version |

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# 1.2　Hardware Functions

CPU Core　　　　MN103S core
　　　　　　　　4 GB of linear address space (for instructions / data)
　　　　　　　　LOAD/STORE architecture with 5-stage pipeline
　　　　　　　　46 basic instructions + 4 extension instructions
　　　　　　　　6 addressing modes
　　　　　　　　Instruction set of 1 byte in word length
　　　　　　　　Machine cycle:  16.7 ns (oscillation frequency: 10 MHz, 6 multiply)
　　　　　　　　Operation mode: Normal mode

Oscillation Circuit

　　　　　　　　External high-speed oscillation (crystal/ ceramic)

Clock Multiplication Circuit
　　　　　　　　External high-speed oscillation is multiplied by 4, 6 and 8.

Operating voltage
　　　　　　　　3.6 V to 5.5 V

Guaranteed operating temperature
　　　　　　　　-40 °C to 85 °C

Internal Memory

　　　　　　　　ROM 256 Kbytes　　　RAM 8 Kbytes

Interrupts

　　　　　　　　Non-maskable interrupt:
　　　　　　　　　　Watchdog timer overflow interrupts, System error interrupts

　　　　　　　　Internal interrupts:　　　47 interrupts
　　　　　　　　<Timer Interrupts>
　　　　　　　　Timer 0 underflow interrupts
　　　　　　　　Timer 1 underflow interrupts
　　　　　　　　Timer 2 underflow interrupts
　　　　　　　　Timer 3 underflow interrupts
　　　　　　　　Timer 4 underflow interrupts
　　　　　　　　Timer 5 underflow interrupts
　　　　　　　　Timer 6 underflow interrupts
　　　　　　　　Timer 7 underflow interrupts
　　　　　　　　Timer 8 overflow/underflow interrupts
　　　　　　　　Timer 8 compare/capture A interrupts
　　　　　　　　Timer 8 compare/capture B interrupts
　　　　　　　　Timer 9 overflow/underflow interrupts
　　　　　　　　Timer 9 compare/capture A interrupts
　　　　　　　　Timer 9 compare/capture B interrupts
　　　　　　　　Timer 10 overflow/underflow interrupts
　　　　　　　　Timer 10 compare/capture A interrupts
　　　　　　　　Timer 10 compare/capture B interrupts
　　　　　　　　Timer 11 overflow/underflow interrupts
　　　　　　　　Timer 11 compare/capture A interrupts
　　　　　　　　Timer 11 compare/capture B interrupts
　　　　　　　　Timer 12 overflow/underflow interrupts
　　　　　　　　Timer 12 compare/capture A interrupts
　　　　　　　　Timer 12 compare/capture B interrupts

Timer 13 overflow/underflow interrupts
Timer 13 compare/capture A interrupts
Timer 13 compare/capture B interrupts
Timer 14 underflow interrupts
Timer 15 underflow interrupts
Timer 16 underflow interrupts
Timer 17 underflow interrupts

<Serial Interface>
Serial 0 reception interrupts
Serial 0 transmission interrupts
Serial 1 reception interrupts
Serial 1 transmission interrupts
Serial 2 reception interrupts
Serial 2 transmission interrupts

<PWM>
PWM0  overflow interrupts
PWM0  underflow interrupts
PWM1  overflow interrupts
PWM1  underflow interrupts

<A/D interrupt>
A/D 0 conversion complete interrupt
A/D 0 conversion complete B interrupt
A/D 1 conversion complete interrupt
A/D 1 conversion complete B interrupt
A/D 2 conversion complete interrupt

External interrupts:          9 interrupts
Interrupt pins:               IRQ00 to IRQ08
Interrupt detection condition:
Edge (rising edge, falling edge), both edges, High-level detection, Low-level detection
Noise filter's filtering is possible at all conditions.

Timer Counter          8-bit timer        12 sets
                       16-bit timer        6 sets


Timer 0 (8-bit timer for general use)
- Interval timer, Timer pulse output, Event count
- Count clock source
   IOCLK, IOCLK/8, IOCLK/32, IOCLK/128, Timer 1 underflow,
  Timer 2 underflow


Timer 1 (8-bit timer for general use)
- Interval timer, Timer pulse output, Event count,
  Cascade connection function
- Count clock source
   IOCLK, IOCLK/8, IOCLK/32, Timer 0 underflow,
  Timer 2 underflow, TM1IO pin input


Timer 2 (8-bit timer for general use)
- Interval timer, Timer pulse output, Event count, Cascade connection function
- Count clock source
   IOCLK, IOCLK/8, IOCLK/32, IOCLK/128, Timer 0 underflow, Timer 1 underflow,
  TM2IO pin input

Timer 3 (8-bit timer for general use)
- Interval timer, Timer pulse output, Event count, Cascade connection function
- Count clock source
    IOCLK, IOCLK/8, IOCLK/32, TM3IO pin input,
    Timer 0 underflow, Timer 1 underflow, Timer 2 underflow,

Timer 4 (8-bit timer for general use)
- Interval timer, Timer pulse output, Event count,
- Count clock source
    IOCLK, IOCLK/8, IOCLK/32, IOCLK/128, TM4IO pin input,
   Timer 5 underflow, Timer 6 underflow

Timer 5 (8-bit timer for general use)
- Interval timer, Timer pulse output,  Event count, Cascade connection function
- Count clock source
    IOCLK, IOCLK/8, IOCLK/32, Timer 4 underflow, Timer 6 underflow, TM5IO pin input

Timer 6 (8-bit timer for general use)
- Interval timer,  Cascade connection function
- Count clock source
    IOCLK, IOCLK/8, IOCLK/32, IOCLK/128, Timer 4 underflow, Timer 5 underflow

Timer 7 (8-bit timer for general use)
- Interval timer, Timer pulse output, Event count, Cascade connection function
- Count clock source
    IOCLK, IOCLK/8, IOCLK/32, TM7IO pin input, Timer 4 underflow,
    Timer 5 underflow, Timer 6 underflow,

Timer 8 (16-bit timer for general use)
- Interval timer, Timer pulse output, Event count, PWM output, input capture,
  one-shot output, external trigger start
- Count clock source
    IOCLK, IOCLK/8, IOCLK/64, Timer 2 underflow,
   TM8BIO pin input

Timer 9 (16-bit timer for general use)
- Interval timer, Timer pulse output, Event count, PWM output, input capture,
  one-shot output, external trigger start
- Count clock source
    IOCLK, IOCLK/8, IOCLK/64, Timer 3 underflow,
   TM9BIO pin input

Timer 10 (16-bit timer for general use)
- Interval timer, Timer pulse output, Event count, PWM output, input capture,
  one-shot output, external trigger start
- Count clock source
    IOCLK, IOCLK/8, Timer 0 underflow, Timer 1 underflow,
   TM10BIO pin input
Timer 11 (16-bit timer for general use)
- Interval timer, Timer pulse output, Event count, PWM output,
  input capture, one-shot output, external trigger start
- Count clock source
    IOCLK, IOCLK/8, Timer 4 underflow, Timer 5 underflow,
   TM11IO pin input
Timer 12 (16-bit timer for general use)

- Interval timer,  trigger start 3-phase PWM,  AD conversion start
- Count clock source
   MCLK, MCLK/8, IOCLK, IOCLK/8, Timer 6 underflow,
  Timer 7 underflow

 Timer 13 (16-bit timer for general use)
- Interval timer, trigger start 3-phase PWM,  AD conversion start
- Count clock source
   MCLK, MCLK/8, IOCLK, IOCLK/8, Timer 6 underflow, Timer 7 underflow

Timer 14 (8-bit timer for general use)
- Interval timer, Baud rate timer
- Count clock source
   IOCLK, IOCLK/8, IOCLK/32, IOCLK/128, Timer 15 underflow, Timer 16 underflow

Timer 15 (8-bit timer for general use)
- Interval timer, Baud rate timer, Cascade connection function
- Count clock source
   IOCLK, IOCLK/8, IOCLK/32, Timer 14 underflow, Timer 16 underflow

Timer 16 (8-bit timer for general use)
- Interval timer, Baud rate timer, Cascade connection function
- Count clock source
   IOCLK, IOCLK/8, IOCLK/32, IOCLK/128, Timer 14 underflow, Timer 15 underflow

Timer 17 (8-bit timer for general use)
- Interval timer, Timer pulse output, Event count, Cascade connection function
- Count clock source
   IOCLK, IOCLK/8, IOCLK/32, TM17IO pin input,
  Timer 14 underflow, Timer 15 underflow, Timer 16 underflow,

Watchdog Timer     Detection time       6.55 ms to 1677.72 ms
                                    (oscillation frequency 10 MHz )
          Generates non-maskable interrupts at detection
          Generates hard-reset at second consecutive overflow

A /D Converter

          A/D0
          - Resolution                    10 bits
          - Minimum conversion time       1.0 μsec
          - Channels                      6 channels (ADIN00 to ADIN05)
          - Use of 3 converters allows simultaneous sampling of 3 phases
          - A/D conversion start trigger is in synchronization with complementary 3-phase PWM
            cycle and 16-bit timer

          A/D1
          - Resolution                    10 bits
          - Minimum conversion time       1.0 μsec
          - Channels                      8 channels (ADIN02 to ADIN09)
          - Use of 3 converters allows simultaneous sampling of 3 phases
          - A/D conversion start trigger is in synchronization with complementary 3-phase PWM
            cycle and 16-bit timer

          A/D2

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- Resolution                    10 bits
- Minimum conversion time       1.0 µsec
- Channels                      10 channels (ADIN06 to ADIN15)
- Use of 3 converters allows simultaneous sampling of 3 phases
- A/D conversion start trigger is in synchronization with complementary 3-phase PWM
  cycle and 16-bit timer

Complementary 3-phase PWM output        2 channels
- Min. resolution: 33.3 nsec
- Triangular and saw-tooth waves output
- Incorporates a dead time insertion circuit
- Can overwrite registers by double buffer during PWM operation
- PWM output protection circuit supporting external interrupts
- Output timing varying function

Serial Interface        3 channels
Serial 0 (Full duplex UART/synchronous serial interface)
  Synchronous serial interface
  - Overrun error detection
  - Transfer clock source
    1/2 and 1/16 of timer 14 underflow, 1/2 and 1/16 of timer 15 underflow,
    and 1/2 and 1/16 of timer 16 underflow, SBT0 pin
  - Can be selected as the first bit to be transferred,
    Any transfer size from 7 to 8 bits can be selected.
  - Maximum transfer rate:  3.0 Mbps
  Full duplex UART
  - Overrun error, and flaming error detection
  - Transfer clock source
    1/16 of timer 14 underflow, 1/16 of timer 15 underflow,
    and 1/16 of timer 16 underflow,
  - Can be selected as the first bit to be transferred,
    Any transfer size from 7 to 8 bits can be selected.
  - Continuous transmission, reception, and transmission/reception
  - Maximum transfer rate:  375 kbps

Serial 1 (Full duplex UART/synchronous serial interface)
  Synchronous serial interface
  - Parity error, Overrun error detection
  - Transfer clock source
    1/2 and 1/16 of timer 14 underflow, 1/2 and 1/16 of timer 15 underflow,
    and 1/2 and 1/16 of timer 16 underflow, SBT1 pin
  - Can be selected as the first bit to be transferred,
    Any transfer size from 7 to 8 bits can be selected.
  - Maximum transfer rate:  3.0 Mbps
  Full duplex UART
  - Parity error, overrun error, and flaming error detection
  - Transfer clock source
    1/16 of timer 14 underflow, 1/16 of timer 15 underflow,
    and 1/16 of timer 16 underflow,
  - Can be selected as the first bit to be transferred,
    Any transfer size from 7 to 8 bits can be selected.
  - Continuous transmission, reception, and transmission/reception
  - Maximum transfer rate:  375 kbps

Serial 2 (Full duplex UART/synchronous serial interface)

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Synchronous serial interface
- Overrun error detection
- Transfer clock source
  1/2, 1/4, 1/16, and 1/64 of timer 14 underflow,
  1/2, 1/4, 1/16, and 1/64 of timer 15 underflow,
  1/2, 1/4, 1/16, and 1/64 of timer 16 underflow,
  IOCLK/2, IOCLK/4, SBT2 pin
- Can be selected as the first bit to be transferred,
  Any transfer size from 2 to 8 bits can be selected.
- Continuous transmission, reception, and transmission/reception
- Maximum transfer rate: 5.0 Mbps
Full duplex UART
- Parity error, overrun error and flaming error detection
- Transfer clock source
  1/32, 1/64, 1/256, and 1/1024 of timer 14 underflow,
  1/32, 1/64, 1/256, and 1/1024 of timer 15 underflow,
  1/32, 1/64, 1/256, and 1/1024 of timer 16 underflow,
  IOCLK/32, IOCLK/64
- Can be selected as the first bit to be transferred,
  Any transfer size from 7 to 8 bits can be selected.
- Continuous transmission, reception, and transmission/reception
- Maximum transfer rate: 300 kbps

Regulator              incorporates regulator, and use of 5 V power supply is possible

Power Supply Detection (Auto reset circuit)
                Detection level      3.6 V to 4.3 V
                When power supply voltage is under detection level, reset is generated.

PPort / pins      I/O ports                    61 pins
                   Motor control output        12 pins
                   External interrupt           9 pins
                   A/D input                   16 pins
                  Special pins                 19 pins
                   Reset input pin              1 pin
                   Oscillation pin              2 pins
                   Test pin                     4 pins
                   Power pin                   10 pins
                   N.C. pin                     2 pins

Package           LQFP80  (14 mm square, 0.65 mm pitch, halogen free)
Code name         LQFP080-P-1414E

Panasonic "halogen free" semiconductor products refer to the products made of molding resin and interposer
which conform to the following standards.
                - Bromine : 900 ppm (Maximum Concentration Value)
                - Chlorine : 900 ppm (Maximum Concentration Value)
                - Bromine + Chlorine : 1500 ppm (Maximum Concentration Value)
The above-mentioned standards are based on the numerical value described in IEC61249-2-21.
Antimony and its compounds are not added intentionally.
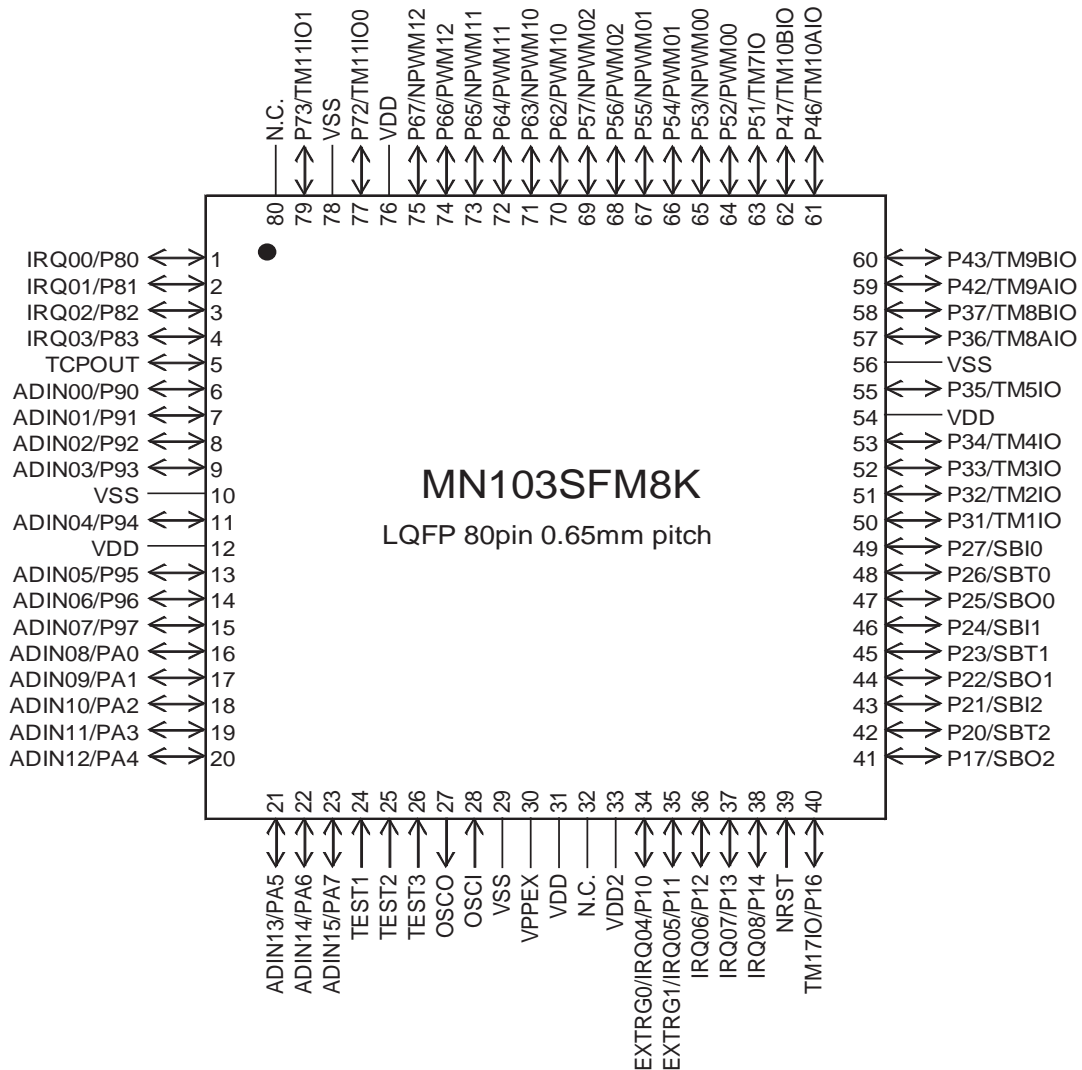
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# 1.3 Pin Description

## 1.3.1 Pin Configuration



Figure:1.3.1  Pin Configuration

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## 1.3.2 Pin Specification

Table:1.3.1 Pin Specification

| Pin | Special functions | I/O | Direction control | Pin control | Function description |
|---|---|---|---|---|---|
| NRST | - | in | - | - | Reset input |
| P10 | IRQ04/EXTRG0 | in/out | P10D | P10R | External interrupt input 4/ Trigger pin 0 for on-board debugging |
| P11 | IRQ05/EXTRG1 | in/out | P11D | P11R | External interrupt input 5/ Trigger pin 1 for on-board debugging |
| P12 | IRQ06 | in/out | P12D | P12R | External interrupt input 6 |
| P13 | IRQ07 | in/out | P13D | P13R | External interrupt input 7 |
| P14 | IRQ08 | in/out | P14D | P14R | External interrupt input 8 |
| P16 | TM17IO | in/out | P16D | P16R | Timer 17 input / output |
| P17 | SBO2 | in/out | P17D | P17R | Serial 2 transmission data output |
| P20 | SBT2 | in/out | P20D | P20R | Serial 2 clock I/O |
| P21 | SBI2 | in/out | P21D | P21R | Serial 2 reception data input |
| P22 | SBO1 | in/out | P22D | P22R | Serial 1 transmission data output |
| P23 | SBT1 | in/out | P23D | P23R | Serial 1 clock I/O |
| P24 | SBI1 | in/out | P24D | P24R | Serial 1 reception data input |
| P25 | SBO0 | in/out | P25D | P25R | Serial 0 transmission data output |
| P26 | SBT0 | in/out | P26D | P26R | Serial 0 clock I/O |
| P27 | SBI0 | in/out | P27D | P27R | Serial 0 reception data input |
| P31 | TM1IO | in/out | P31D | P31R | Timer 1 I/O |
| P32 | TM2IO | in/out | P32D | P32R | Timer 2 I/O |
| P33 | TM3IO | in/out | P33D | P33R | Timer 3 I/O |
| P34 | TM4IO | in/out | P34D | P34R | Timer 4 I/O |
| P35 | TM5IO | in/out | P35D | P35R | Timer 5 I/O |
| P36 | TM8AIO | in/out | P36D | P36R | Timer 8A I/O |
| P37 | TM8BIO | in/out | P37D | P37R | Timer 8B I/O |
| P42 | TM9AIO | in/out | P42D | P42R | Timer 9A I/O |
| P43 | TM9BIO | in/out | P43D | P43R | Timer 9B I/O |
| P46 | TM10AIO | in/out | P46D | P46R | Timer 10A I/O |
| P47 | TM10BIO | in/out | P47D | P47R | Timer 10B I/O |
| P51 | TM7IO | in/out | P51D | P51R | Timer 7 I/O |
| P52 | PWM00 | in/out | P52D | P52R | 3-phase PWM0 signal output 0 |
| P53 | NPWM00 | in/out | P53D | P53R | 3-phase PWM0 signal reverse output 0 |
| P54 | PWM01 | in/out | P54D | P54R | 3-phase PWM0 signal output 1 |
| P55 | NPWM01 | in/out | P55D | P55R | 3-phase PWM0 signal reverse output 1 |
| P56 | PWM02 | in/out | P56D | P56R | 3-phase PWM0 signal output 2 |
| P57 | NPWM02 | in/out | P57D | P57R | 3-phase PWM0 signal reverse output 2 |
| P62 | PWM10 | in/out | P62D | P62R | 3-phase PWM1 signal output 0 |
| P63 | NPWM10 | in/out | P63D | P63R | 3-phase PWM1 signal reverse output 0 |
| P64 | PWM11 | in/out | P64D | P64R | 3-phase PWM1 signal output 1 |
| P65 | NPWM11 | in/out | P65D | P65R | 3-phase PWM1 signal reverse output 1 |
| P66 | PWM12 | in/out | P66D | P66R | 3-phase PWM1 signal output 2 |
| P67 | NPWM12 | in/out | P67D | P67R | 3-phase PWM1 signal reverse output 2 |
| P72 | TM11IO0 | in/out | P72D | P72R | Timer 11 I/O 0 |
| P73 | TM11IO1 | in/out | P73D | P73R | Timer 11 I/O 1 |
| P80 | IRQ00 | in/out | P80D | P80R | External interrupt input 0 |
| P81 | IRQ01 | in/out | P81D | P81R | External interrupt input 1 |
| P82 | IRQ02 | in/out | P82D | P82R | External interrupt input 2 |
| P83 | IRQ03 | in/out | P83D | P83R | External interrupt input 3 |
| P90 | ADIN00 | in/out | P90D | P90R | AD analog signal input 0 |
| P91 | ADIN01 | in/out | P91D | P91R | AD analog signal input 1 |
| P92 | ADIN02 | in/out | P92D | P92R | AD analog signal input 2 |
| P93 | ADIN03 | in/out | P93D | P93R | AD analog signal input 3 |
| P94 | ADIN04 | in/out | P94D | P94R | AD analog signal input 4 |
| P95 | ADIN05 | in/out | P95D | P95R | AD analog signal input 5 |
| P96 | ADIN06 | in/out | P96D | P96R | AD analog signal input 6 |
| P97 | ADIN07 | in/out | P97D | P97R | AD analog signal input 7 |

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| Pin | Special functions | I/O | Direction control | Pin control | Function description |
|-----|-------------------|-----|-------------------|-------------|----------------------|
| PA0 | ADIN08 | in/out | PA0D | PA0R | AD analog signal input 8 |
| PA1 | ADIN09 | in/out | PA1D | PA1R | AD analog signal input 9 |
| PA2 | ADIN10 | in/out | PA2D | PA2R | AD analog signal input 10 |
| PA3 | ADIN11 | in/out | PA3D | PA3R | AD analog signal input 11 |
| PA4 | ADIN12 | in/out | PA4D | PA4R | AD analog signal input 12 |
| PA5 | ADIN13 | in/out | PA5D | PA5R | AD analog signal input 13 |
| PA6 | ADIN14 | in/out | PA6D | PA6R | AD analog signal input 14 |
| PA7 | ADIN15 | in/out | PA7D | PA7R | AD analog signal input 15 |

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## 1.3.3 Pin Functions

Table:1.3.2 Pin Functions

| Name | TQFP 48 Pin No. | I/O | Other Function | Function | Description |
|---|---|---|---|---|---|
| VDD<br>VDD<br>VDD<br>VDD | 12<br>31<br>54<br>76 | - | - | Power supply pin | Power pins for 5 V, digital IO<br>Apply 5 V to all of pins and connect capacitor of over 10 μF between all of the VDD and VSS pins.<br>It is recommended that total capacitance between all of the VDD and VSS is more than 10-times capacitance between all of the VDD2 and VSS. |
| VDD2 | 33 | - | - | Power supply pin | Power pins for 1.8 V, digital IO<br>Connect capacitor of over 1 μF between all of the VDD2 and VSS pins. |
| VSS<br>VSS<br>VSS<br>VSS | 10<br>29<br>56<br>78 | - | - | Power supply pin | GND for digital |
| VPPEX | 30 | - | | Power supply pin | Power for flash EEPROM<br>Connect with VDD. |
| OSC1<br>OSC0 | 28<br>27 | input<br>output | - | Clock input pin<br>Clock output pin | Extend ceramic or crystal oscillators or input a clock to OSC1. |
| NRST | 39 | input | - | Reset pins (negative logic) | This pin resets the chip when power is turned on and contains an internal pull-up resistor. Setting this pin "L" level initializes the internal state of the device. Thereafter, setting the input to "H" level releases the reset. The hardware waits for the system clock to stabilize, and processes the reset interrupt. Connect capacitor of over 0.1 μF between NRST and VSS pins. |
| P10<br>P11<br>P12<br>P13<br>P14<br>P16<br>P17 | 34<br>35<br>36<br>37<br>38<br>40<br>41 | I/O | IRQ04/ EXTRG0<br>IRQ05/ EXTRG1<br>IRQ06<br>IRQ07<br>IRQ08<br>TM7IO<br>SBO2 | I/O port 1 | 7-bit CMOS I/O ports.<br>Each bit can be set individually as either input or output by the P1DIR register.<br>Pull-up resistor for each bit can be selected individually by the P1PLU register.<br>At reset, the input mode (P10 to P14, P16, P17) is selected, and pull-up resistor is disabled. |
| P20<br>P21<br>P22<br>P23<br>P24<br>P25<br>P26<br>P27 | 42<br>43<br>44<br>45<br>46<br>47<br>48<br>49 | I/O | SBT2<br>SBI2<br>SBO1<br>SBT1<br>SBI1<br>SBO0<br>SBT0<br>SBI0 | I/O port 2 | 8-bit CMOS I/O ports.<br>Each bit can be set individually as either input or output by the P2DIR register.<br>Pull-up resistor for each bit can be selected individually by the P2PLU register.<br>At reset, the input mode (P20 to P27) is selected, and pull-up resistor is disabled. |
| P31<br>P32<br>P33<br>P34<br>P35<br>P36<br>P37 | 50<br>51<br>52<br>53<br>55<br>57<br>58 | I/O | TM1IO<br>TM2IO<br>TM3IO<br>TM4IO<br>TM5IO<br>TM8AIO<br>TM8BIO | I/O port 3 | 7-bit CMOS I/O ports.<br>Each bit can be set individually as either input or output by the P3DIR register.<br>Pull-up resistor for ech bit can be selected individually by the P3PLU register.<br>At reset, the input mode (P31 to P37) is selected, and pull-up resistor is disabled. |

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| Name | TQFP 48 Pin No. | I/O | Other Function | Function | Description |
|------|------|-----|----------------|----------|-------------|
| P42<br>P43<br>P46<br>P47 | 59<br>60<br>61<br>62 | I/O | TM9AIO<br>TM9BIO<br>TM10AIO<br>TM10BIO | I/O port 4 | 4-bit CMOS I/O port.<br>Each bit can be set individually as either input or output by the P4DIR register.<br>Pull-up resistor for each bit can be selected individually by the P4PLU register.<br>At reset, the input mode (P42, P43, P46, P47) is selected and pull-up resistor is disabled. |
| P51<br>P52<br>P53<br>P54<br>P55<br>P56<br>P57 | 63<br>64<br>65<br>66<br>67<br>68<br>69 | I/O | TM7IO<br>PWM00<br>NPWM00<br>PWM01<br>NPWM01<br>PWM02<br>NPWM02 | I/O port 5 | 7-bit CMOS I/O ports.<br>Each bit can be set individually as either input or output by the P5DIR register.<br>Pull-up resistor for each bit can be selected individually by the P5PLU register.<br>At reset, the input mode (P51 to P57) is selected, and pull-up resistor is disabled. |
| P62<br>P63<br>P64<br>P65<br>P66<br>P67 | 70<br>71<br>72<br>73<br>74<br>75 | I/O | PWM10<br>NPWM10<br>PWM11<br>NPWM11<br>PWM12<br>NPWM12 | I/O port 6 | 6-bit CMOS I/O ports.<br>Each bit can be set individually as either input or output by the P6DIR register.<br>Pull-up resistor for each bit can be selected individually by the P6PLU register.<br>At reset, the input mode (P62 to P67) is selected, and pull-up resistor is disabled. |
| P72<br>P73 | 77<br>79 | I/O | TM11IO0<br>TM11IO1 | I/O port 7 | 2-bit CMOS I/O ports.<br>Each bit can be set individually as either input or output by the P7DIR register.<br>P pull-up resistor for each bit can be selected individually by the P7PLU register.<br>At reset, the input mode (P72, P73) is selected, and pull-up resistor is disabled. |
| P80<br>P81<br>P82<br>P83 | 1<br>2<br>3<br>4 | I/O | IRQ00<br>IRQ01<br>IRQ02<br>IRQ03 | I/O port 8 | 4-bit CMOS input ports.<br>Each bit can be set individually as either input or output by the P8PLU register.<br>Pull-up resistor for each bit can be selected individually by the P8PLU register.<br>At reset, the input mode (P80 to P83) is selected, and pull-up resistor is disabled. |
| P90<br>P91<br>P92<br>P93<br>P94<br>P95<br>P96<br>P97 | 6<br>7<br>8<br>9<br>11<br>13<br>14<br>15 | I/O | ADIN00<br>ADIN01<br>ADIN02<br>ADIN03<br>ADIN04<br>ADIN05<br>ADIN06<br>ADIN07 | I/O port 9 | 8-bit CMOS input ports.<br>Each bit can be set individually as either input or output by the P9DIR register.<br>Pull-up resistor for each bit can be selected individually by the P9PLU register.<br>At reset, the input mode (P90 to P97) is selected, and pull-up resistor is disabled. |
| PA0<br>PA1<br>PA2<br>PA3<br>PA4<br>PA5<br>PA6<br>PA7 | 16<br>17<br>18<br>19<br>20<br>21<br>22<br>23 | I/O | ADIN08<br>ADIN09<br>ADIN10<br>ADIN11<br>ADIN12<br>ADIN13<br>ADIN14<br>ADIN15 | I/O port A | 8-bit CMOS input ports.<br>Each bit can be set individually as either input or output by the PADIR register.<br>Pull-up resistor for each bit can be selected individually by the PAPLU register.<br>At reset, the input mode (PA0 to PA7) is selected, and pull-up resistor is disabled. |
| SB00<br>SB01<br>SB02 | 47<br>44<br>41 | Output | P25<br>P22<br>P17 | Serial interface transmission data output pin | Transmission data output pins for serial interface 0, 1, and 2.<br>Select output by the P1DIR and P2DIR registers and serial pin function by the P1MD and P2MD registers.<br>These can be used as normal I/O pins when serial interfaces are not used. |

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| Name | TQFP 48 Pin No. | I/O | Other Function | Function | Description |
|------|------|------|------|------|------|
| SBI0<br>SBI1<br>SBI2 | 49<br>46<br>43 | Input | P27<br>P24<br>P21 | Serial interface reception data input pin | Reception data input pins for serial interface 0, 1, and 2.<br>Pull-up resistor can be selected by the P2PLU register. Select input by the P2DIR register.<br>These can be used as normal I/O pins when serial interfaces are not used. |
| SBT0<br>SBT1<br>SBT2 | 48<br>45<br>42 | I/O | P26<br>P23<br>P20 | Serial interface clock I/O pin | Clock I/O pins for serial interface 0, 1, and 2.<br>Pull-up resistor can be selected by the P2PLU register. Select either input or output by the P2DIR register and serial pin function by the P2MD register.<br>These can be used as normal I/O pins when serial interfaces are not used. |
| TM1IO<br>TM2IO<br>TM3IO<br>TM4IO<br>TM5IO<br>TM7IO<br>TM17IO | 50<br>51<br>52<br>53<br>55<br>63<br>40 | I/O | P31<br>P32<br>P33<br>P34<br>P35<br>P51<br>P16 | Timer I/O pin | Event counter input and timer pulse output pins for 8-bit timer 1 to 5, 7 and 17.<br>At event count input, input mode dan be selected by the P1, 3 and 5DIR registers. At input mode, pull-up resistor can be selected by the P1, 3 and 5PLU registers.<br>At  timer pulse output, selected  timer output pins by the P1,3 and 5MD registers and set output mode by the P1,3 and 5DIR registers.<br>These can be used as normal I/O pins when these are not used as timer I/O pins. |
| TM8AIO<br>TM8BIO<br>TM9AIO<br>TM9BIO<br>TM10AIO<br>TM10BIO<br>TM11IO0<br>TM11IO1 | 57<br>58<br>59<br>60<br>61<br>62<br>77<br>79 | I/O | P36<br>P37<br>P42<br>P43<br>P46<br>P47<br>P72<br>P73 | Timer I/O pin | Event counter input, timer output, and PWM output pins for 16-bit timer 8 to 11.<br>At event counte input,  input mode can be selected by the P3, 4, and 7DIR registers. At input mode, pull-up resistor can be selected by the P3, 4, and 7PLU register.<br>At timer output and PWM output, select timer output pins by the P3, 4, and 7MD registers, and set output mode by the P3, 4, and 7DIR register.<br>These can be used as normal I/O pins when these are not used as timer I/O pins. |
| TM11IO0<br>TM11IO1 | 77<br>79 | Output | P72<br>P73 | PWM output pin | Motor control PWM signal output pins for 16-bit timer 11. These output PWM signals for 16-bit timer 11 to 2 pins simultaneously.<br>At PWM output, select  timer output pin by the P7MD register and set to output mode by the P7DIR register.<br>These can be used as normal I/O pins when these are not used as timer I/O pins. |
| ADIN00<br>ADIN01<br>ADIN02<br>ADIN03<br>ADIN04<br>ADIN05<br>ADIN06<br>ADIN07<br>ADIN08<br>ADIN09<br>ADIN10<br>ADIN11<br>ADIN12<br>ADIN13<br>ADIN14<br>ADIN15 | 6<br>7<br>8<br>9<br>11<br>13<br>14<br>15<br>16<br>17<br>18<br>19<br>20<br>21<br>22<br>23 | Input | P90<br>P91<br>P92<br>P93<br>P94<br>P95<br>P96<br>P97<br>PA0<br>PA1<br>PA2<br>PA3<br>PA4<br>PA5<br>PA6<br>PA7 | Analogue input pin | Analogue input pins for 16-channel, 10-bit 3 A/D converters.<br>These can be used as normal I/O pins when these are not used as analog input. |

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| Name | TQFP 48 Pin No. | I/O | Other Function | Function | Description |
|------|------|------|------|------|------|
| IRQ00<br>IRQ01<br>IRQ02<br>IRQ03<br>IRQ04<br>IRQ05<br>IRQ06<br>IRQ07<br>IRQ08 | 1<br>2<br>3<br>4<br>34<br>35<br>36<br>37<br>38 | Input | P80<br>P81<br>P82<br>P83<br>P10/ EXTRG0<br>P11/ EXTRG1<br>P12<br>P13<br>P14 | External interrupt pin | External interrupt input pins.<br>The valid edge can be selected. Set whether both edges are detected or not by the edge detection register (IRQEDGESEL). When it is set not to detect both edges, select rising edge, falling edge, H level, or L level by the external interrupt condition specification register (EXTMD0 and EXTMD1). When it is set to detect both edges, select rising edge by the external interrupt condition setting register. |
| PWM00<br>PWM01<br>PWM02<br>PWM10<br>PWM11<br>PWM12 | 64<br>66<br>68<br>70<br>72<br>74 | Output | P52<br>P54<br>P56<br>P62<br>P64<br>P66 | Motor control PWM signal output pin | Motor control 3-phase PWM signal output pins.<br>Select PWM signal output pins by the P5MD and P6MD registers and set PWM output by the PWM off registers.<br>These can be used as normal I/O pins when these are not used as PWM signal output pins. |
| NPWM00<br>NPWM01<br>NPWM02<br>NPWM11<br>NPWM12<br>NPWM13 | 65<br>67<br>69<br>71<br>73<br>75 | Output | P53<br>P55<br>P57<br>P63<br>P65<br>P67 | Motor control PWM signal reverse output pin | Motor control 3-phase PWM signal revers output pins.<br>Select PWM signal output pins by the P5MD and P6MD registers and set PWM output by the PWM off registers.<br>These can be used as normal I/O pins when these are not used as PWM signal output pins. |
| TCPOUT | 5 | Input | - | Test signal input | Test signal input pin. Fix at VSS. |
| TEST1<br>TEST2<br>TEST3 | 24<br>25<br>26 | Input | - | Test signal input | Test signal input pins built-in pull-up resistor. Pull-up with resistor of over 1 kΩ. |

⚠ VPPEX is power supply for flash EEPROM rewriting. Its potential should be the same as VDD.

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# 1.4   Block Diagram
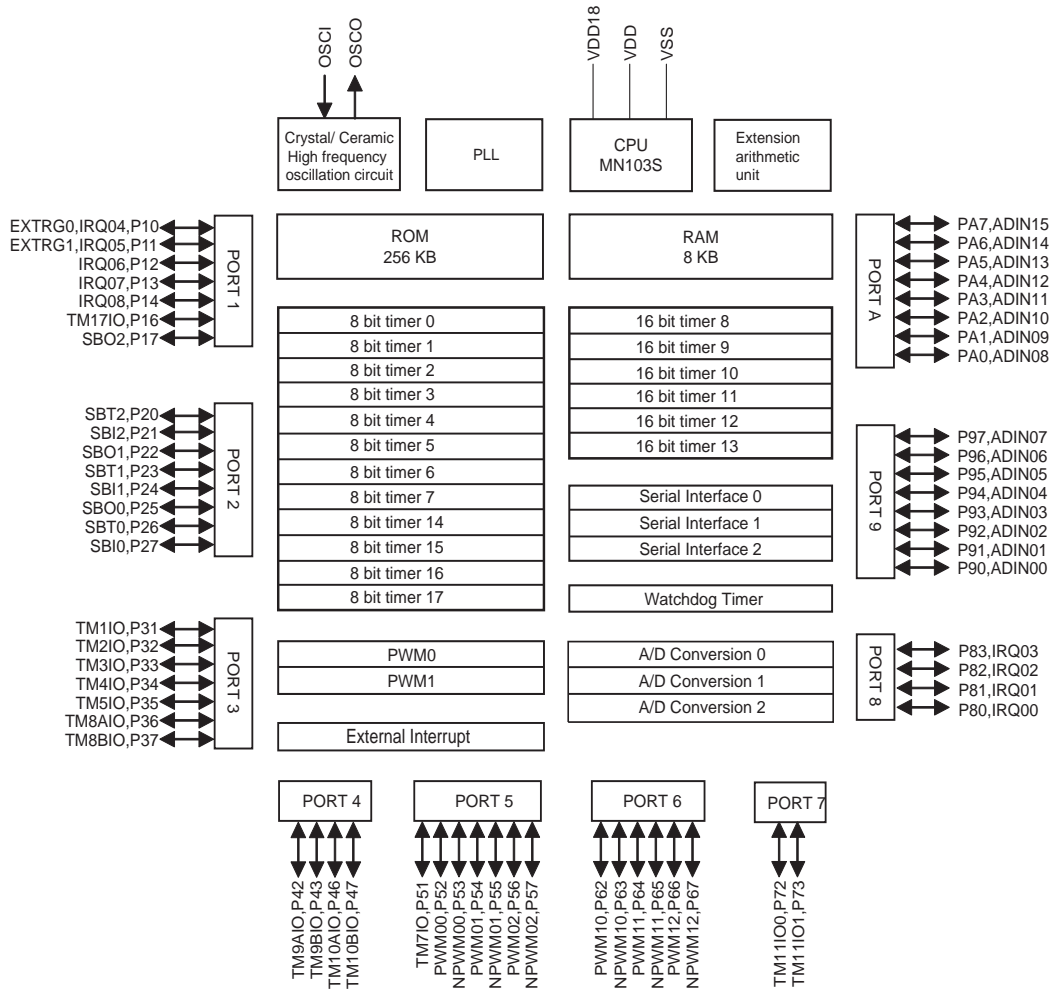
## 1.4.1     Block Diagram



Figure:1.4.1  Block Diagram

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# 1.5  Electrical Characteristics

This LSI manual describes the standard specification.

Electrical characteristics given in this section are preliminary and subject to change without notice. When using LSI, contact our sales office for product specifications.

| Model | CMOS  LSI |
|---|---|
| Application | General-purpose |
| Function | CMOS 32-bit 1 chip microcontroller |

## 1.5.1    Absolute Maximum Ratings

$V_{SS}$=0.0 V

| | Parameter | Symbol | Rating | Unit |
|---|---|---|---|---|
| A1 | External supply voltage | $V_{DD}$ | -0.3 to +7.0 | V |
| A2 | Internal supply voltage | $V_{DD2}$ | -0.3 to +2.5 | V |
| A3 | Input pin voltage | $V_{I1}$ | -0.3 to $V_{DD}$ +0.3 (upper limit: 7.0) | V |
| A4 | I/O pin voltage | $V_{IO}$ | -0.3 to $V_{DD}$ +0.3 (upper limit: 7.0) | V |
| A5 | Peak output current | $I_{OPEAK}$ | ±15 | mA |
| A6 | Typ. range output current | $I_{OAVG}$ | ±8 | mA |
| A7 | Operating ambient temperature | $T_{OPR}$ | -40 to +85 | °C |
| A8 | Storage temperature | $T_{STG}$ | -40 to +125 | °C |
| A9 | Power dissipation | $P_D$ | 500 | mW |

Note:  The absolute maximum ratings are the limit values beyond which the LSI may be damaged. It is not guarantee the operation in these conditions. The rating of the average output current is applied for the period of any 100 ms.

Note:  It cannot supply the internal power supply voltage to a circuit except this LSI.

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## 1.5.2    Operating Conditions

$V_{SS}=0.0$ V
Ta= -40 °C to +85 °C

| Parameter | | Symbol | Conditions | Limits | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min. | Typ. | Max. | |
| B1 | External supply voltage1 | $V_{DD}$ | - | $V_{RST}$ | 5.0 | 5.5 | V |

Note)  For power supply detection level $V_{RST}$, refer to "Auto reset circuit characteristics".

$V_{DD} = V_{RST}$ to 5.5 V
$V_{SS} = 0.0$ V
Ta= -40 °C to +85 °C

Oscillation

| Parameter | | Symbol | Conditions | Limits | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min. | Typ. | Max. | |
| B2 | Input frequency | $F_{OSC}$ | - | 5.0 | - | 15 | MHz |
| B3 | Internal feedback resistor | $R_{FB}$ | - | - | 1.2 | - | MΩ |

Note) Capacity value differs depending on oscillators to be used. Consult the oscillator mamufacture for the appropriate circuit constant.
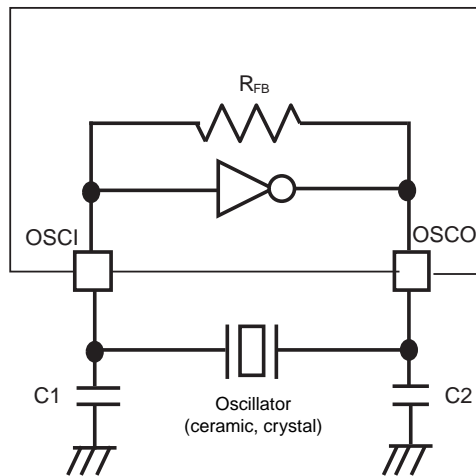


Figure:1.5.1  Oscillation

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<div align="right">

$V_{DD}$ = 5.0 V
$V_{SS}$ = 0.0 V
Ta= -40 °C to +85 °C

</div>

| Parameter | | Symbol | Conditions | Limits | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min. | Typ. | Max. | |
| External clock input 1 OSCI (OSCO left open) | | | | | | | |
| B4 | Clock frequency | Fcp | - | 5.0 | - | 15.0 | MHz |
| B5 | High-level pulse width | twh1 | Figure:1.5.2 | 25.0 | - | - | ns |
| B6 | Low-level pulse width | twl1 | Figure:1.5.2 | 25.0 | - | - | ns |
| B7 | Rise time | twr1 | Figure:1.5.2 | - | - | 5.0 | ns |
| B8 | Fall time | twf1 | Figure:1.5.2 | - | - | 5.0 | ns |

Note: Be sure that the clock duty ratio is 45 % to 55 %.
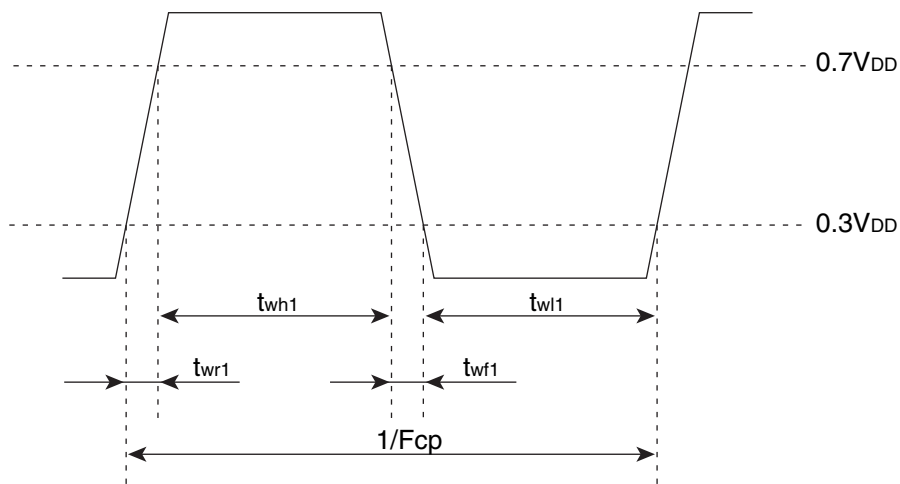


Figure:1.5.2  OSCI Timing Chart

## 1.5.3　DC Characteristics

$V_{SS}$=0.0 V
Ta= -40 °C to +85 °C
Output pin left open

DC Characteristics

| | Parameter | Symbol | Conditions | Limits | | Unit |
|---|---|---|---|---|---|---|
| | | | | Typ. | Max. | |
| C1 | Power supply current in NORMAL mode | $I_{DD1}$ | $V_{DD}$ = 5.0 V<br>$F_{OSC}$ = 10 MHz<br>PLL is used.<br>MCLK= 60 MHz, IOCLK =30 MHz<br>Peripheral circuits are stopped. | 20 | - | mA |
| C2 | | $I_{DD2}$ | $V_{DD}$ = 5.0 V<br>$F_{OSC}$ = 10 MHz<br>PLL is used.<br>MCLK= 60 MHz, IOCLK =30 MHz<br>Peripheral circuits are operating. | - | 35 | mA |

$V_{DD}$ =  5.0 V
$V_{SS}$ =  0.0 V
Ta= -40 °C to +85 °C

| | Parameter | Symbol | Conditions | Limits | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min. | Typ. | Max. | |
| Input pins1 NRST, TEST1, TEST2 | | | | | | | |
| C3 | Input voltage High level | $V_{IH1}$ | - | $V_{DD}$ x 0.7 | - | $V_{DD}$ | V |
| C4 | Input voltage Low level | $V_{IL1}$ | - | $V_{SS}$ | - | $V_{DD}$ x 0.3 | V |
| C5 | Internal Pull-up resistor | $R_{IO1}$ | $V_{DD}$ =5.0 V, $V_{IN}$ = 0 V | 15 | 30 | 60 | kΩ |

$V_{DD}$ = 5.0 V
$V_{SS}$ = 0.0 V
Ta= -40 °C to +85 °C

| | Parameter | Symbol | Conditions | Limits | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min. | Typ. | Max. | |
| Input pins 2 VPPEX, TEST3 | | | | | | | |
| C6 | Input voltage High level | $V_{IH2}$ | - | $V_{DD}$ x 0.7 | - | $V_{DD}$ | V |
| C7 | Input voltage Low level | $V_{IL2}$ | - | $V_{SS}$ | - | $V_{DD}$ x 0.3 | V |

$V_{DD}$ = 5.0 V
$V_{SS}$ = 0.0 V
Ta= -40 °C to +85 °C

| Parameter | | Symbol | Conditions | Limits | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min. | Typ. | Max. | |
| I/O pin P10 to P14, P16, P17, P20 to P27, P31 to P37, P42, P43, P46, P47, P51 to P57, P62 to P67, P72, P73, P80 to P83, P85, P90 to P97, PA0 to PA7 | | | | | | | |
| C8 | Input voltage High level | $V_{IH4}$ | – | $V_{DD}$ x 0.7 | - | $V_{DD}$ | V |
| C9 | Input voltage Low level | $V_{IL4}$ | – | $V_{SS}$ | - | $V_{DD}$ x 0.3 | V |
| C10 | Input leak current | $I_{LK4}$ | – | - | - | ± 5 | μA |
| C11 | Internal pull-up resistor | $R_{IO4}$ | $V_{DD}$ = 5.0 V, $V_{IN}$ = 0 V | 15 | 30 | 60 | kΩ |
| C12 | Output voltage High level | $V_{OH4}$ | $V_{DD}$ = 5.0 V, $I_{OH}$ = -2.5 mA | 4.5 | - | - | V |
| C13 | Output voltage Low level | $V_{OL4}$ | $V_{DD}$ = 5.0 V, $I_{OL0}$ = 2.5 mA | - | - | 0.5 | V |

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## 1.5.4    Analog Characteristics

A/D0, A/D1, A/D2

| | Parameter | Symbol | Conditions | Limits | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min. | Typ. | MAx. | |
| D1 | Resolution | - | - | - | - | 10 | Bits |
| D2 | Non-linearity error | INLE | Sampling time ≥ 150 ns A/D conversion clock ≤ 30 MHz | - | - | ±2 | LSB |
| D3 | Differential linearity error | DNLE | | - | - | ±3 | LSB |
| D4 | Zero transition voltage | - | | -20 | - | 20 | mV |
| D5 | Full-scale transition voltage | - | | 4980 | - | 5020 | mV |
| D6 | A/D conversion time | - | - | 1.0 | - | - | μs |
| D7 | Analog input voltage | $V_{IA}$ | - | $V_{SS}$ | - | $V_{DD}$ | V |
| D8 | Analog input leakage current | $I_{IA}$ | Unselected channel $V_{ADIN}$ = 0 V to $V_{DD}$ | - | - | ±5 | μA |
| D9 | Power supply current during operation (VDD pin) | $I_{AD}$ | A/D conversion clock = 30 MHz | - | 1 | - | mA |

Auto-reset

| | Parameter | Symbol | Conditions | Limits | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min. | Typ. | MAx. | |
| D10 | Power supply voltage detection level1 | $V_{RST1}$ | At rising | 3.6 | 3.95 | 4.3 | V |
| D11 | Power supply voltage detection level2 | $V_{RST2}$ | At falling | 3.5 | 3.85 | 4.2 | V |
| D12 | Change rate of power supply voltage | $\Delta V_{DD}$ | - | 0.2 | - | - | ms/V |

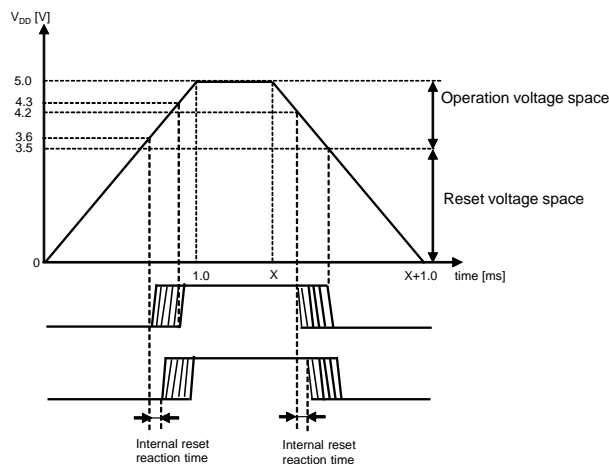Note:  Connect 0.1 μF capacitor between NRST and VSS pins. .



Figure:1.5.3  Auto Reset Circuit Characteristics

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## 1.5.5    AC Characteristics

Reset signal input timing

$V_{DD}$ = 5.0 V
$V_{SS}$ = 0.0 V
Ta= -40 °C to +85 °C

| Parameter | | Symbol | Conditions | Limits | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min. | Typ. | Max. | |
| E1 | Reset signal pulse width (NRST) | $t_{NRSTW}$ | - | 1 | - | - | μs |

NRST

$t_{NRSTW}$
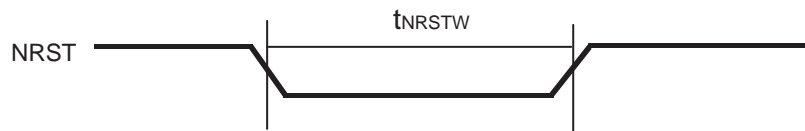
Figure:1.5.4  Reset Signal Pulse Width

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## 1.5.6 Flash EEPROM E/W Characteristics

$V_{SS} = 0.0$ V

| Parameter | | Symbol | Conditions | Limits | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | |
| F1 | Power supply voltage at E/W | $V_{DDEW}$ | | $V_{RST}$ | - | 5.5 | V |
| F2 | Ambient temperature at E/W | $V_{OPREW}$ | | -40 | - | 85 | °C |
| F3 | Permissible rewriting times | $E_{MAX1}$ | Large sector (32 KB) | 1,000 | - | - | Times |
| F4 | Permissible rewriting times | $E_{MAX2}$ | Small sector (8 KB) | 100,000 | - | - | Times |
| F5 | Data retention time | $T_{HOLD}$ | | 10 | - | - | Years |

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# 1.6   Package Dimension

PACKAGE CODE: LQFP080-P-1414E

UNIT : m m
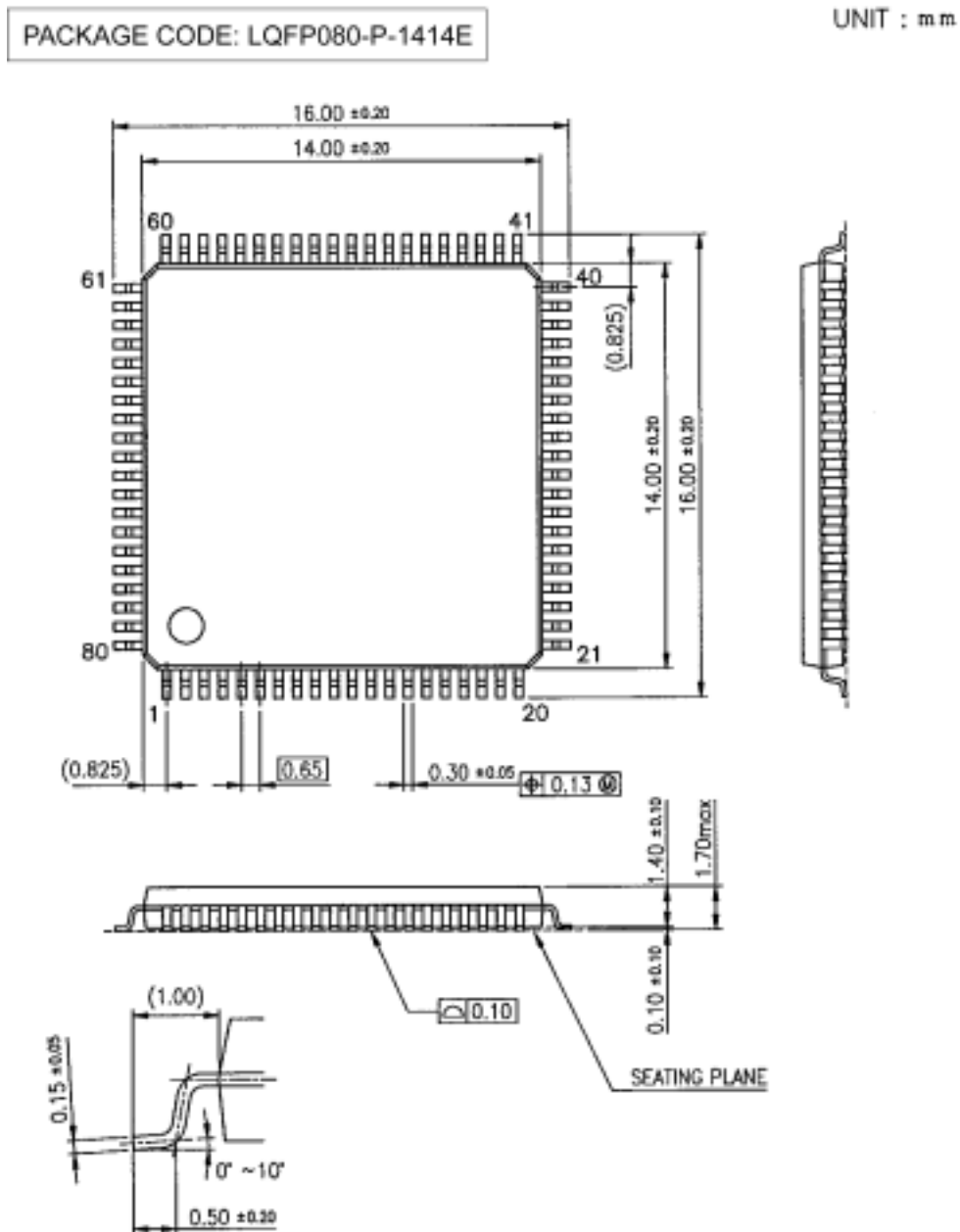


Figure:1.6.1  Package Dimension

⚠ The external dimensions of the package are subject to change. Before using this product, please obtain product specifications from the sales offices.

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