

Notification about the transfer of the semiconductor business

The semiconductor business of Panasonic Corporation was transferred on September 1, 2020 to Nuvoton Technology Corporation (hereinafter referred to as "Nuvoton"). Accordingly, Panasonic Semiconductor Solutions Co., Ltd. became under the umbrella of the Nuvoton Group, with the new name of Nuvoton Technology Corporation Japan (hereinafter referred to as "NTCJ").

In accordance with this transfer, semiconductor products will be handled as NTCJ-made products after September 1, 2020. However, such products will be continuously sold through Panasonic Corporation.

Publisher of this Document is NTCJ.

If you would find description "Panasonic" or "Panasonic semiconductor solutions", please replace it with NTCJ.

※ Except below description page

"Request for your special attention and precautions in using the technical information and semiconductors described in this book"

Nuvoton Technology Corporation Japan

MTM764200LBF

Dual P-channel MOS FET

For switching

■ Features

- Low Drain-source On-state Resistance: $R_{DS(on)typ} = 100\text{ m}\Omega$ ($V_{GS} = -4.0\text{ V}$)
- Low drive voltage: 1.8 V drive
- Halogen-free / RoHS compliant
(EU RoHS / UL-94 V-0 / MSL:Level 1 compliant)

■ Marking Symbol: JC

■ Basic Part Number

Dual Pch MOS 20 V (Individual)

■ Packaging

MTM764200LBF Embossed type (Thermo-compression sealing):
3 000 pcs / reel (standard)

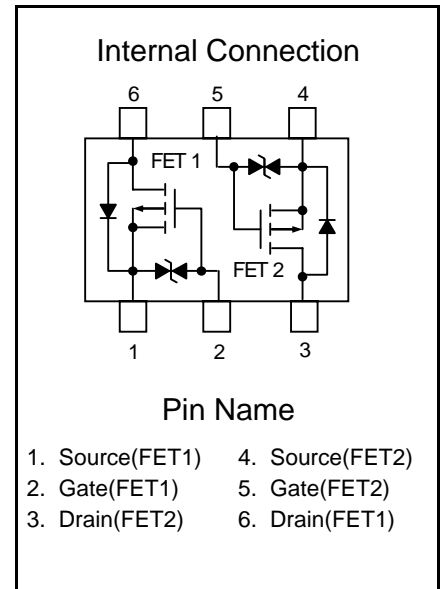
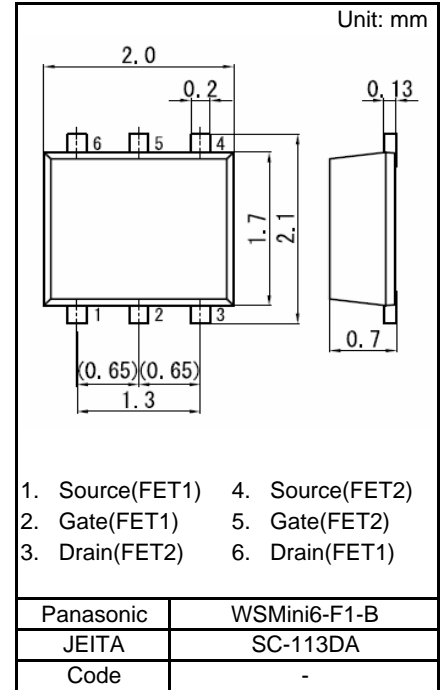
■ Absolute Maximum Ratings $T_a = 25\text{ }^\circ\text{C}$

Parameter		Symbol	Rating	Unit
FET1	Drain-source Voltage	VDS	-20	V
	Gate-source Voltage	VGS	± 10	V
FET2	Drain current	ID	-1.2	A
	Drain current (Pulsed) ^{*1}	IDp	-7	A
Overall	Total Power Dissipation ^{*2}	PD	700	mW
	Channel Temperature	Tch	150	$^\circ\text{C}$
	Storage Temperature	Tstg	-55 to +150	$^\circ\text{C}$

Note: *1 $t = 10\text{ }\mu\text{s}$, Duty cycle $\leq 1\%$

*2 Measuring on ceramic substrate at $40\text{ mm} \times 38\text{ mm} \times 0.2\text{ mm}$.

PD absolute maximum rating Non-heat sink: 150 mW.



■ Electrical Characteristics Ta = 25 °C ± 3 °C
FET1,FET2

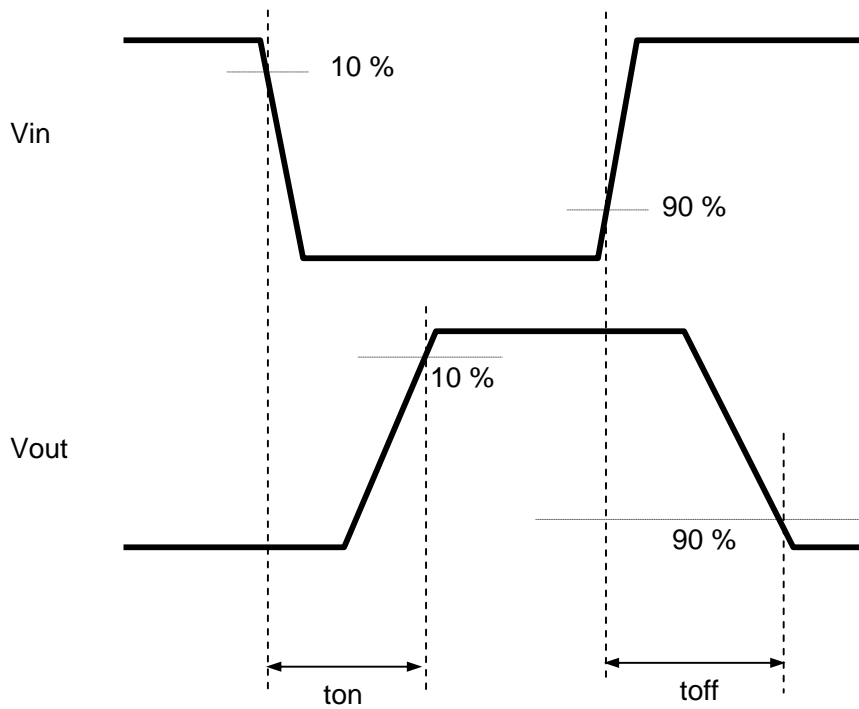
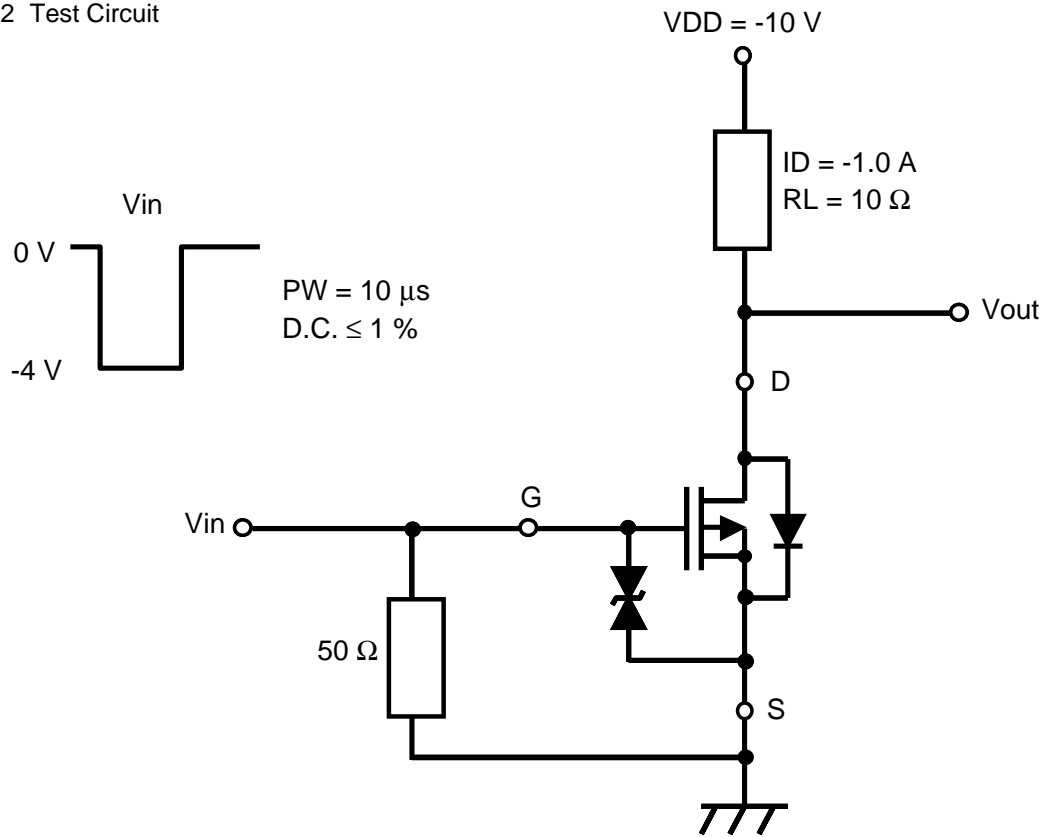
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Drain-source Breakdown Voltage	VDSS	ID = -1.0 mA, VGS = 0 V	-20			V
Zero Gate Voltage Drain Current	IDSS	VDS = -20 V, VGS = 0 V			-1.0	μA
Gate-source Leakage Current	IGSS	VGS = ±8.0 V, VDS = 0 V			±10	μA
Gate-source Threshold Voltage	Vth	ID = -1.0 mA, VDS = -10 V	-0.40	-0.85	-1.30	V
Drain-source On-state Resistance *1	RDS(on)1	ID = -1.0 A, VGS = -4.0 V		100	130	mΩ
	RDS(on)2	ID = -0.6 A, VGS = -2.5 V		130	200	
	RDS(on)3	ID = -0.2 A, VGS = -1.8 V		150	280	
Forward transfer admittance *1	Yfs	ID = -1.0 A, VDS = -10 V, f = 1 kHz	3.0			S
Input Capacitance	Ciss	VDS = -10 V, VGS = 0 V, f = 1 MHz		440		pF
Output Capacitance	Coss			40		
Reverse Transfer Capacitance	Crss			38		
Turn-on Time *2	ton	VDD = -10 V, VGS = 0 to -4 V, ID = -1.0 A		35		ns
Turn-off Time *2	toff	VDD = -10 V, VGS = -4 to 0 V, ID = -1.0 A		100		ns

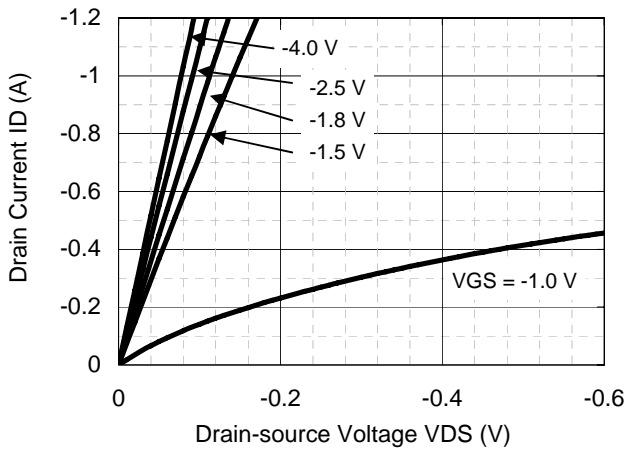
Note Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030 Measuring methods for transistors.

*1 Pulse Test

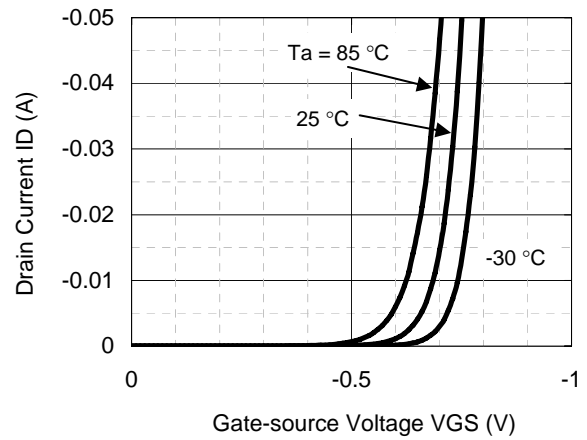
*2 See Test circuit.

*2 Test Circuit

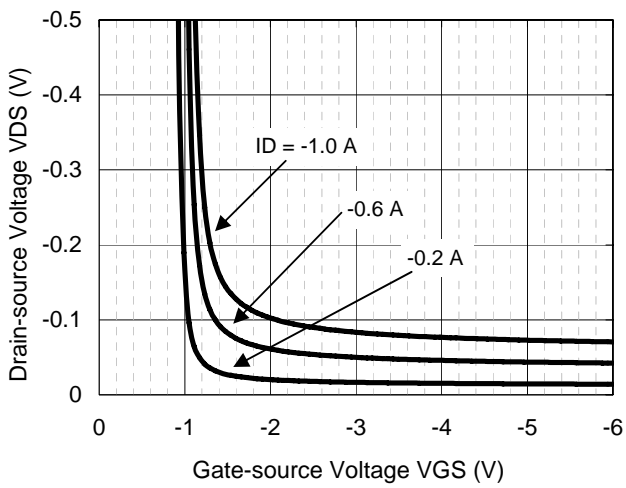




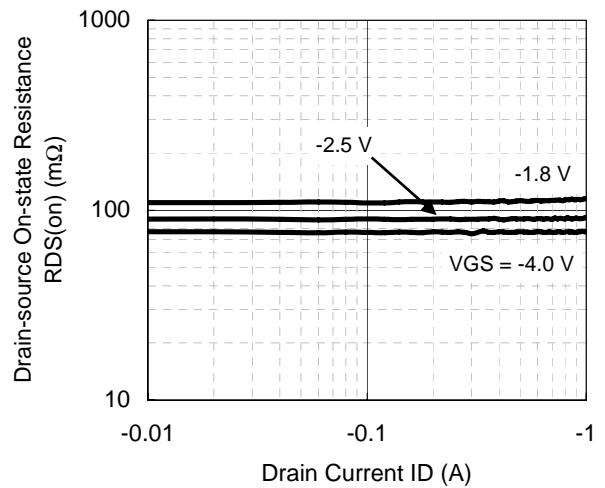
ID - VDS



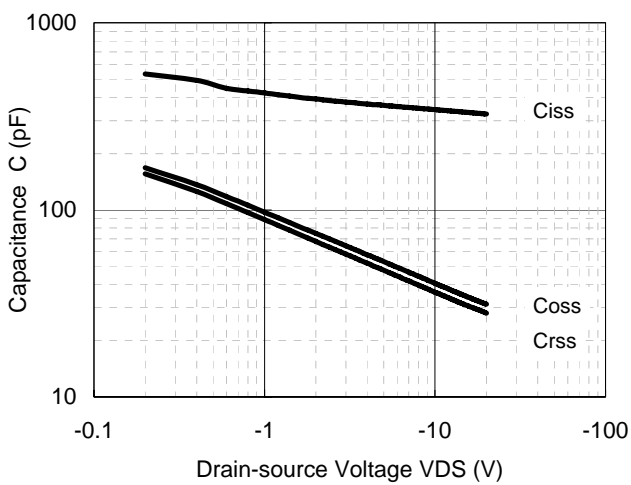
ID - VGS



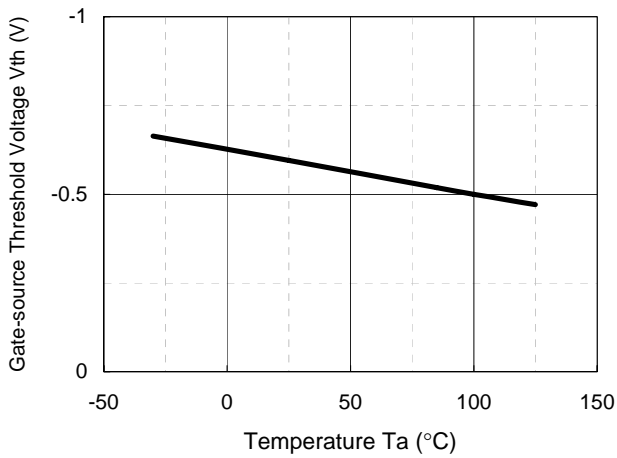
VDS - VGS



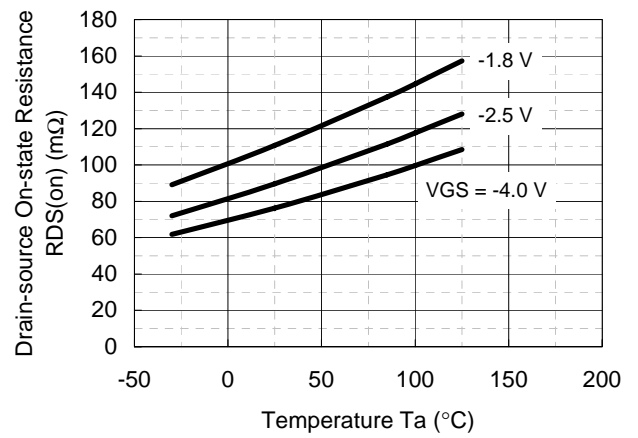
RDS(on) - ID



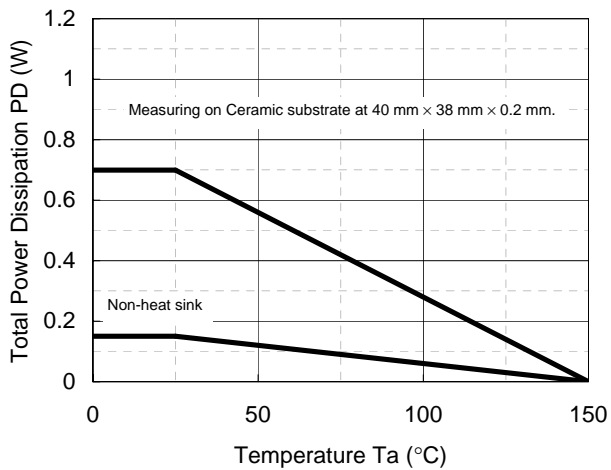
Capacitance - VDS



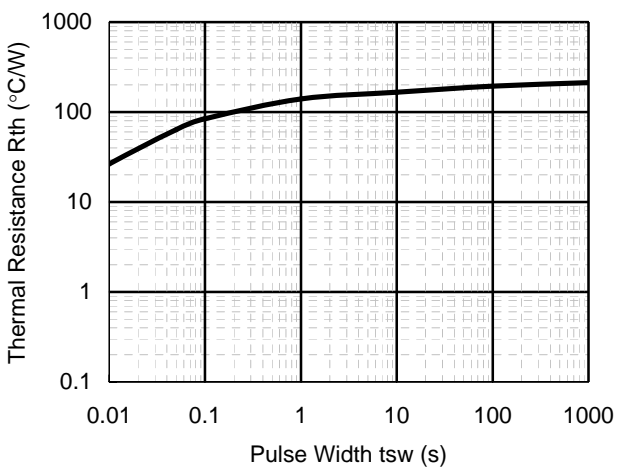
V_{th} - T_a



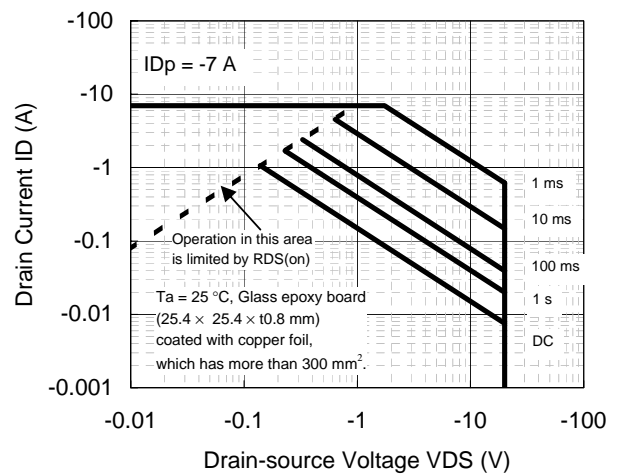
$R_{DS(on)}$ - T_a



P_D - T_a



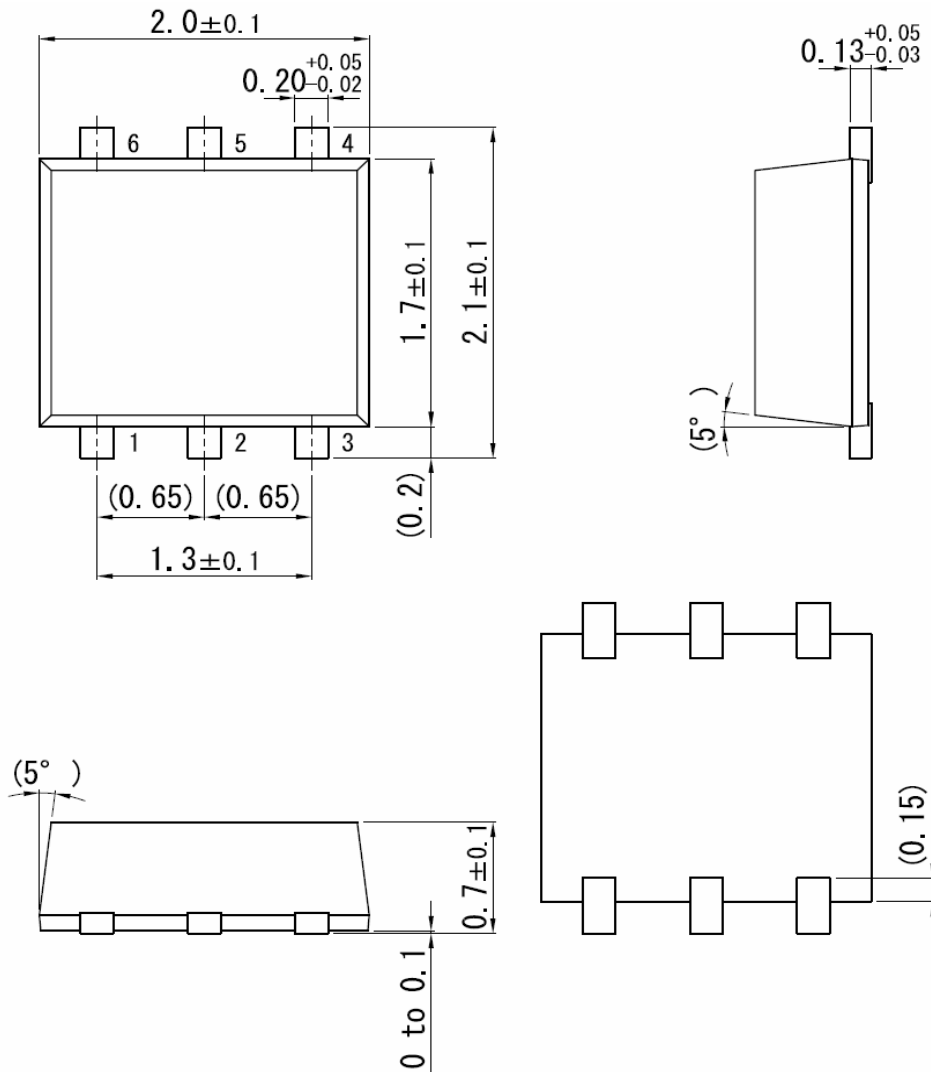
R_{th} - t_{sw}



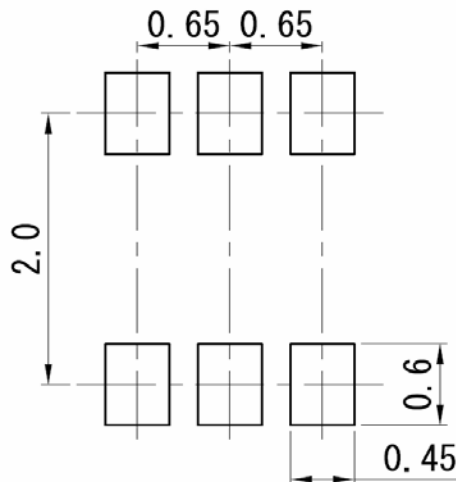
Safe Operating Area

WSMini6-F1-B

Unit: mm



■ Land Pattern (Reference) (Unit: mm)



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