MTMF8231

Silicon N-channel MOSFET

For Li-ion battery protection circuit

■ Overview

MTMF8231 is low R_{on} N-channel MOSFET designed for Li-ion battery circuit of notebook computers.

■ Features

- Super Low on resistance: R_{on} = 3 mΩ (typ.) (V_{GS} = 10 V, I_D = 5.0 A)
- Thin flat-lead package
- Incorporating a built-in gate protection-diode

■ Absolute Maximum Ratings T_a = 25°C

Parameter	Symbol	Rating	Unit
Drain-source surrender voltage	V_{DSS}	30	V
Gate-source surrender voltage	V_{GSS}	±20	V
Drain current	I_D	18	A
Peak drain current	I_{DP}	72	A
Avalanche current	IAS	18	A
Power dissipation *	P_D	1.0	W
Channel temperature	T_{ch}	150	°C
Storage temperature	T_{stg}	–55 to +150	°C

Note) *: Measuring on cglass epoxy board at 25.4 mm × 25.4 mm × 0.8 mm
Absolute maximum rating without heat sink for P_D is 500 mA

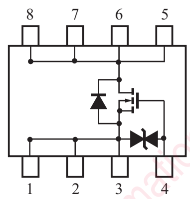
■ Package

- Code
  SO8-F1-B
- Pin Name

1: Source	2: Source
3: Source	4: Gate
5: Drain	6: Drain
7: Drain	8: Drain

■ Marking Symbol: AA

■ Internal Connection

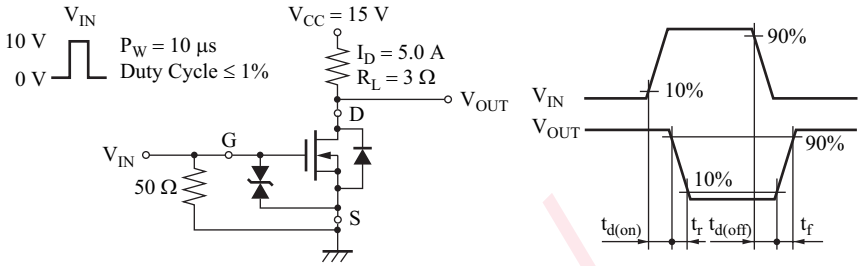


■ Electrical Characteristics T_a = 25°C±3°C

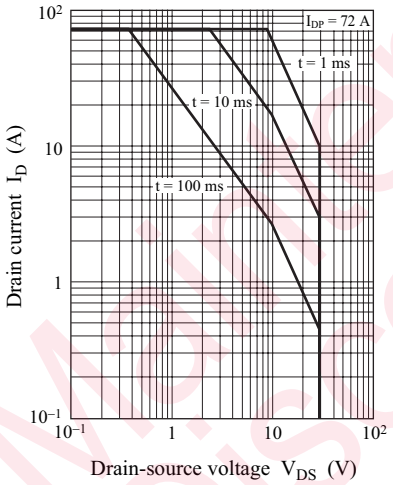
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Drain-source surrender voltage	V_{DSS}	I_D = 1 mA, V_{GS} = 0	30			V
Drain-source cutoff current	I_{DSS}	V_{DS} = 30 V, V_{GS} = 0			10	μA
Gate-source cutoff current	I_{GSS}	V_{GS} = ±16 V, V_{DS} = 0			±10	μA
Gate threshold voltage	V_{TH}	I_D = 1.0 mA, V_{DS} = 10.0 V	1.4		2.5	V
Drain-source ON resistance	$R_{DS(on)}$	I_D = 5.0 A, V_{GS} = 4.5 V		6.5	9.8	mΩ
		I_D = 5.0 A, V_{GS} = 10 V		3.0	4.2	
Forward transfer admittance	$\lvert Y_{fs} \rvert$	I_D = 5.0 A, V_{DS} = 10 V	10			S
Short-circuit input capacitance (Common source)	C_{iss}	V_{DS} = 10 V, V_{GS} = 0, f = 1 MHz		6000		pF
Short-circuit output capacitance (Common source)	C_{oss}			690		pF
Reverse transfer capacitance (Common source)	C_{rss}			420		pF
Avalanche energy capability	EAS	V_{DD} = 24 V, V_{GS} = 10 V to 0 V, I_D = 18 A L = 0.5 mH, R_g = 25Ω, T_{ch} = 25°C (initial)		162		mJ
Turn-on delay time *	$t_{d(on)}$	V_{DD} = 15 V, V_{GS} = 0 V to 10 V, I_D = 5.0 A		20		ns
Turn-off delay time *	$t_{d(off)}$	V_{DD} = 15 V, V_{GS} = 0 V to 10 V, I_D = 5.0 A		30		ns
Rise time *	t_r	V_{DD} = 15 V, V_{GS} = 10 V to 0 V, I_D = 5.0 A		400		ns
Fall time *	t_f	V_{DD} = 15 V, V_{GS} = 10 V to 0 V, I_D = 5.0 A		420		ns

Note) 1. Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030 measuring methods for transistors.
2. *: Measurement circuit

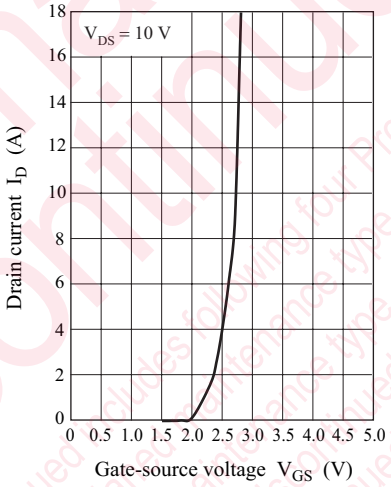
Measurement circuit



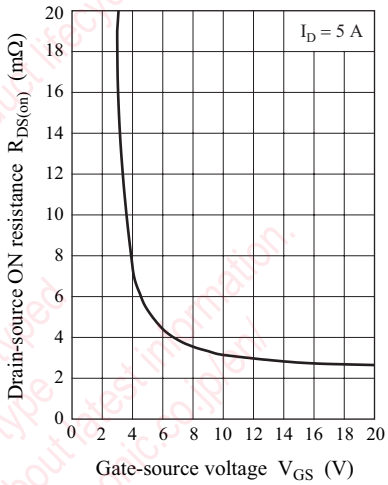
I_D — V_{DS}



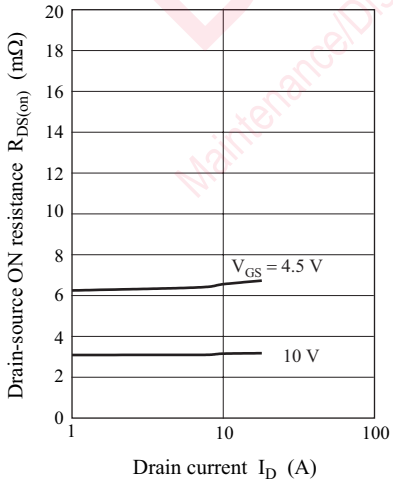
I_D — V_{GS}



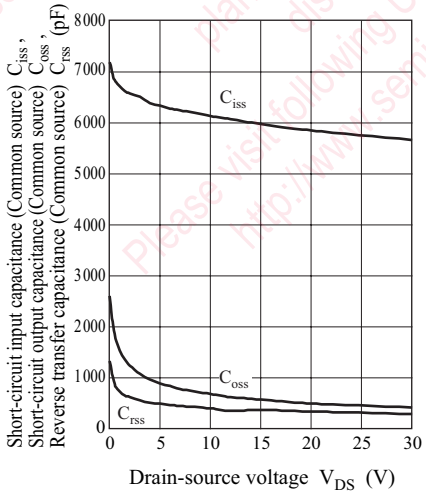
$R_{DS(on)}$ — V_{GS}



$R_{DS(on)}$ — I_D

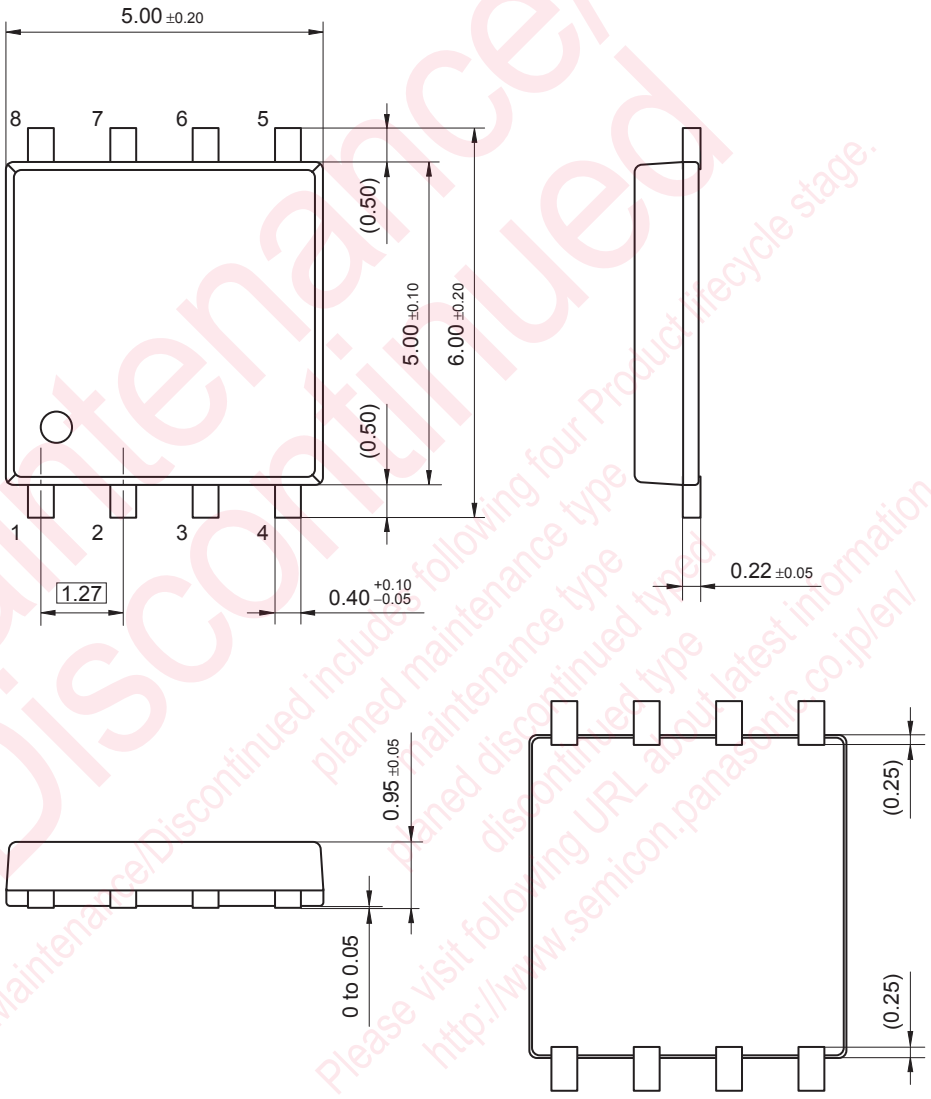


C_{iss} , C_{rss} , C_{oss} — V_{DS}



SO8-F1-B

Unit: mm



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