Notification about the transfer of the semiconductor business

The semiconductor business of Panasonic Corporation was transferred on September 1, 2020 to Nuvoton Technology Corporation (hereinafter referred to as "Nuvoton"). Accordingly, Panasonic Semiconductor Solutions Co., Ltd. became under the umbrella of the Nuvoton Group, with the new name of Nuvoton Technology Corporation Japan (hereinafter referred to as "NTCJ").

In accordance with this transfer, semiconductor products will be handled as NTCJ-made products after September 1, 2020. However, such products will be continuously sold through Panasonic Corporation.

Publisher of this Document is NTCJ.
If you would find description “Panasonic” or “Panasonic semiconductor solutions”, please replace it with NTCJ.

※ Except below description page
“Request for your special attention and precautions in using the technical information and semiconductors described in this book”

Nuvoton Technology Corporation Japan

SK840303

Silicon N-channel MOS FET

For DC-DC converter circuits

■ Overview

SK840303 is the N-channel MOS FET that is highly suitable for DC-DC converter and other switching circuits.

■ Features

- Low drain-source ON resistance:$R_{DS(on)}$ typ. = 6 mΩ (V_{GS} = 4.5 V)
- Small package with back side heat sink for improved heat dissipation.
- Eco-friendly Halogen-free package

■ Packaging

SK8403030L Embossed type (Thermo-compression sealing): 3 000 pcs / reel (standard)

■ Absolute Maximum Ratings T_a = 25°C

Parameter		Symbol	Rating	Unit
Drain-source surrender voltage		V_{DSS}	33	V
Gate-source surrender voltage		V_{GSS}	±20	V
Drain current		I_D	22	A
Peak drain current *1, 2		I_{DP}	66	A
Power dissipation	T_C = 25°C	P_D	28	W
	t = 10 s *1, 2		2	
Repetitive peak avalanche current *3		I_{AR}	22	A
Avalanche energy capability *4		EAS	50	mJ
Channel temperature		T_{ch}	150	°C
Storage temperature		T_{stg}	−55 to +150	°C

Note) *1: Mounted on a glass epoxy PC board: 25.4 mm × 25.4 mm × 0.8 mm
*2: Pulse measurement: Channel temperature not to exceed 150°C
*3: V_{DD} = 24 V, V_{GS} = 10 V → 0 V, L = 0.1 mH, Tch = 25°C (initial)
*4: V_{DD} = 24 V, V_{GS} = 10 V → 0 V, L = 0.1 mH, I_{AR} =15 A, Tch = 25°C (initial)

■ Package

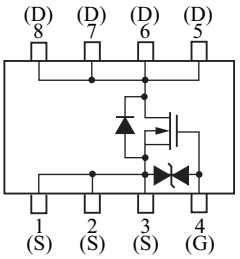
- Code
  HSSO8-F1-B
  Package dimension clicks here.→ Click!

- Pin Name

1: Source	5: Drain
2: Source	6: Drain
3: Source	7: Drain
4: Gate	8: Drain

■ Marking Symbol: 03

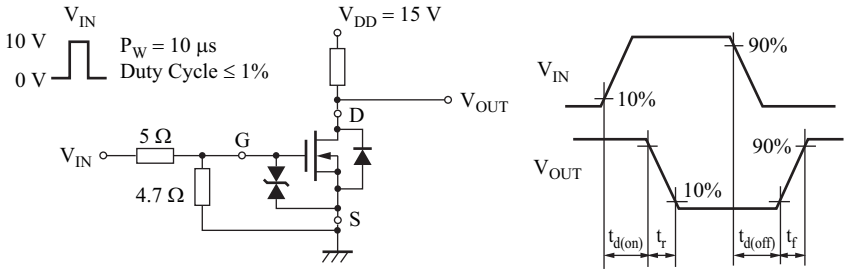
■ Internal Connection



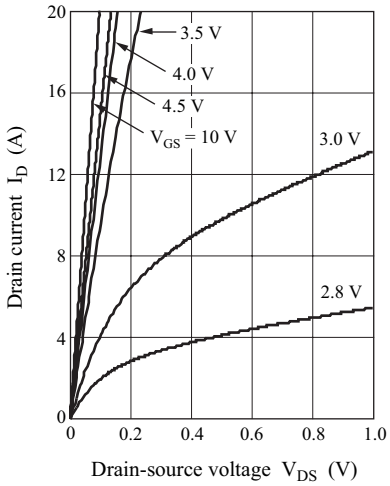
■ Electrical Characteristics $T_a = 25°C \pm 3°C$

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Static Characteristics						
Drain-source surrender voltage	V_{DSS}	$I_D = 1$ mA, $V_{GS} = 0$ V	33			V
Drain-source cutoff current	I_{DSS}	$V_{DS} = 33$ V, $V_{GS} = 0$ V			10	μA
Gate-source cutoff current	I_{GSS}	$V_{GS} = \pm 16$ V, $V_{DS} = 0$ V			±10	μA
Gate-source threshold voltage	$V_{GS(th)}$	$I_D = 2.3$ mA, $V_{DS} = 10$ V	1		2.5	V
Drain-source ON resistance	$R_{DS(on)}$	$I_D = 11$ A, $V_{GS} = 10$ V		4	6	mΩ
		$I_D = 11$ A, $V_{GS} = 4.5$ V		6	9	
	$\lvert Y_{fs} \rvert$	$I_D = 11$ A, $V_{GS} = 10$ V		90		S
Dynamic Characteristics						
Short-circuit input capacitance (Common source)	C_{iss}	$V_{DS} = 10$ V, $V_{GS} = 0$ V, f = 1 MHz	850	1450	2050	pF
Short-circuit output capacitance (Common source)	C_{oss}		190	320	450	pF
Reverse transfer capacitance (Common source)	C_{rss}		40	110	180	pF
Signal source resistance	R_g	f = 8 MHz		2.8	5	Ω
Turn-on delay time *	$t_{d(on)}$	$V_{DD} = 15$ V, $V_{GS} = 0$ V to 10 V, $I_D = 11$ A		8		ns
Rise time *	t_r			7		ns
Turn-off delay time *	$t_{d(off)}$	$V_{DD} = 15$ V, $V_{GS} = 10$ V to 0 V, $I_D = 11$ A		40		ns
Fall time *	t_f			6		ns
Gate charge load	Q_g	$V_{DD} = 15$ V, $V_{GS} = 0$ V to 4.5 V, $I_D = 22$ A		10		nC
Gate-source charge	Q_{gs}			5		nC
Gate-drain charge	Q_{gd}			3		nC
Body diode characteristics						
Drain-source voltage	V_{SD}	$I_S = 11$ A, $V_{GS} = 0$ V		0.8	1.2	V

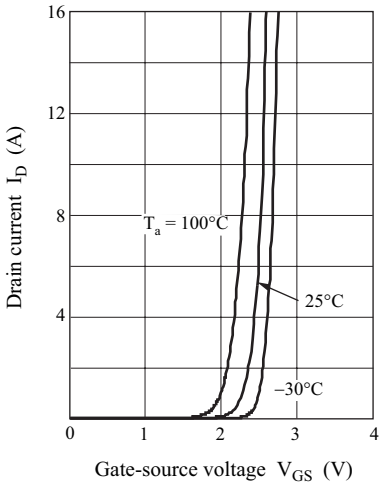
Note) 1. Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030 measuring methods for transistors.
2. *: Measurement circuit



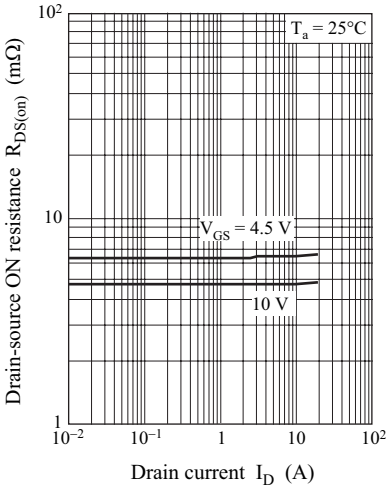
I_D — V_{DS}



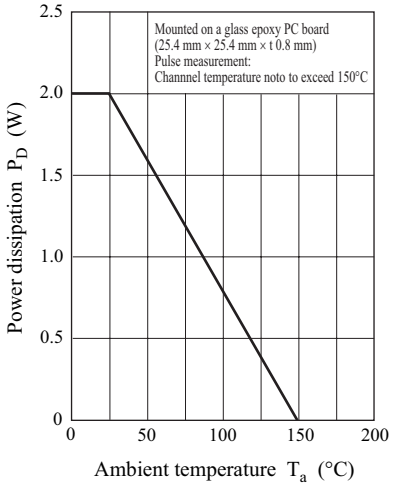
I_D — V_{GS}



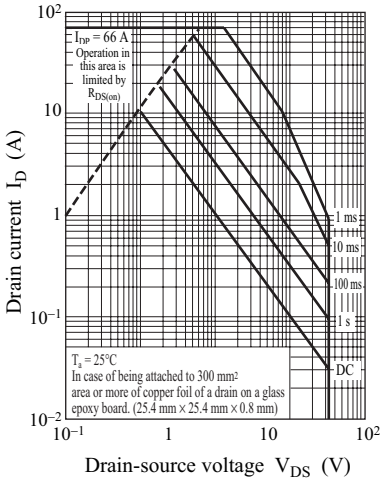
$R_{DS(on)}$ — I_D



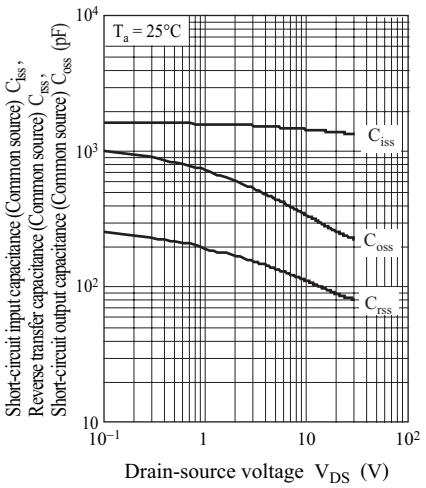
P_D — T_a



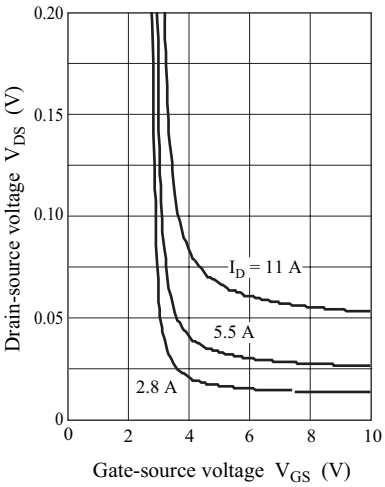
Safe operation area



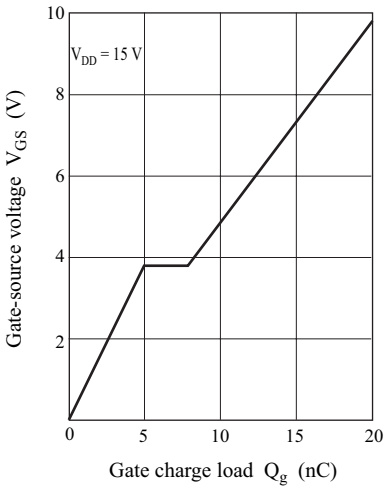
C_{iss} , C_{rss} , C_{oss} — V_{DS}



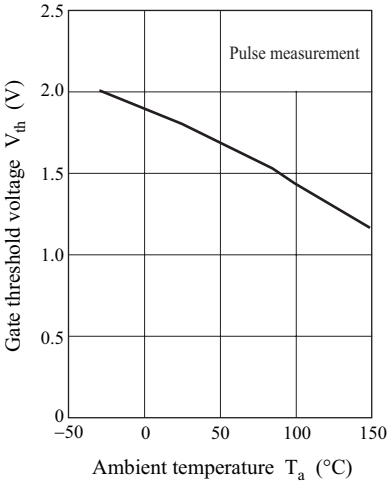
V_{DS} — V_{GS}



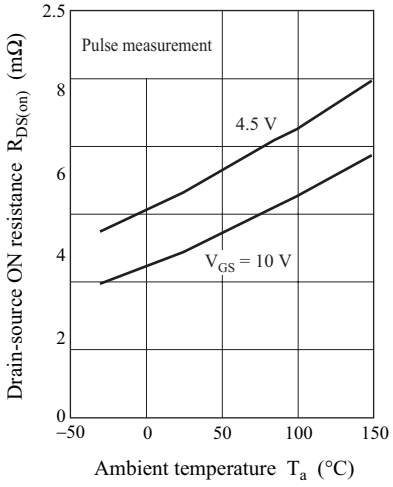
V_{GS} — Q_g



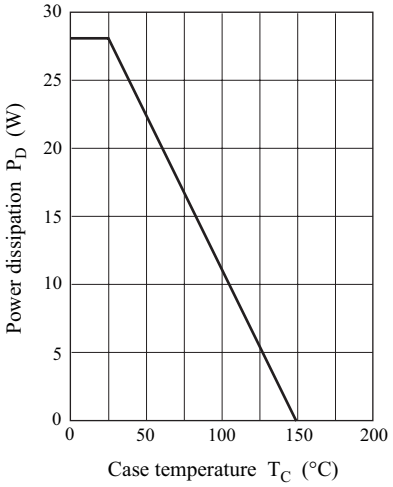
V_{th} — T_a



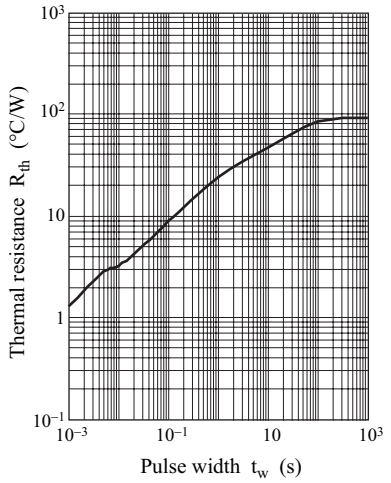
$R_{DS(on)}$ — T_a



P_D — T_C



R_{th} — t_w



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