# **UNR31A4**

# Silicon PNP epitaxial planar type

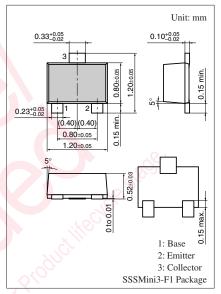
For digital circuits

#### Features

- Suitable for high-density mounting and downsizing of the equipment
- Contribute to low power consumption

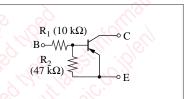
### Absolute Maximum Ratings $T_a = 25^{\circ}C$

Parameter	Symbol	Rating	Unit	
Collector-base voltage (Emitter open)	V <sub>CBO</sub>	-50	V	
Collector-emitter voltage (Base open)	V <sub>CEO</sub>	-50	V	
Collector current	I <sub>C</sub>	-80	mA	
Total power dissipation	P <sub>T</sub>	100	mW	
Junction temperature	Tj	125	°C	
Storage temperature	T <sub>stg</sub>	-55 to +125	°C	



Marking Symbol: CK

#### Internal Connection



#### Electrical Characteristics $T_a = 25^{\circ}C \pm 3^{\circ}C$

Parameter	Symbol	Conditions	Min	Тур	Max	Unit
Collector-base voltage (Emitter open)	V <sub>CBO</sub>	$I_{\rm C} = -10 \ \mu A, I_{\rm E} = 0$	-50			V
Collector-emitter voltage (Base open)	V <sub>CEO</sub>	$I_{\rm C} = -2 \text{ mA}, I_{\rm B} = 0$	-50			V
Collector-base cutoff current (Emitter open)	I <sub>CBO</sub>	$V_{CB} = -50 \text{ V}, I_E = 0$			- 0.1	μΑ
Collector-emitter cutoff current (Base open)	I <sub>CEO</sub>	$V_{CE} = -50 \text{ V}, I_B = 0$			- 0.5	μΑ
Emitter-base cutoff current (Collector open)	I <sub>EBO</sub>	$V_{EB} = -6 V, I_C = 0$			- 0.2	mA
Forward current transfer ratio	h <sub>FE</sub>	$V_{CE} = -10 \text{ V}, I_C = -5 \text{ mA}$	80			
Collector-emitter saturation voltage	V <sub>CE(sat)</sub>	$I_{\rm C} = -10 \text{ mA}, I_{\rm B} = -0.3 \text{ mA}$			- 0.25	V
Output voltage high level	V <sub>OH</sub>	$V_{CC} = -5 \text{ V},  \text{V}_{B} = -0.5  \text{V},  \text{R}_{L} = 1  \text{k} \Omega$	-4.9			V
Output voltage low level	V <sub>OL</sub>	$V_{CC} = -5 \text{ V}, \text{ V}_{B} = -2.5 \text{ V}, \text{ R}_{L} = 1 \text{ k}\Omega$			- 0.2	V
Input resistance	R <sub>1</sub>		-30%	10	+30%	kΩ
Resistance ratio	R <sub>1</sub> / R <sub>2</sub>		0.17	0.21	0.25	_
Transition frequency	f <sub>T</sub>	$V_{CB} = -10 \text{ V}, I_E = 1 \text{ mA}, f = 200 \text{ MHz}$		80		MHz

Note) Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030 measuring methods for transistors.

## **UNR31A4**

120

100

80

60

40

20

0 L 0

300

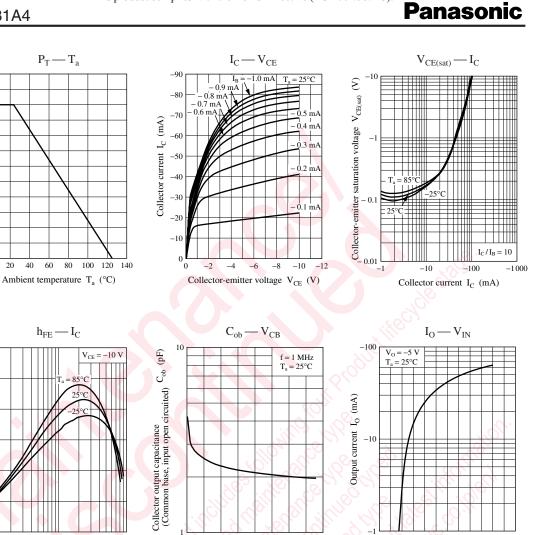
50

0

-1

20 40 60 80

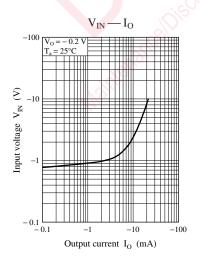
Total power dissipation  $P_{T}$  (mW)



-2 -3 -4 -5 -6

Input voltage V<sub>IN</sub> (V)

0 -1



-10

Collector current I<sub>C</sub> (mA)

-100

0

-20

Collector-base voltage V<sub>CB</sub> (V)

-30

-40

-10

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