## UNR32A3

## Silicon NPN epitaxial planar type

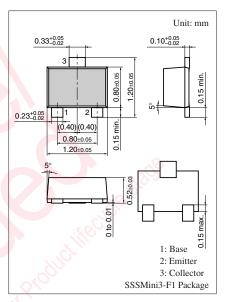
#### For digital circuits

#### ■ Features

- Suitable for high-density mounting and downsizing of the equipment
- Contribute to low power consumption

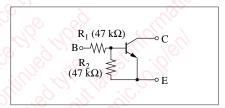
### ■ Absolute Maximum Ratings $T_a = 25$ °C

Parameter	Symbol	Rating	Unit	
Collector-base voltage (Emitter open)	V <sub>CBO</sub>	50	V	
Collector-emitter voltage (Base open)	$V_{CEO}$	50	V	
Collector current	$I_{C}$	80	mA	
Total power dissipation	$P_{T}$	100	mW	
Junction temperature	$T_{j}$	125	°C	
Storage temperature	T <sub>stg</sub>	-55 to +125	°C	



Marking Symbol: FN

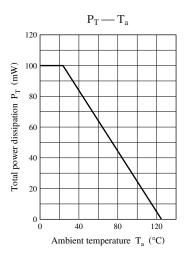
#### Internal Connection

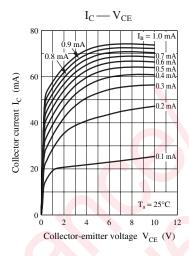


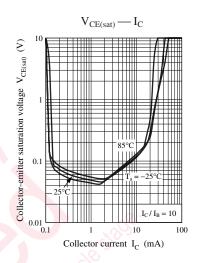
### ■ Electrical Characteristics $T_a = 25^{\circ}C \pm 3^{\circ}C$

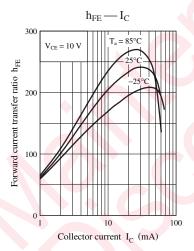
Parameter	Symbol	Conditions	Min	Тур	Max	Unit
Collector-base voltage (Emitter open)	$V_{CBO}$	$I_C = 10  \mu A, I_E = 0$	50			V
Collector-emitter voltage (Base open)	V <sub>CEO</sub>	$I_C = 2 \text{ mA}, I_B = 0$	50			V
Collector-base cutoff current (Emitter open)	$I_{CBO}$	$V_{CB} = 50 \text{ V}, I_{E} = 0$			0.1	μΑ
Collector-emitter cutoff current (Base open)	I <sub>CEO</sub>	$V_{CE} = 50 \text{ V}, I_{B} = 0$			0.5	μΑ
Emitter-base cutoff current (Collector open)	$I_{EBO}$	$V_{EB} = 6 \text{ V}, I_{C} = 0$			0.1	mA
Forward current transfer ratio	h <sub>FE</sub>	$V_{CE} = 10 \text{ V}, I_{C} = 5 \text{ mA}$	80			_
Collector-emitter saturation voltage	V <sub>CE(sat)</sub>	$I_C = 10 \text{ mA}, I_B = 0.3 \text{ mA}$			0.25	V
Output voltage high-level	V <sub>OH</sub>	$V_{CC} = 5 \text{ V}, V_{B} = 0.5 \text{ V}, R_{L} = 1 \text{ k}\Omega$	4.9			V
Output voltage low-level	V <sub>OL</sub>	$V_{CC} = 5 \text{ V}, V_{B} = 3.5 \text{ V}, R_{L} = 1 \text{ k}\Omega$			0.2	V
Input resistance	R <sub>1</sub>		-30%	47	+30%	kΩ
Resistance ratio	$R_1/R_2$		0.8	1.0	1.2	_
Transition frequency	$f_T$	$V_{CB} = 10 \text{ V}, I_{E} = -2 \text{ mA}, f = 200 \text{ MHz}$		150		MHz

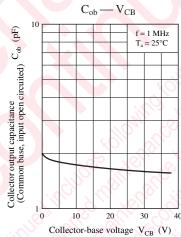
Note) Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030 measuring methods for transistors.

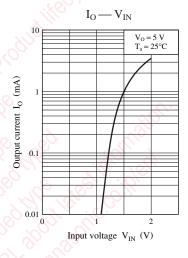


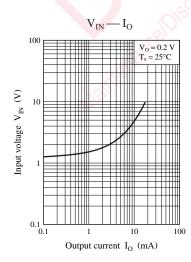












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