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# UNR92AEG

Silicon NPN epitaxial planar type

For digital circuits

#### Features

- Optimum for high-density mounting and downsizing of the equipment
- Contribute to low power consumption

#### Absolute Maximum Ratings $T_a = 25^{\circ}C$

Parameter	Symbol	Rating	Unit	
Collector-base voltage (Emitter open)	V <sub>CBO</sub>	50	V	
Collector-emitter voltage (Base open)	V <sub>CEO</sub>	50	V	
Collector current	I <sub>C</sub>	80	mA	
Total power dissipation	P <sub>T</sub>	125	mW	
Junction temperature	Tj	125	°C	
Storage temperature	T <sub>stg</sub>	-55 to +125	°C	



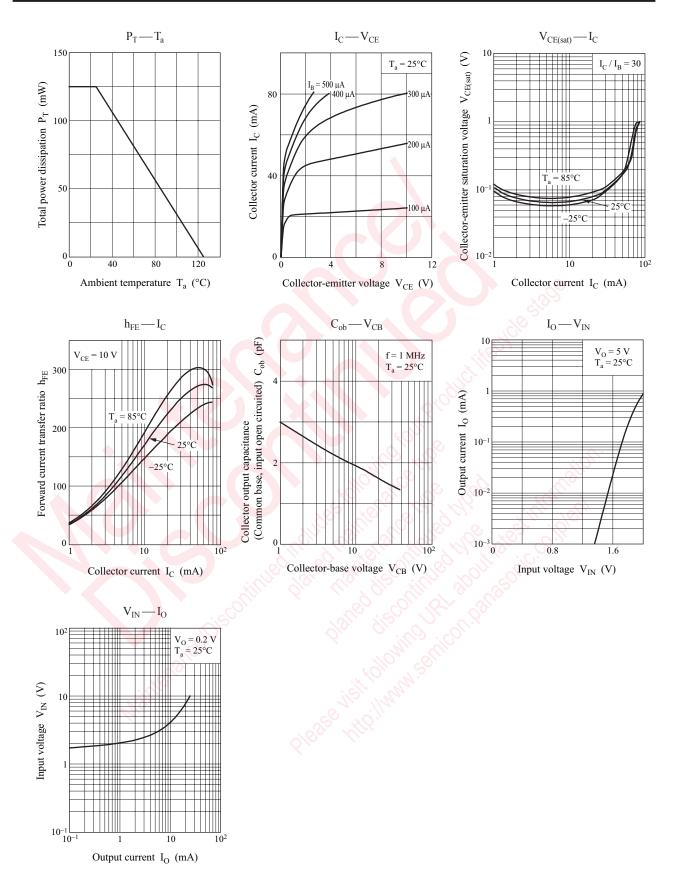
#### Electrical Characteristics $T_a = 25^{\circ}C \pm 3^{\circ}C$

Parameter	Symbol	Conditions	Min	Тур	Max	Unit
Collector-base voltage (Emitter open)	V <sub>CBO</sub>	$I_{\rm C} = 10 \ \mu \text{A}, I_{\rm E} = 0$	50			V
Collector-emitter voltage (Base open)	V <sub>CEO</sub>	$I_{\rm C} = 2 \mathrm{mA}, I_{\rm B} = 0$	50			V
Collector-base cutoff current (Emitter open)	I <sub>CBO</sub>	$V_{CB} = 50 \text{ V}, I_E = 0$			0.1	μΑ
Collector-emitter cutoff current (Base open)	I <sub>CEO</sub>	$V_{\rm CE} = 50 \text{ V}, I_{\rm B} = 0$			0.5	μΑ
Emitter-base cutoff current (Collector open)	$I_{EBO}$	$V_{\rm EB} = 6 V, I_{\rm C} = 0$			0.2	mA
Forward current transfer ratio	h <sub>FE</sub>	$V_{CE} = 10 \text{ V}, I_C = 5 \text{ mA}$	60			
Collector-emitter saturation voltage	V <sub>CE(sat)</sub>	$I_{\rm C} = 10 \text{ mA}, I_{\rm B} = 0.3 \text{ mA}$			0.25	V
Output voltage high-level	V <sub>OH</sub>	$V_{CC} = 5 V, V_B = 0.5 V, R_L = 1 k\Omega$	4.9			V
Output voltage low-level	V <sub>OL</sub>	$V_{\rm CC} = 5 \text{ V}, V_{\rm B} = 6 \text{ V}, R_{\rm L} = 1 \text{ k}\Omega$			0.2	V
Input resistance	R <sub>1</sub>		-30%	47	+30%	kΩ
Resistance ratio	$R_1 / R_2$		1.70	2.14	2.60	
Transition frequency	f <sub>T</sub>	$V_{CB} = 10 \text{ V}, I_E = -2 \text{ mA}, f = 200 \text{ MHz}$		150		MHz

Note) Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030 measuring methods for transistors.

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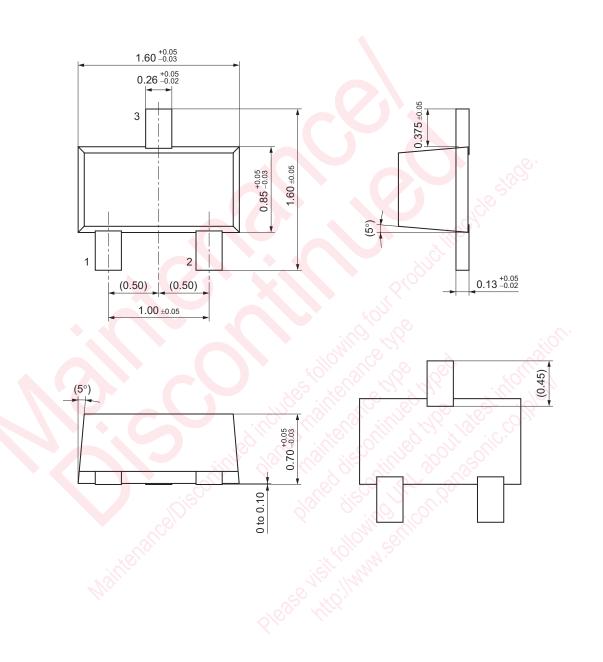
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### SSMini3-F3

Unit: mm



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