



# PJD50N10AL

## 100V N-Channel Enhancement Mode MOSFET

**Voltage**

**100 V**

**Current**

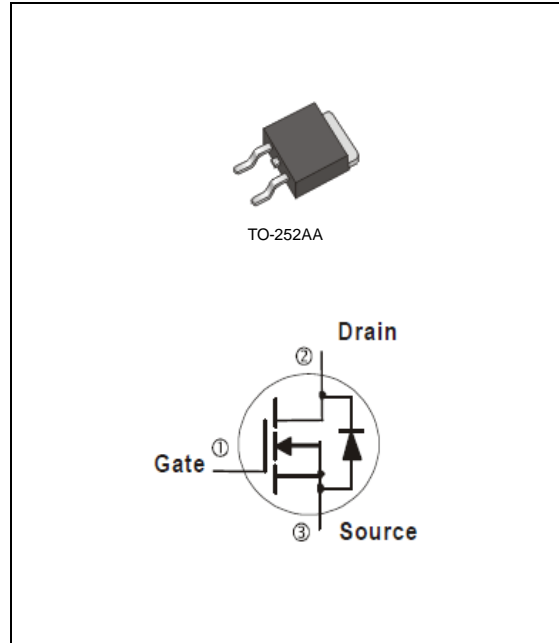
**42 A**

### Features

- $R_{DS(ON)}$ ,  $V_{GS}@10V$ ,  $I_D@20A < 25m\Omega$
- $R_{DS(ON)}$ ,  $V_{GS}@4.5V$ ,  $I_D@15A < 28.5m\Omega$
- Advanced Trench Process Technology
- High density cell design for ultra low on-resistance
- Lead free in compliance with EU RoHS 2011/65/EU directive
- Green molding compound as per IEC61249 Std.. (Halogen Free)

### Mechanical Data

- Case : TO-252AA Package
- Terminals : Solderable per MIL-STD-750, Method 2026
- Approx. Weight : 0.0104 ounces, 0.297grams



### Maximum Ratings and Thermal Characteristics ( $T_A=25^\circ C$ unless otherwise noted)

PARAMETER		SYMBOL	LIMIT	UNITS
Drain-Source Voltage		$V_{DS}$	100	V
Gate-Source Voltage		$V_{GS}$	$\pm 20$	V
Continuous Drain Current	$T_C=25^\circ C$	$I_D$	42	A
	$T_C=100^\circ C$		26	
Pulsed Drain Current (Note 1)	$T_C=25^\circ C$	$I_{DM}$	150	
Power Dissipation	$T_C=25^\circ C$	$P_D$	83	W
	$T_C=100^\circ C$		33	
Continuous Drain Current	$T_A=25^\circ C$	$I_D$	6.3	A
	$T_A=70^\circ C$		5.1	A
Power Dissipation	$T_A=25^\circ C$	$P_D$	2.0	W
Power Dissipation	$T_A=70^\circ C$		1.3	
Single Pulse Avalanche Energy (Note 6)		$E_{AS}$	63.4	mJ
Operating Junction and Storage Temperature Range		$T_J, T_{STG}$	-55~150	$^\circ C$
Typical Thermal Resistance (Note 4,5)	Junction to Case	$R_{\theta JC}$	1.5	$^\circ C/W$
	Junction to Ambient	$R_{\theta JA}$	62.5	

- Limited only By Maximum Junction Temperature



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## Electrical Characteristics (T<sub>A</sub>=25°C unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNITS
<b>Static</b>						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> =0V, I <sub>D</sub> =250uA	100	-	-	V
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250uA	1.0	1.8	2.5	V
Drain-Source On-State Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> =10V, I <sub>D</sub> =20A	-	20	25	mΩ
		V <sub>GS</sub> =4.5V, I <sub>D</sub> =15A	-	22	28.5	
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =80V, V <sub>GS</sub> =0V	-	-	1.0	uA
Gate-Source Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> =±20V, V <sub>DS</sub> =0V	-	-	±100	nA
<b>Dynamic</b> (Note 7)						
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> =50V, I <sub>D</sub> =10A, V <sub>GS</sub> =10V (Note 1,2)	-	29	-	nC
Gate-Source Charge	Q <sub>gs</sub>		-	4.5	-	
Gate-Drain Charge	Q <sub>gd</sub>		-	6.4	-	
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> =30V, V <sub>GS</sub> =0V, f=1.0MHZ	-	1485	-	pF
Output Capacitance	C <sub>oss</sub>		-	135	-	
Reverse Transfer Capacitance	C <sub>rss</sub>		-	67	-	
Turn-On Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> =50V, I <sub>D</sub> =10A, V <sub>GS</sub> =10V, R <sub>G</sub> =3Ω (Note 1,2)	-	7.8	-	ns
Turn-On Rise Time	t <sub>r</sub>		-	30	-	
Turn-Off Delay Time	t <sub>d(off)</sub>		-	35	-	
Turn-Off Fall Time	t <sub>f</sub>		-	14	-	
<b>Drain-Source Diode</b>						
Maximum Continuous Drain-Source Diode Forward Current	I <sub>S</sub>	---	-	-	42	A
Diode Forward Voltage	V <sub>SD</sub>	I <sub>S</sub> =1.0A, V <sub>GS</sub> =0V	-	0.7	1.2	V

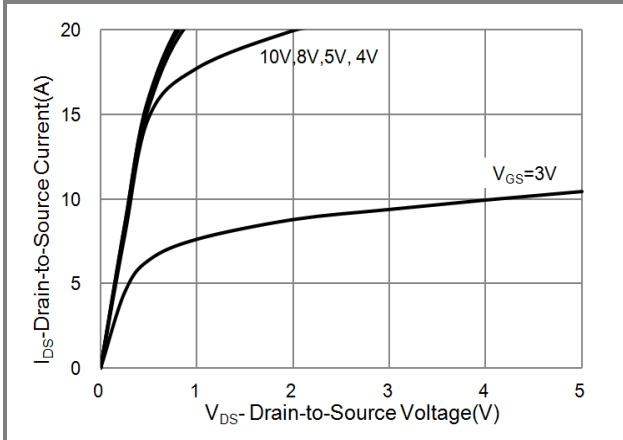
NOTES :

1. Pulse width ≤ 300us, Duty cycle ≤ 2%
2. Essentially independent of operating temperature typical characteristics.
3. Repetitive rating, pulse width limited by junction temperature T<sub>J</sub>(MAX)=150°C. Ratings are based on low frequency and duty cycles to keep initial T<sub>J</sub> = 25°C.
4. The maximum current rating is package limited.
5. R<sub>θJA</sub> is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. Mounted on a 1 inch<sup>2</sup> with 2oz.square pad of copper.
6. The test condition is L=3mH, I<sub>AS</sub>=6.5A, V<sub>DD</sub>=25V, V<sub>GS</sub>=10V
7. Guaranteed by design, not subject to production testing.

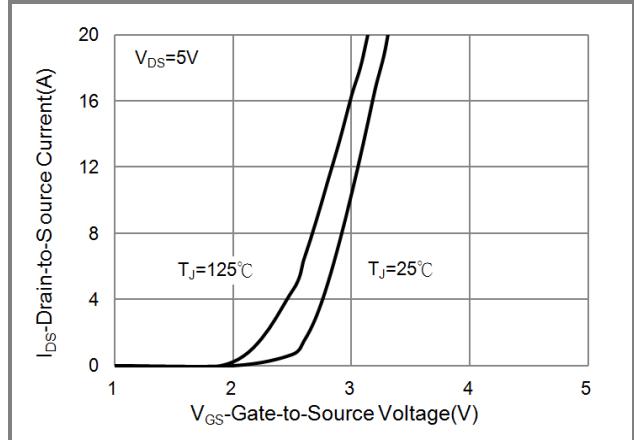


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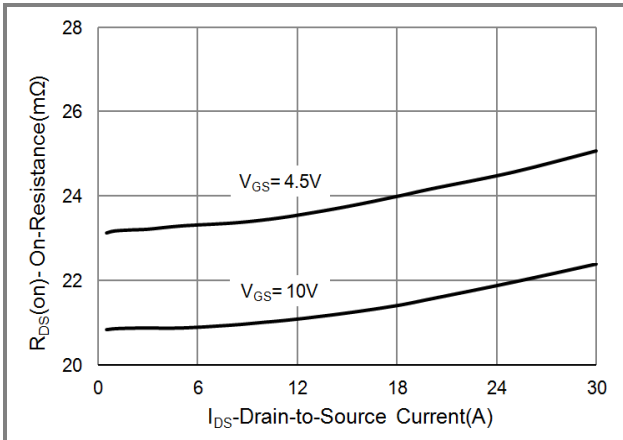
## TYPICAL CHARACTERISTIC CURVES



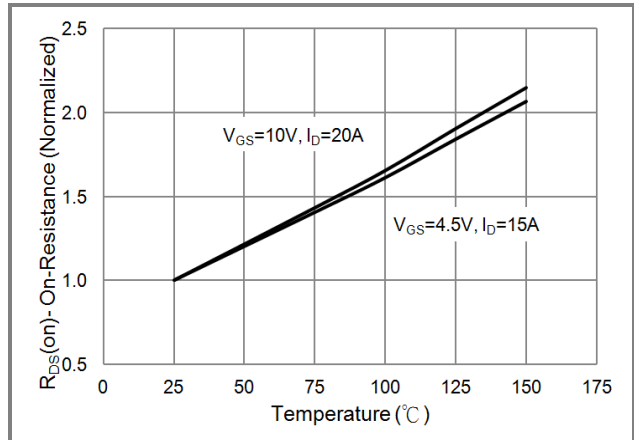
**Fig.1 Output Characteristics**



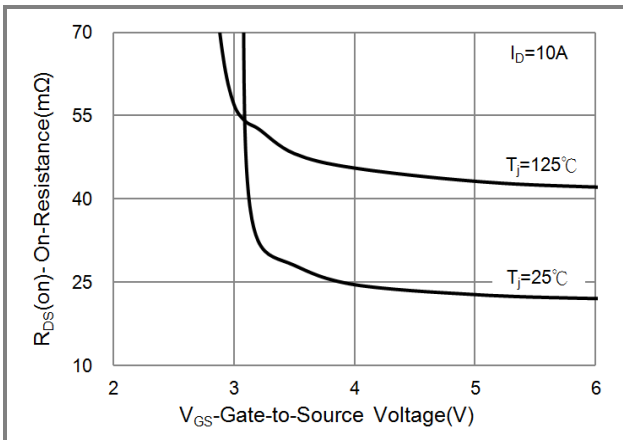
**Fig.2 Transfer Characteristics**



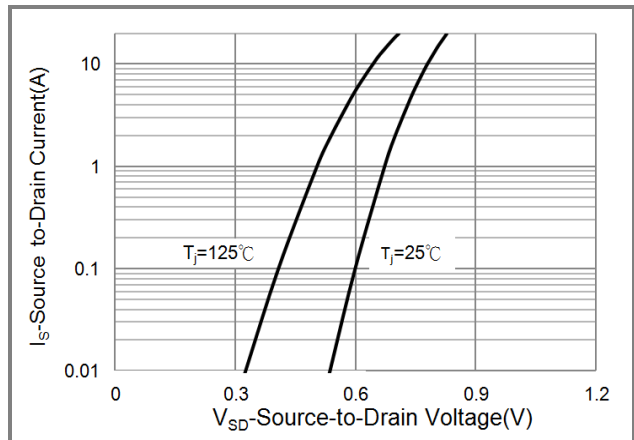
**Fig.3 On-Resistance vs. Drain Current**



**Fig.4 On-Resistance vs. Junction temperature**



**Fig.5 On-Resistance Variation with VGS.**



**Fig.6 Source-Drain Diode Forward Voltage**



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## TYPICAL CHARACTERISTIC CURVES

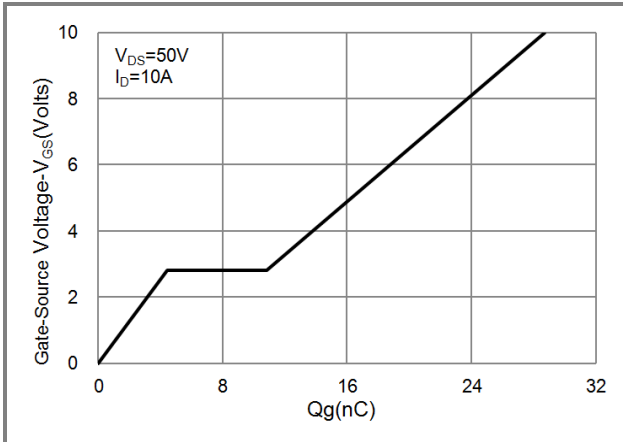


Fig.7 Gate-Charge Characteristics

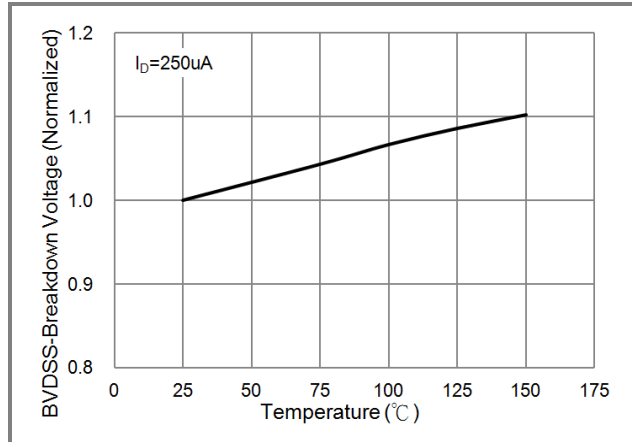


Fig.8 Breakdown Voltage Variation vs. Temperature

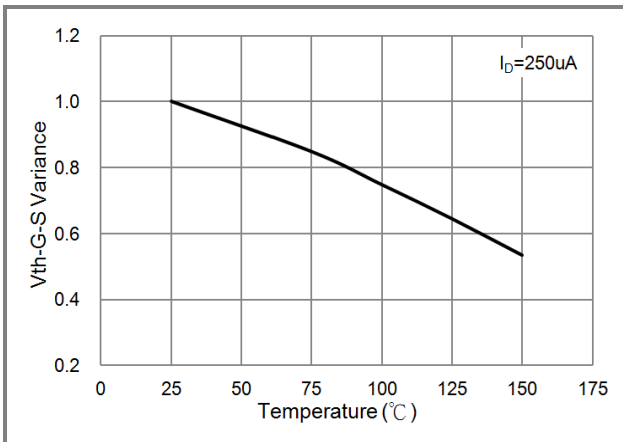


Fig.9 Threshold Voltage Variation with Temperature

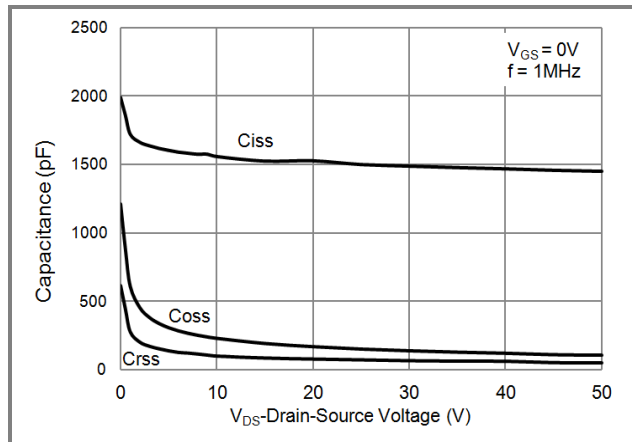


Fig.10 Capacitance vs. Drain-Source Voltage

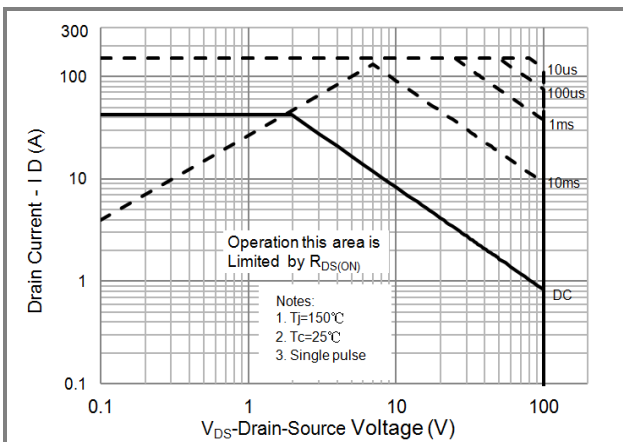


Fig.11 Maximum Safe Operating Area



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## TYPICAL CHARACTERISTIC CURVES

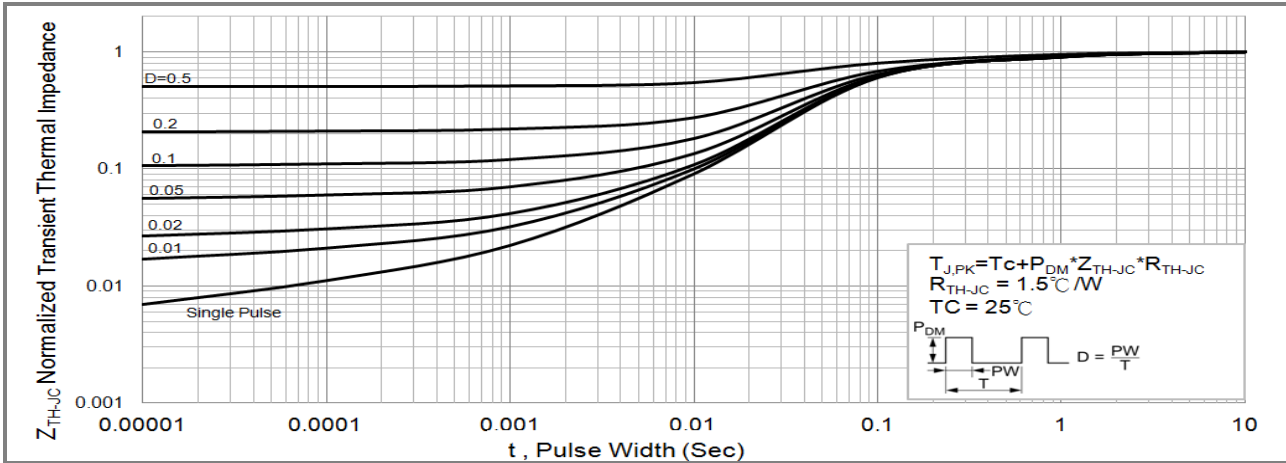
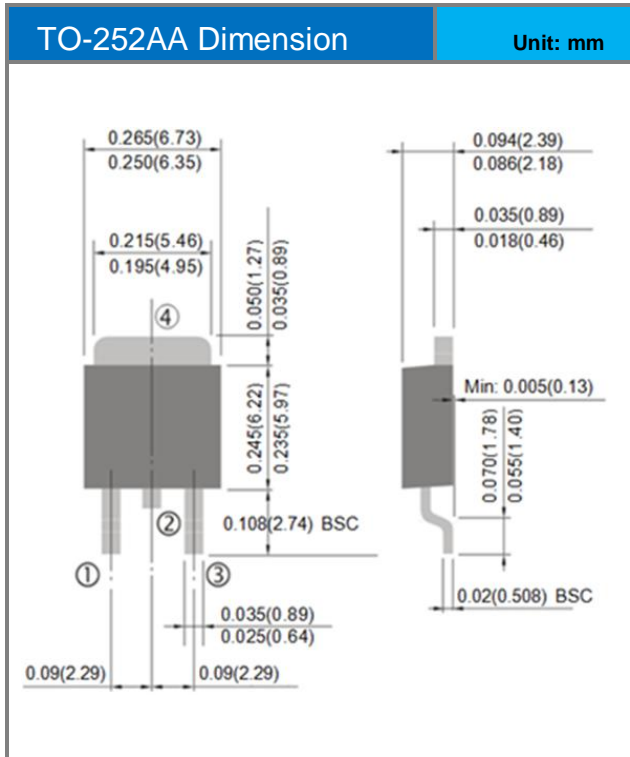


Fig.12 Normalized Transient Thermal Impedance vs. Pulse Width



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## Packaging Information



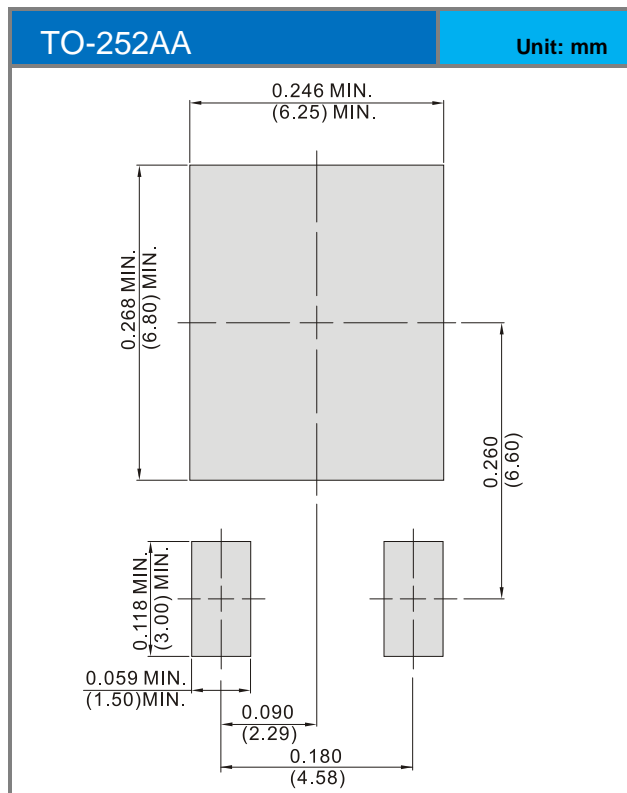


# PJD50N10AL

## PART NO PACKING CODE VERSION

Part No Packing Code	Package Type	Packing Type	Marking	Version
PJD50N10AL_L2_00001	TO-252AA	3,000pcs / 13" reel	50N10AL	Halogen free

## MOUNTING PAD LAYOUT





## PJD50N10AL

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