



PJQ1912

60V N-Channel Enhancement Mode MOSFET – ESD Protected

Voltage 60 V **Current** 410 mA

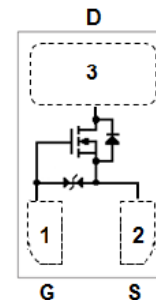
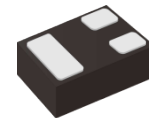
Features

- $R_{DS(ON)}$, $V_{GS}@10V$, $I_D@200mA < 3\Omega$
- $R_{DS(ON)}$, $V_{GS}@4.5V$, $I_D@100mA < 4\Omega$
- Advanced Trench Process Technology
- ESD Protected 2KV HBM
- Specially Designed for Switch Load
- Lead free in compliance with EU RoHS 2.0
- Green molding compound as per IEC 61249 standard

Mechanical Data

- Case : DFN1006-3L Package
- Terminals : Solderable per MIL-STD-750, Method 2026
- Approx. Weight : 0.00002 ounces, 0.0007 grams

DFN1006-3L



Maximum Ratings and Thermal Characteristics ($T_A=25^\circ\text{C}$ unless otherwise noted)

PARAMETER		SYMBOL	LIMIT	UNITS
Drain-Source Voltage		V_{DS}	60	V
Gate-Source Voltage		V_{GS}	± 20	
Continuous Drain Current ^(Note 4)	$T_A=25^\circ\text{C}$	I_D	410	mA
	$T_A=70^\circ\text{C}$		330	
Pulsed Drain Current ^(Note 1)	$T_A=25^\circ\text{C}$	I_{DM}	800	
Power Dissipation	$T_A=25^\circ\text{C}$	P_D	900	mW
	$T_A=70^\circ\text{C}$		580	
Operating Junction and Storage Temperature Range		T_J, T_{STG}	-55~150	$^\circ\text{C}$
Typical Thermal Resistance ^(Note 5)	Junction to Ambient	$R_{\theta JA}$	139	$^\circ\text{C/W}$



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Electrical Characteristics (T_A=25°C unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNITS
Static						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V, I _D =250uA	60	-	-	V
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =250uA	1.0	1.6	2.5	
Drain-Source On-State Resistance	R _{DS(on)}	V _{GS} =10V, I _D =200mA	-	2.1	3	Ω
		V _{GS} =4.5V, I _D =100mA	-	2.2	4	
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =60V, V _{GS} =0V	-	-	1	uA
Gate-Source Leakage Current	I _{GSS}	V _{GS} =±20V, V _{DS} =0V	-	-	±10	uA
Dynamic (Note 6)						
Total Gate Charge	Q _g	V _{DS} =30V, I _D =500mA, V _{GS} =10V(Note 2,3)	-	1.5	-	nC
Gate-Source Charge	Q _{gs}		-	0.4	-	
Gate-Drain Charge	Q _{gd}		-	0.3	-	
Input Capacitance	C _{iss}	V _{DS} =30V, V _{GS} =0V, f=1.0MHZ	-	20	-	pF
Output Capacitance	C _{oss}		-	8	-	
Reverse Transfer Capacitance	C _{rss}		-	2	-	
Turn-On Delay Time	t _{d(on)}	V _{DD} =30V, I _D =500mA, V _{GS} =10V, R _G =3.3Ω (Note 2,3)	-	2	-	ns
Turn-On Rise Time	t _r		-	20	-	
Turn-Off Delay Time	t _{d(off)}		-	5	-	
Turn-Off Fall Time	t _f		-	22	-	
Drain-Source Diode						
Diode Forward Current	I _S	---	-	-	410	mA
Diode Forward Voltage	V _{SD}	I _S =200mA, V _{GS} =0V	-	0.86	1.3	V

NOTES :

1. Pulse width ≤ 300us, Duty cycle ≤ 2%.
2. Essentially independent of operating temperature typical characteristics.
3. Repetitive rating, pulse width limited by junction temperature T_{J(MAX)}=150°C. Ratings are based on low frequency and duty cycles to keep initial T_J=25°C.
4. The maximum current rating is package limited.
5. R_{θJA} is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. Mounted on a 1 inch² with 2oz.square pad of copper.
6. Guaranteed by design, not subject to production testing.



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TYPICAL CHARACTERISTIC CURVES

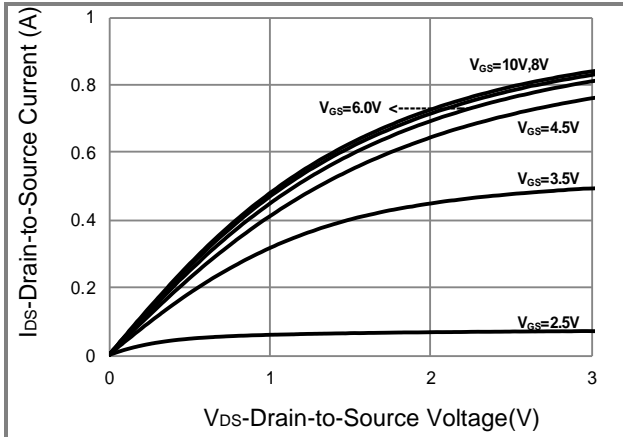


Fig.1 Output Characteristics

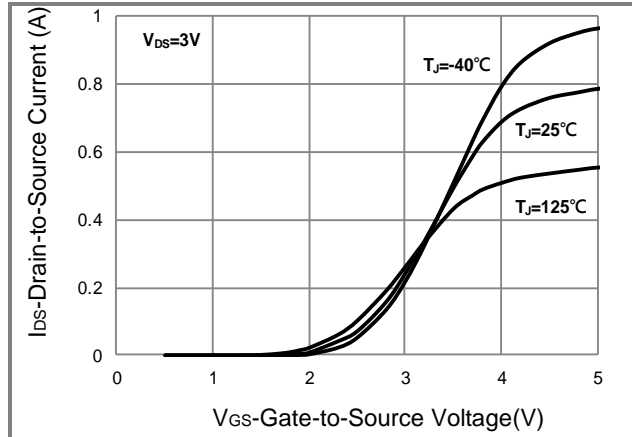


Fig.2 Transfer Characteristics

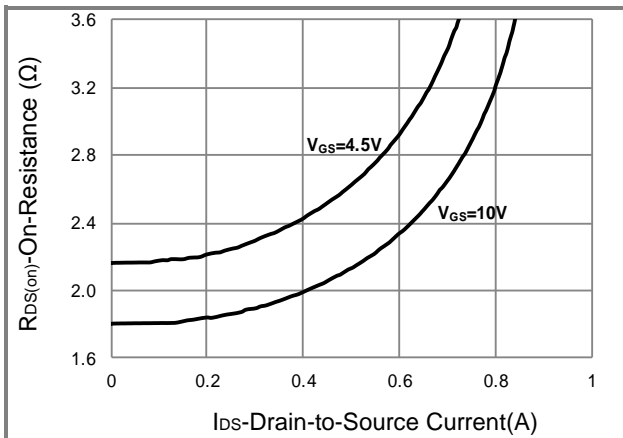


Fig.3 On-Resistance vs. Drain Current

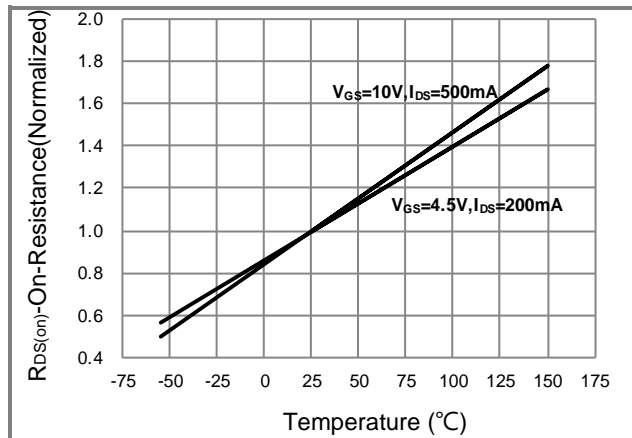


Fig.4 On-Resistance vs. Junction temperature

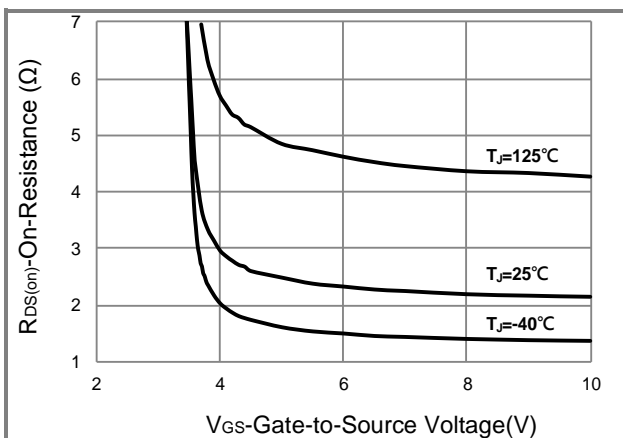


Fig.5 On-Resistance Variation with V_{GS}

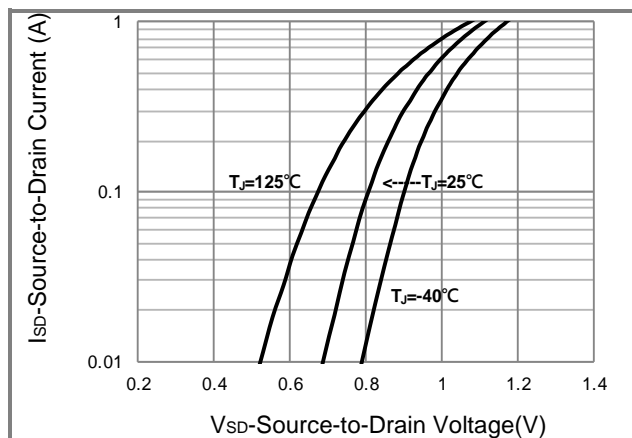


Fig.6 Source-Drain Diode Forward Voltage



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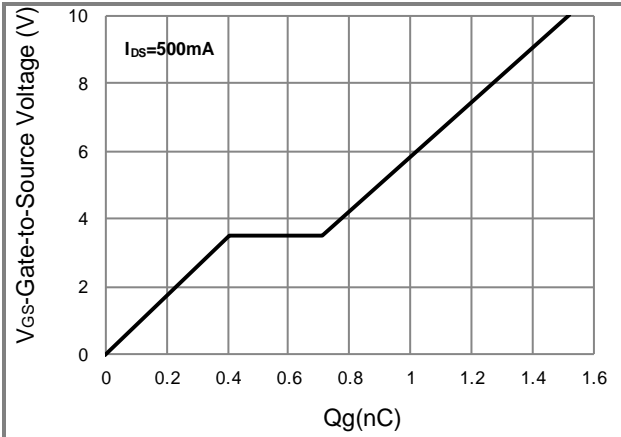


Fig.7 Gate-Charge Characteristics

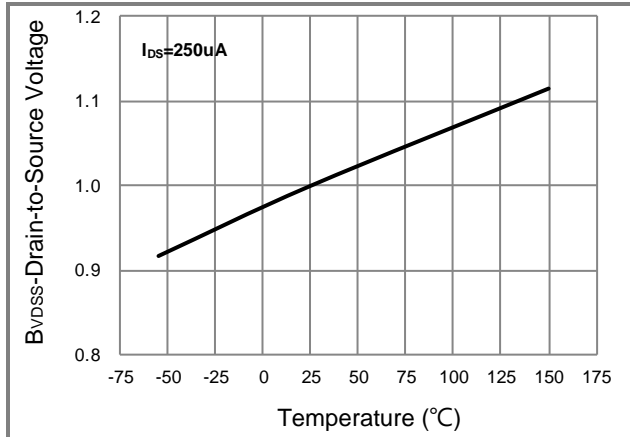


Fig.8 Breakdown Voltage Variation vs. Temperature

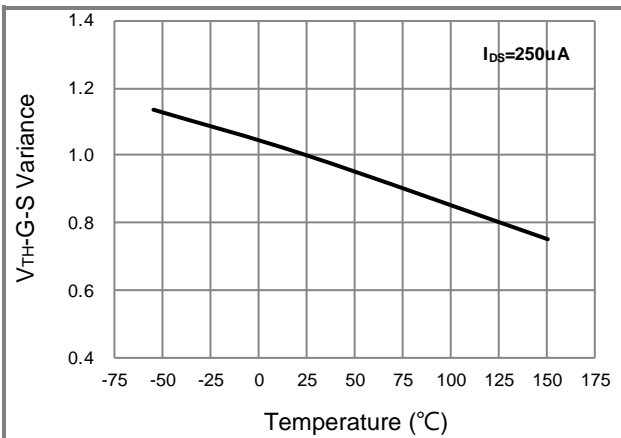


Fig.9 Threshold Voltage Variation with Temperature

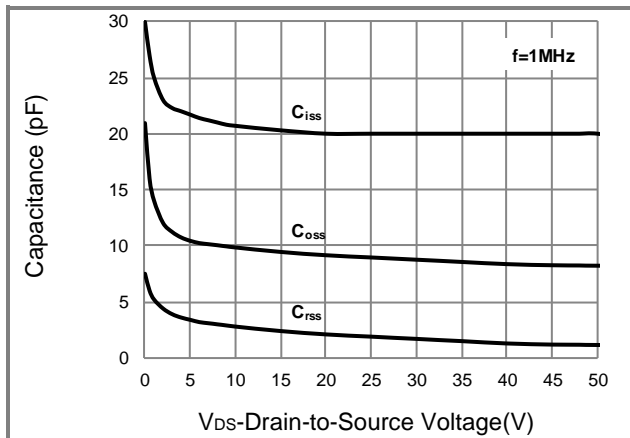


Fig.10 Capacitance vs. Drain-Source Voltage

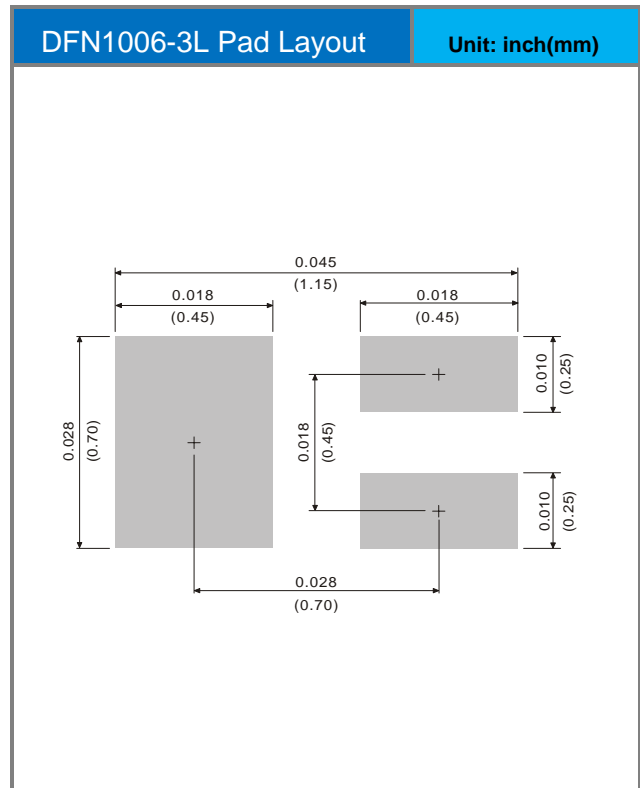
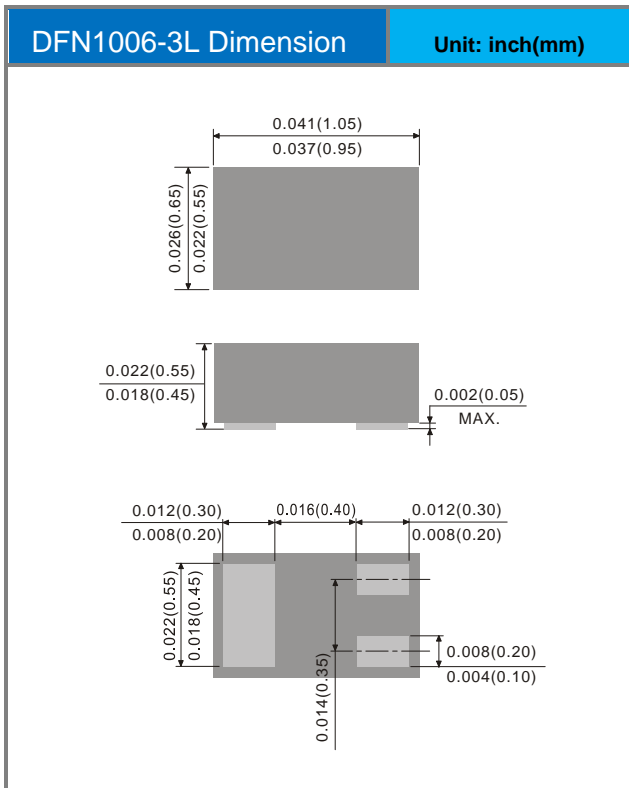


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Part No. Packing Code Version

Part No. Packing Code	Package Type	Packing Type	Marking	Version
PJQ1912_R1_00201	DFN1006-3L	10K pcs / 7" reel	C	Halogen free RoHS compliant

Packaging Information & Mounting Pad Layout





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