PAIN	JII
	SEMI
	CONDUCTOR

30V P-Channel Enhancement Mode MOSFET

Current

-5A

Features

Voltage

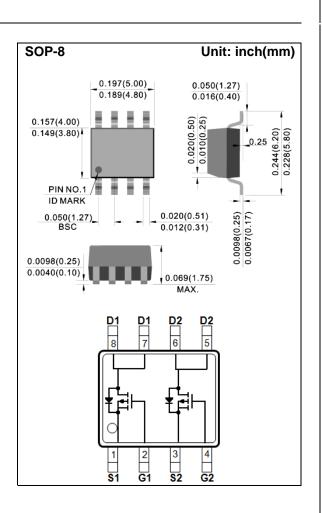
• RDS(ON) , VGS@-10V, ID@-5.0A<54mΩ

-30 V

- RDS(ON), VGS@-4.5V, ID@-3.5A<61mΩ
- RDS(ON), VGS@-2.5V, ID@-2.5A<82mΩ
- Advanced Trench Process Technology
- High density cell design for ultra low on-resistance
- Lead free in compliance with EU RoHS 2011/65/EU directive
- Green molding compound as per IEC61249 Std. (Halogen Free)

Mechanical Data

- Case: SOP-8 Package
- Terminals: Solderable per MIL-STD-750, Method 2026
- Approx. Weight: 0.0029 ounces, 0.083 grams
- Marking: L9801



Maximum Ratings and Thermal Characteristics ($T_A=25^{\circ}C$ unless otherwise noted)

PARAMETER		SYMBOL	LIMIT	UNITS
Drain-Source Voltage		V _{DS}	-30	V
Gate-Source Voltage	V _{GS}	<u>+</u> 12	V	
Continuous Drain Current		I _D	5	А
Pulsed Drain Current		I _{DM}	20	А
Power Dissipation	T _a =25°C	P _D	2	W
	Derate above 25°C		16	mW/°C
Operating Junction and Storage Temperature Range		T_J, T_{STG}	-55~150	°C
Typical Thermal resistance - Junction to Ambient ^(Note 3)		$R_{ extsf{ heta}JA}$	62.5	°C/W



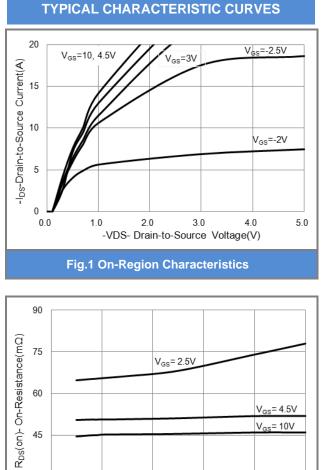
Electrical Characteristics ($T_A=25^{\circ}C$ unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNITS
Static						
Drain-Source Breakdown Voltage	BV_{DSS}	V _{GS} =0V,I _D =-250uA	-30	-	-	V
Gate Threshold Voltage	V _{GS(th)}	$V_{DS}=V_{GS}$, $I_{D}=-250$ uA	-0.5	-0.97	-1.3	V
Drain-Source On-State Resistance	R _{DS(on)}	V _{GS} =-10V,I _D =-5.0A	-	45	54	mΩ
		V _{GS} =-4.5V,I _D =-3.5A	-	51	61	
		V _{GS} =-2.5V,I _D =-2.5A	-	67	82	
Zero Gate Voltage Drain Current	I _{DSS}	V_{DS} =-30V, V_{GS} =0V	-	-0.01	-1.0	uA
Gate-Source Leakage Current	I _{GSS}	V _{GS} = <u>+</u> 12V,V _{DS} =0V	-	<u>+</u> 10	<u>+</u> 100	nA
Dynamic ^(Note 5)						
Total Gate Charge	Q_{g}		-	9.1	-	nC
Gate-Source Charge	Q_gs	V _{DS} =-15V, I _D =-5.0A, V _{GS} =4.5V ^(Note 1,2)	-	1.8	-	
Gate-Drain Charge	Q_gd		-	2.6	-	
Input Capacitance	Ciss	V _{DS} =-15V, V _{GS} =0V, f=1.0MHZ	-	816	-	pF
Output Capacitance	Coss		-	64	-	
Reverse Transfer Capacitance	Crss		-	42	-	
Turn-On Delay Time	td _(on)		-	5	-	
Turn-On Rise Time	tr	V _{DD} =-15V, I _D =-5.0A, V _{GS} =-10V,	-	45	-	
Turn-Off Delay Time	td _(off)		-	66	-	ns
Turn-Off Fall Time	tf	$R_G=6\Omega^{(Note 1,2)}$	-	10	-	
Drain-Source Diode						
Maximum Continuous Drain-Source Diode Forward Current	I _S		-	-	-2	A
Diode Forward Voltage	V _{SD}	I _S =-1.0A, V _{GS} =0V	-	0.77	-1.2	V

NOTES :

- 1. Pulse width</br>
- 2. Essentially independent of operating temperature typical characteristics.
- 3. The maximum current rating is package limited.
- 4. $R_{\Theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. Mounted on a 1 inch² with 2oz.square pad of copper
- 5. Guaranteed by design, not subject to production testing





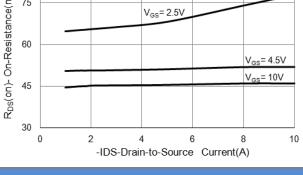
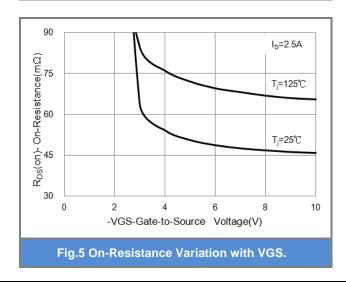


Fig.3 On-Resistance vs. Drain Current



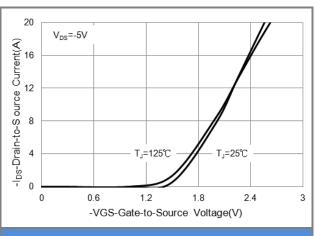


Fig.2 Transfer Characteristics

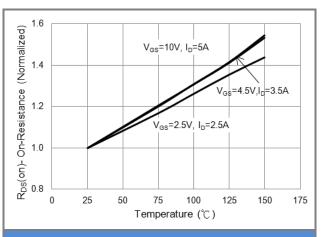
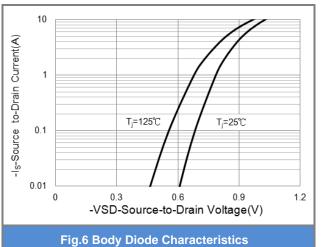


Fig.4 On-Resistance vs. Junction temperature





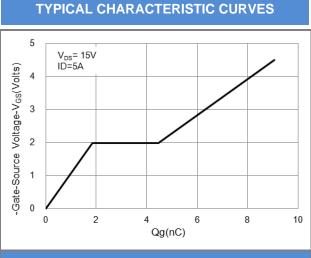


Fig.7 Gate-Charge Characteristics

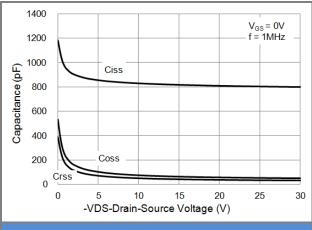


Fig.9 Capacitance vs. Drain-Source Voltage.

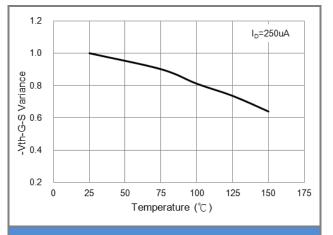


Fig.8 Threshold Voltage Variation with Temperature.

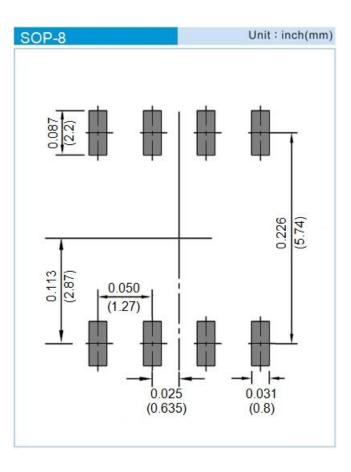




PART NO PACKING CODE VERSION

Part No Packing Code	Package Type	Packing type	Marking	Version
PJL9801_R2_00001	SOP-8	2.5K pcs / 13" reel	L9801	Halogen free

MOUNTING PAD LAYOUT





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