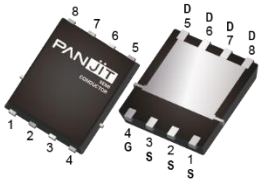
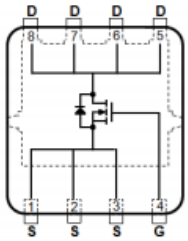
100V N-Channel Enhancement Mode MOSFET

Voltage	**100 V**	**R_{DSON}**	**4.4 mΩ**
Current	**122 A**	**$Q_{G\ (TYP)}$**	**40.5 nC**

DFN5060-8L





Top side view

Feature

- $R_{DS(ON)}$ < 4.4 mΩ at V_{GS} = 10 V, I_D = 50 A
- $R_{DS(ON)}$ < 6.5 mΩ at V_{GS} = 6 V, I_D = 25 A
- High switching speed
- Low reverse transfer capacitance
- Lead free in compliance with EU RoHS 2.0
- Green molding compound as per IEC 61249 standard

Mechanical Data

- Case: DFN5060-8L Package
- Terminals: Solderable per MIL-STD-750, Method 2026
- Approx. Weight: 0.08 grams

Application

- SR solutions of PD Charger, Brick Power, 48V DC/DC converter

Absolute Maximum Ratings (T_A = 25 °C unless otherwise specified)

PARAMETER		SYMBOL	LIMIT	UNITS
Drain-Source Voltage		V_{DS}	100	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current (Note 3)	T_C=25 °C	I_D	122	A
	T_C=100 °C		77	
Pulsed Drain Current	T_C=25 °C	I_{DM}	488	A
Single Pulse Avalanche Current (Note 5)		I_{AS}	50	A
Single Pulse Avalanche Energy (Note 5)		E_{AS}	318	mJ
Power Dissipation	T_C=25 °C	P_D	125	W
	T_C=100 °C		50	
Operating Junction and Storage Temperature Range		T_J,T_{STG}	-55~150	°C

Thermal Characteristics

PARAMETER		SYMBOL	MAXIMUM	UNITS
Thermal Resistance	Junction-to-Case (Bottom)	$R_{\theta JC}$	1.0	°C/W
	Junction-to-Ambient (Note 4)	$R_{\theta JA}$	50	°C/W

Electrical Characteristics (T_A = 25 °C unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNITS
Static						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0 V, I_D=250 μA	100	-	-	V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=270 μA	1.8	2.8	3.8	
Drain-Source On-State Resistance (Note 1)	$R_{DS(on)}$	V_{GS}=10 V, I_D=50 A	-	3.8	4.4	mΩ
		V_{GS}=6 V, I_D=25 A	-	5.0	6.5	
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=100 V, V_{GS}=0 V	-	-	1	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±20 V, V_{DS}=0 V	-	-	±100	nA
Transfer characteristics (Note 1)	g_{fs}	V_{DS}=10 V, I_D=50 A	-	105	-	S
Dynamic (Note 6)						
Total Gate Charge	Q_g	V_{DS}=50 V, I_D=50 A, V_{GS}=10 V	-	40.5	53	nC
Gate-Source Charge	Q_{gs}		-	15	-	
Gate-Drain Charge	Q_{gd}		-	6	-	
Gate Plateau Voltage	$V_{plateau}$		-	5	-	V
Input Capacitance	C_{iss}	V_{DS}=50 V, V_{GS}=0 V, f=250 kHz	-	3010	3910	pF
Output Capacitance	C_{oss}		-	1080	1400	
Reverse Transfer Capacitance	C_{rss}		-	14	-	
Output Charge	Q_{oss}	V_{DS}=50 V, V_{GS}=0 V	-	85	110	nC
Turn-On Delay Time	$t_{d(on)}$	V_{DD}=50 V, I_D=50 A, V_{GS}=10 V, R_G=6.0 Ω (Note 2)	-	11	-	ns
Rise Time	t_r		-	6	-	
Turn-Off Delay Time	$t_{d(off)}$		-	22	-	
Fall Time	t_f		-	8	-	
Gate Resistance	R_g	f =1.0 MHz	-	0.8	1.6	Ω
Drain-Source Diode						
Diode Forward Voltage	V_{SD}	I_S=50 A, V_{GS}=0 V	-	0.9	1.2	V
Reverse Recovery Charge	Q_{rr}	I_F=50 A, V_{DD}=50 V di/dt=100 A/μs	-	85	-	nC
Reverse Recovery Time	T_{rr}		-	56	-	ns

NOTES :

1. Pulse width ≤ 300 μs, Duty cycle ≤ 2 %
2. Essentially independent of operating temperature typical characteristics.
3. The maximum drain current calculated by maximum junction temperature and thermal impedance. It can be varied by application and environment.
4. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. Mounted on a 1 $inch^2$ with 2oz.square pad of copper.
5. E_{AS} is calculated based on the condition of L = 1.0 mH, I_{AS} = 25.2 A, V_{DD} = 50 V, V_{GS} = 10 V. 100% test at L = 0.1 mH, I_{AS} = 50 A in production.
6. Guaranteed by design, not subject to production testing.

TYPICAL CHARACTERISTIC CURVES

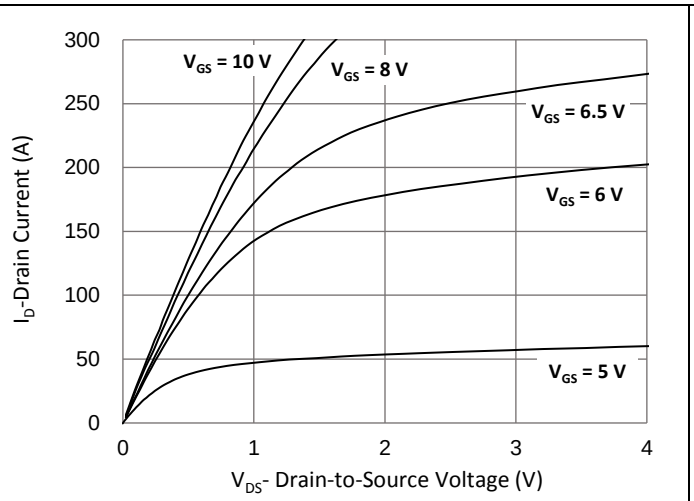


Fig.1 Output Characteristics

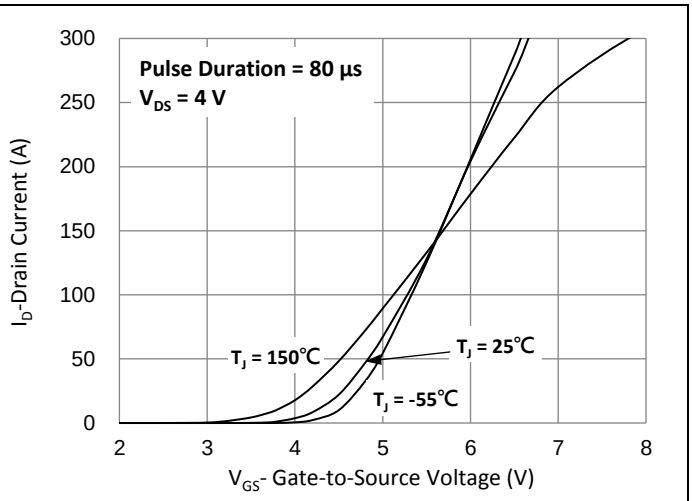


Fig.2 Transfer Characteristics

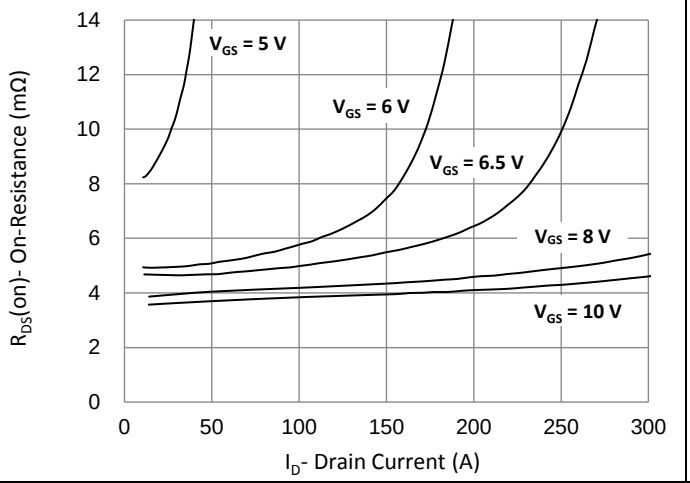


Fig.3 On-Resistance vs. Drain Current

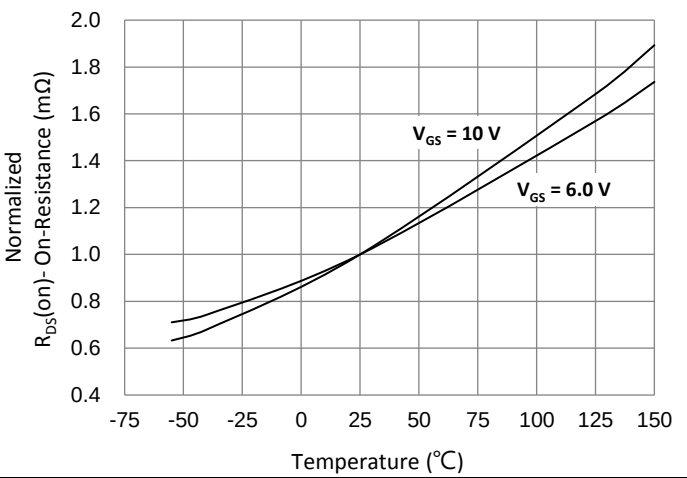


Fig.4 On-Resistance vs. Junction temperature

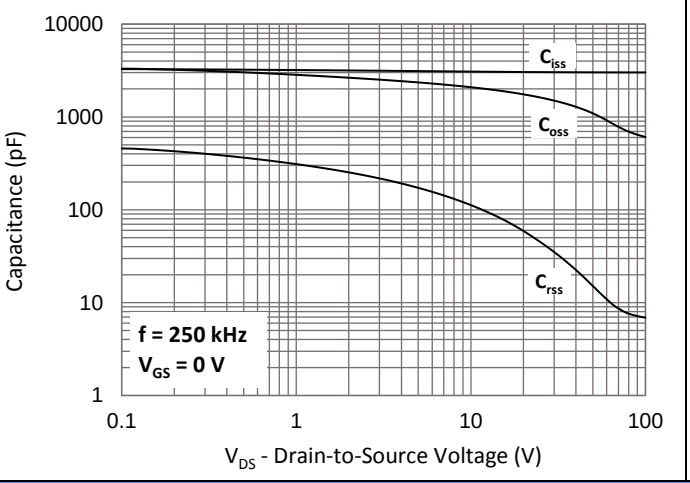


Fig.5 Capacitance vs. Drain-Source Voltage

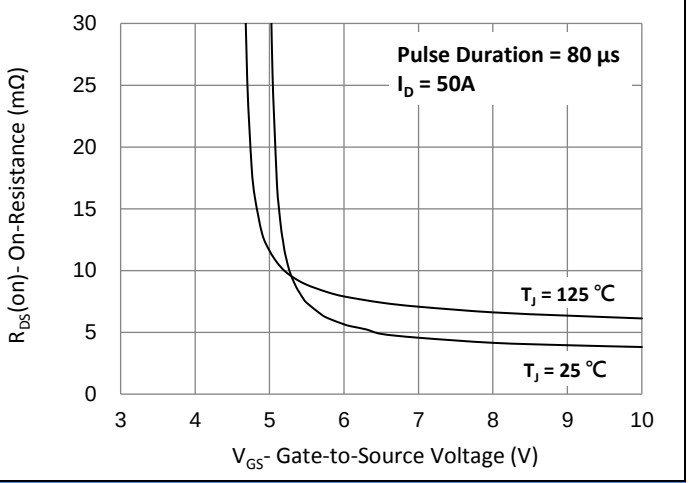


Fig.6 On-Resistance vs. Gate-Source Voltage

TYPICAL CHARACTERISTIC CURVES

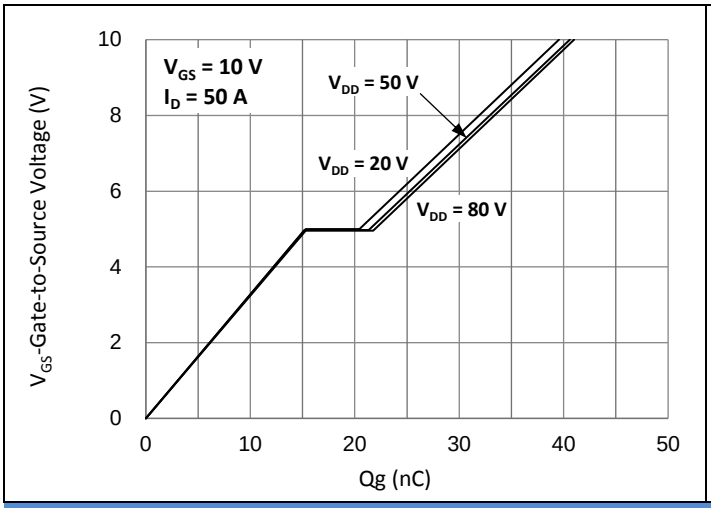


Fig.7 Gate-Charge Characteristics

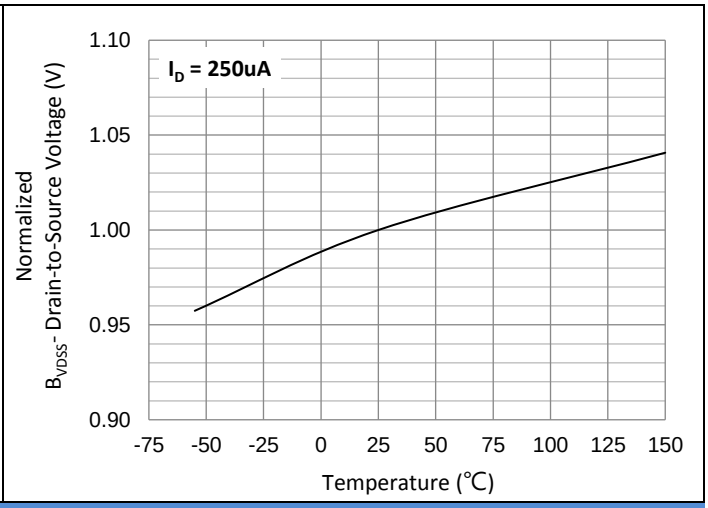


Fig.8 Breakdown Voltage Variation vs. Temperature

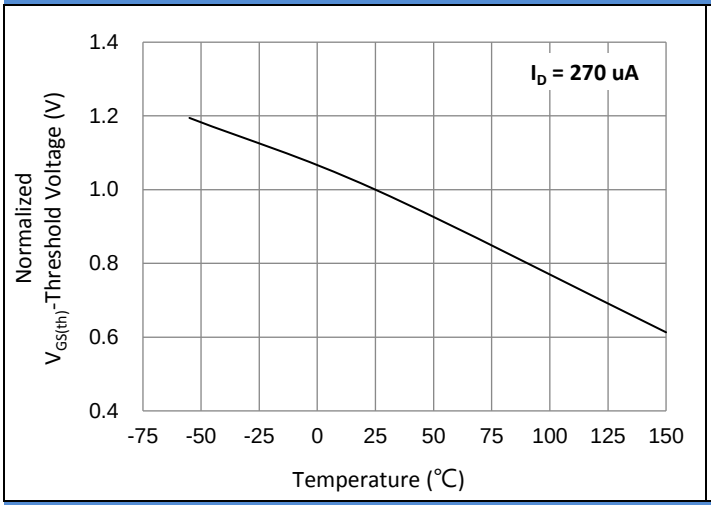


Fig.9 Threshold Voltage Variation with Temperature

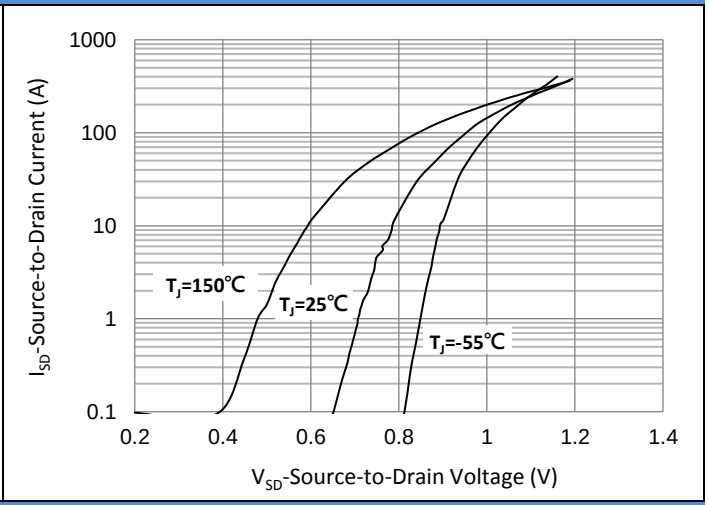


Fig.10 Source-Drain Diode Forward Voltage

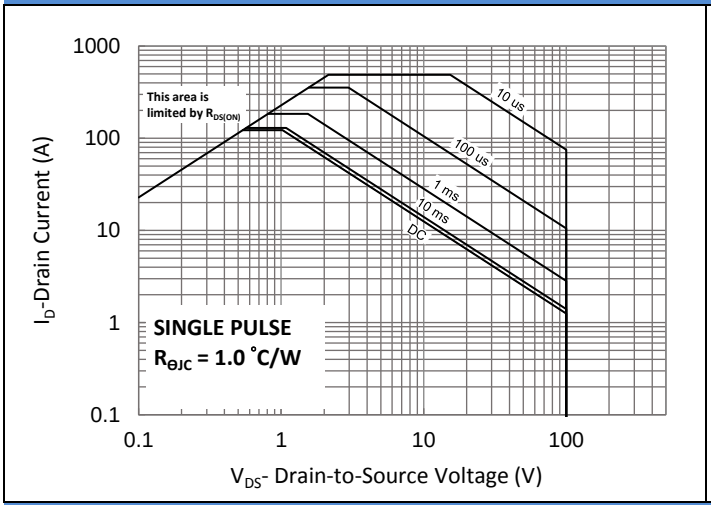


Fig.11 Maximum Safe Operating Area

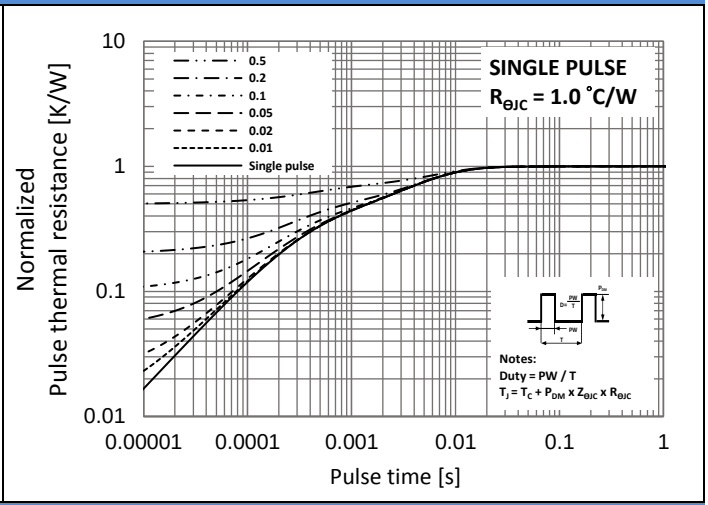


Fig.12 Normalized Transient Thermal Impedance

TYPICAL CHARACTERISTIC CURVES

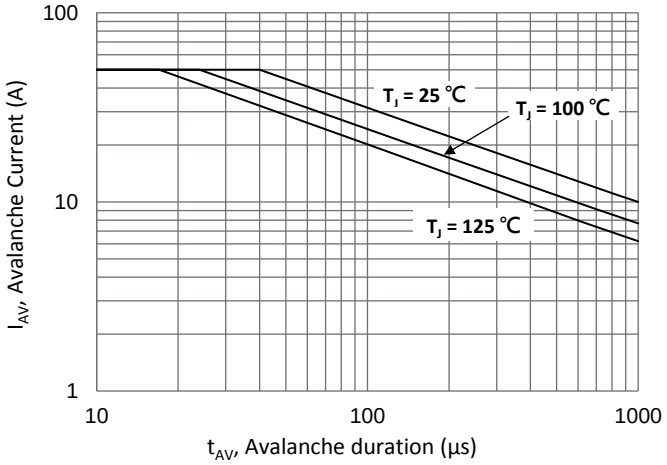


Fig.13 Avalanche Characteristics

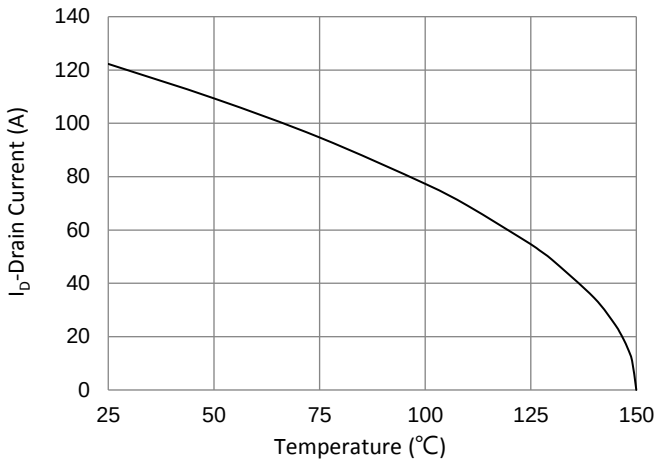


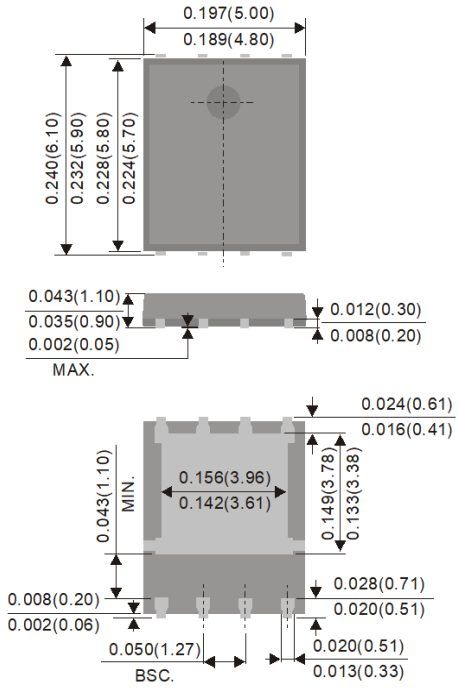
Fig.14 Drain Current vs. Case Temperature

Product and Packing Information

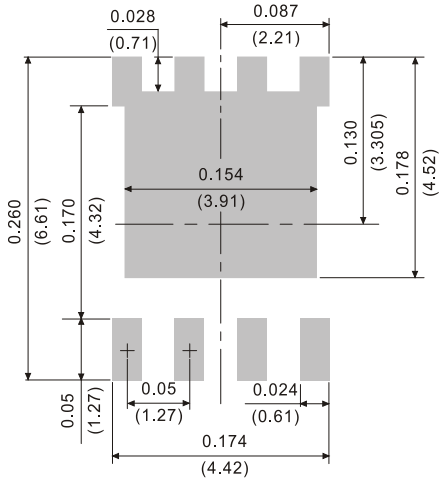
Part No.	Package Type	Packing Type	Marking
PSMQC040N10NS2	DFN5060-8L	3000pcs / 13” reel	040N10NS

Packaging Information & Mounting Pad Layout

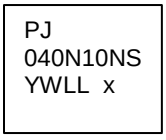
DFN5060-8L Dimension — Unit: inch(mm)



DFN5060-8L Pad Layout — Unit: inch(mm)



Marking Diagram



Y = Year Code
W = Week Code (A~Z)
LL = Lot Code (00~99)
x = Production Line Code

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