ΡΛΝ	JIT
	SEMI
	CONDUCTOR

40V N-Channel Enhancement Mode MOSFET

Voltage

Current 50 A

Features

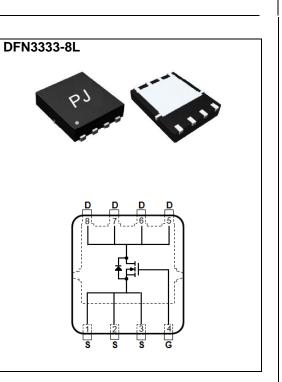
- $R_{DS(ON)}$, $V_{GS}@10V$, $I_D@20A < 7.5m\Omega$
- R_{DS(ON)}, V_{GS}@4.5V, I_D@10A<10.5mΩ

40 V

- Advanced Trench Process Technology
- High density cell design for ultralow on-resistance
- Lead free in compliance with EU RoHS 2.0
- Green molding compound as per IEC 61249 standard

Mechanical Data

- Case : DFN3333-8L Package
- Terminals : Solderable per MIL-STD-750, Method 2026
- Approx. Weight : 0.001 ounces, 0.03 grams



Maximum Ratings and Thermal Characteristics (T_A=25°C unless otherwise noted)

PARAMETE	R	SYMBOL	LIMIT	UNITS	
Drain-Source Voltage		V _{DS}	40	- V	
Gate-Source Voltage		V _{GS}	<u>+</u> 20	V	
Continuous Drain Current	T _C =25°C	I _D	50		
	Tc=100°C		32	А	
Pulsed Drain Current ^(Note 1)	T _C =25°C	I _{DM}	200		
Power Dissipation	Tc=25°C	5	45		
	T _C =100°C	Po	18	W	
Continuous Drain Current	T _A =25°C	ΙD	12.7		
	T _A =70°C		10	A	
Power Dissipation	T _A =25°C	5	2		
Power Dissipation	T _A =70°C	Po	1.3	W	
Operating Junction and Storage T	emperature Range	T _J ,T _{STG}	-55~150	°C	
Typical Thermal Resistance ^(Note 4,5)	Junction to Case	$R_{\theta JC}$	2.8		
	Junction to Ambient	R _{θJA}	62.5	°C/W	

Limited only By Maximum Junction Temperature



Electrical Characteristics (T_A=25°C unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNITS
Static						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V, I _D =250uA	40	-	-	
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =250uA	1	1.61	2.5	V
Drain-Source On-State Resistance	_	V _{GS} =10V, I _D =20A	-	6.3	7.5	mΩ
	RDS(on)	V _{GS} =4.5V, I _D =10A	-	8	10.5	
Zero Gate Voltage Drain Current	IDSS	V _{DS} =40V, V _{GS} =0V	-	-	1	uA
Gate-Source Leakage Current	lgss	V _{GS} = <u>+</u> 20V, V _{DS} =0V	-	-	<u>+</u> 100	nA
Dynamic ^(Note 6)						
Total Gate Charge	Qg	V _{DS} =20V, I _D =10A, V _{GS} =4.5V ^(Note 1,2)	-	17	-	
Gate-Source Charge	Q _{gs}		-	4.9	-	nC
Gate-Drain Charge	Q_{gd}		-	6.4	-	
Input Capacitance	Ciss	V _{DS} =25V, V _{GS} =0V, f=1MHZ	-	1759	-	
Output Capacitance	Coss		-	176	-	pF
Reverse Transfer Capacitance	Crss		-	126	-	
Turn-On Delay Time	td _(on)	V _{DD} =15V, I _D =1A, V _{GS} =10V, R _G =6Ω _(Note 1,2)	-	11	-	
Turn-On Rise Time	tr		-	21	-	
Turn-Off Delay Time	td _(off)		-	40	-	ns
Turn-Off Fall Time	t _f		-	25	-	
Drain-Source Diode	•		•	•	•	•
Maximum Continuous Drain-Source	ls		-	-	50	А
Diode Forward Current	10					
Diode Forward Voltage	V_{SD}	Is=1A, V _G s=0V	-	0.7	1	V

NOTES :

- 1. Pulse width</br>
- 2. Essentially independent of operating temperature typical characteristics.
- Repetitive rating, pulse width limited by junction temperature T_{J(MAX)}=150°C. Ratings are based on low frequency and duty cycles to keep initial T_J =25°C.
- 4. The maximum current rating is package limited.
- 5. $R_{\Theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. Mounted on a 1 inch² with 2oz.square pad of copper.
- 6. Guaranteed by design, not subject to production testing.



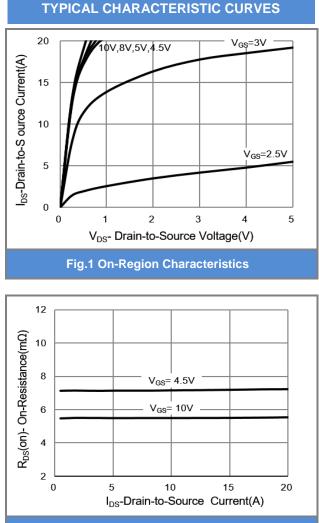
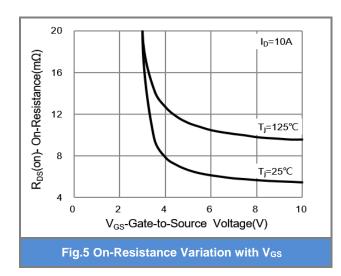


Fig.3 On-Resistance vs. Drain Current



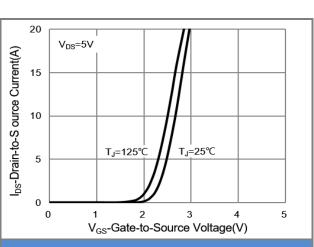


Fig.2 Transfer Characteristics

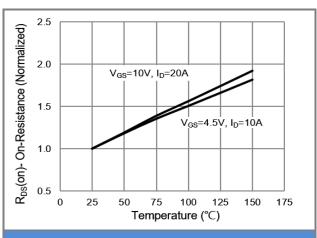
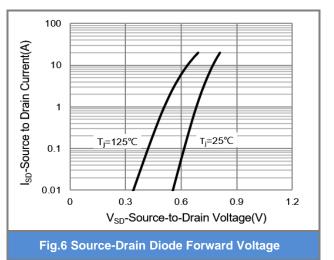


Fig.4 On-Resistance vs. Junction temperature



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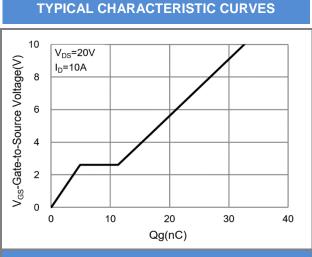


Fig.7 Gate-Charge Characteristics

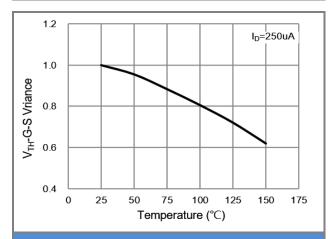
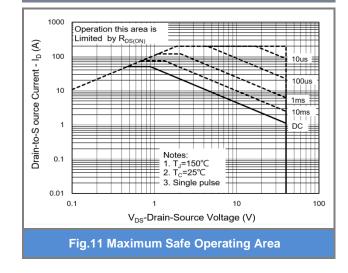
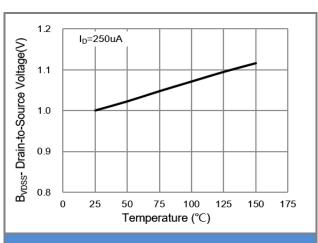
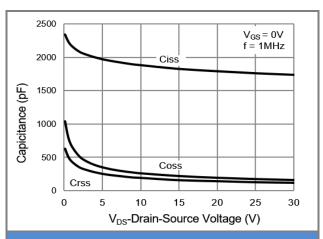


Fig.9 Threshold Voltage Variation with Temperature

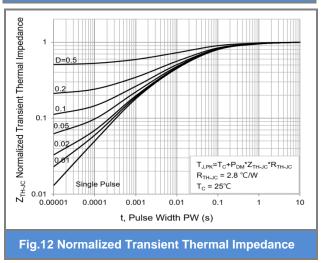










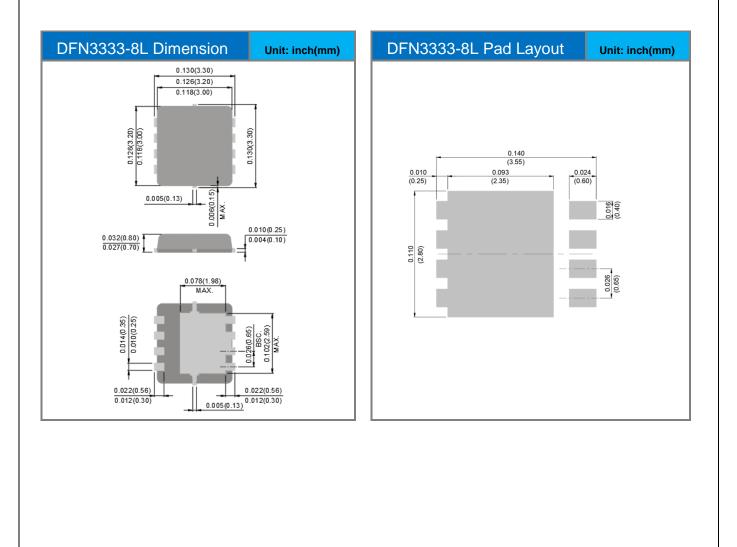




Part No. Packing Code Version

Part No. Packing Code	Package Type	Packing Type	Marking	Version
PJQ4442P_R2_00001	DFN3333-8L	5K pcs / 13" reel	4442	Halogen free RoHS compliant

Packaging Information & Mounting Pad Layout





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