



PJQ5606

30V Complementary Enhancement Mode MOSFET

Voltage

30/-30 V

Current

25/-22 A

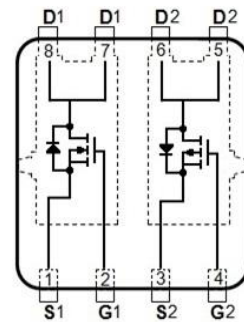
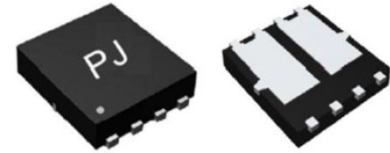
Features

- High switching speed
- Improved dv/dt capability
- Low Gate Charge
- Low reverse transfer capacitance
- Low reverse transfer capacitance
- Lead free in compliance with EU RoHS 2.0
- Green molding compound as per IEC 61249 standard

Mechanical Data

- Case : DFN5060B-8L Package
- Terminals : Solderable per MIL-STD-750, Method 2026
- Approx. Weight : 0.0035 ounces, 0.092 grams

DFN5060B-8L



Maximum Ratings and Thermal Characteristics (T_A=25 °C unless otherwise noted)

PARAMETER		SYMBOL	N-CH LIMIT	P-CH LIMIT	UNITS
Drain-Source Voltage		V _{DS}	30	-30	V
Gate-Source Voltage		V _{GS}	±20		
Continuous Drain Current (Note 4)	T _C =25°C	I _D	25	-22	A
	T _C =100°C		16	-14	
Pulsed Drain Current (Note 1)	T _C =25°C	I _{DM}	100	-88	
Power Dissipation	T _C =25°C	P _D	21		W
	T _C =100°C		8.4		
Continuous Drain Current (Note 4)	T _A =25°C	I _D	7	-6.1	A
	T _A =70°C		5.6	-5	
Power Dissipation	T _A =25°C	P _D	1.7		W
	T _A =70°C		1.1		
Operating Junction and Storage Temperature Range		T _J , T _{STG}	-55~150		°C
Typical Thermal Resistance (Note 4,5)	Junction to Case	R _{θJC}	6		°C/W
	Junction to Ambient	R _{θJA}	73.5		

- Limited only By Maximum Junction Temperature



PJQ5606

N-CH Electrical Characteristics ($T_A=25^\circ\text{C}$ unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNITS
Static						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=250\mu A$	30	-	-	V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	1	1.67	2.5	
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=8A$	-	16	19	m Ω
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS}=4.5V, I_D=5A$	-	22	28	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=30V, V_{GS}=0V$	-	-	1	μA
Gate-Source Leakage Current	I_{GSS}	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	± 100	nA
Dynamic (Note 6)						
Total Gate Charge	Q_g	$V_{DS}=15V, I_D=8A,$ $V_{GS}=4.5V$ (Note 2,3)	-	4.8	-	nC
Gate-Source Charge	Q_{gs}		-	1.5	-	
Gate-Drain Charge	Q_{gd}		-	2	-	
Input Capacitance	C_{iss}	$V_{DS}=25V, V_{GS}=0V,$ $f=1MHz$	-	429	-	pF
Output Capacitance	C_{oss}		-	59	-	
Reverse Transfer Capacitance	C_{rss}		-	47	-	
Turn-On Delay Time	$t_{d(on)}$	$V_{DS}=15V, I_D=1A,$ $V_{GS}=10V, R_G=6\Omega$ (Note 2,3)	-	6.8	-	ns
Turn-On Rise Time	t_r		-	16	-	
Turn-Off Delay Time	$t_{d(off)}$		-	27	-	
Turn-Off Fall Time	t_f		-	7.1	-	
Drain-Source Diode						
Maximum Continuous Drain-Source Diode Forward Current	I_S	---	-	-	25	A
Diode Forward Voltage	V_{SD}	$I_S=1A, V_{GS}=0V$	-	0.74	1	V



PJQ5606

P-CH Electrical Characteristics ($T_A=25^{\circ}\text{C}$ unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNITS
Static						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=-250\mu A$	-30	-	-	V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=-250\mu A$	-1	-1.53	-2.5	
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS}=-10V, I_D=-4A$	-	25	30	m Ω
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS}=-4.5V, I_D=-2A$	-	36	45	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=-30V, V_{GS}=0V$	-	-	-1	μA
Gate-Source Leakage Current	I_{GSS}	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	± 100	nA
Dynamic (Note 6)						
Total Gate Charge	Q_g	$V_{DS}=-15V, I_D=-4A,$ $V_{GS}=-4.5V$ (Note 1,2)	-	7.8	-	nC
Gate-Source Charge	Q_{gs}		-	2.7	-	
Gate-Drain Charge	Q_{gd}		-	2.8	-	
Input Capacitance	C_{iss}	$V_{DS}=-15V, V_{GS}=0V,$ $f=1\text{MHZ}$	-	846	-	pF
Output Capacitance	C_{oss}		-	120	-	
Reverse Transfer Capacitance	C_{rss}		-	76	-	
Turn-On Delay Time	$t_{d(on)}$	$V_{DS}=-15V, I_D=-1A,$ $V_{GS}=-10V, R_G=6\Omega$ (Note 1,2)	-	3.6	-	ns
Turn-On Rise Time	t_r		-	23	-	
Turn-Off Delay Time	$t_{d(off)}$		-	90	-	
Turn-Off Fall Time	t_f		-	50	-	
Drain-Source Diode						
Maximum Continuous Drain-Source Diode Forward Current	I_S	---	-	-	-22	A
Diode Forward Voltage	V_{SD}	$I_S=-1A, V_{GS}=0V$	-	-0.75	-1	V

NOTES :

1. Pulse width $\leq 300\mu s$, Duty cycle $\leq 2\%$.
2. Essentially independent of operating temperature typical characteristics.
3. Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}=150^{\circ}\text{C}$. Ratings are based on low frequency and duty cycles to keep initial $T_J=25^{\circ}\text{C}$.
4. The maximum current rating is package limited.
5. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. Mounted on a 1 inch² with 2oz.square pad of copper..
6. Guaranteed by design, not subject to production testing.



PJQ5606

N-CH TYPICAL CHARACTERISTIC CURVES

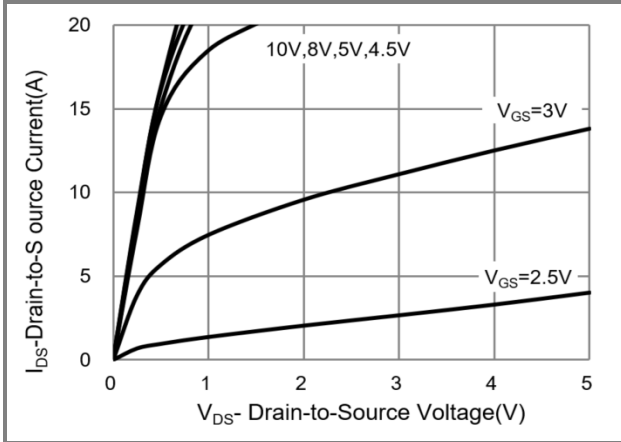


Fig.1 Output Characteristics

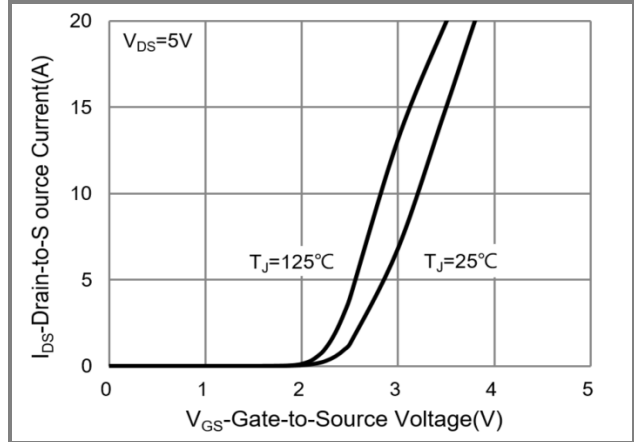


Fig.2 Transfer Characteristics

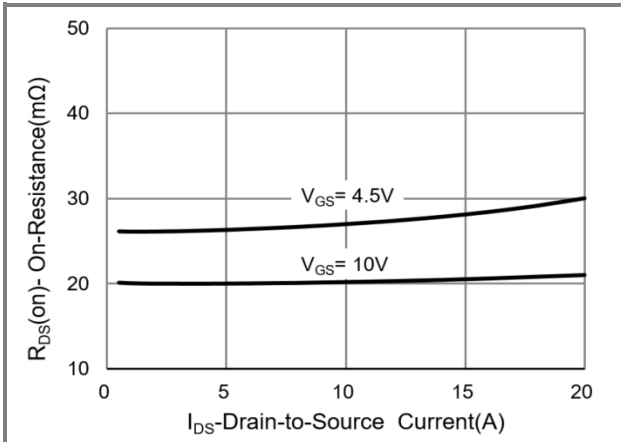


Fig.3 On-Resistance vs. Drain Current

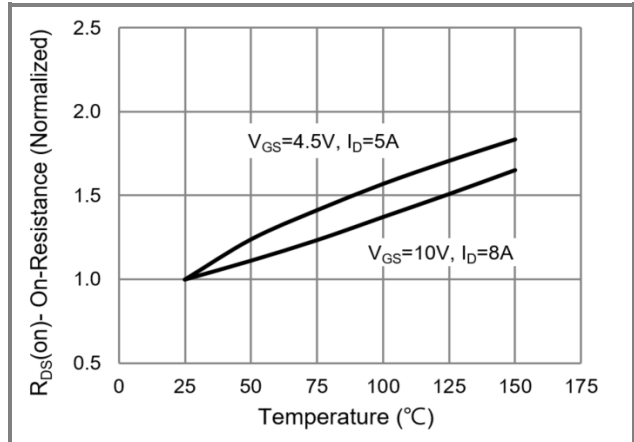


Fig.4 On-Resistance vs. Junction temperature

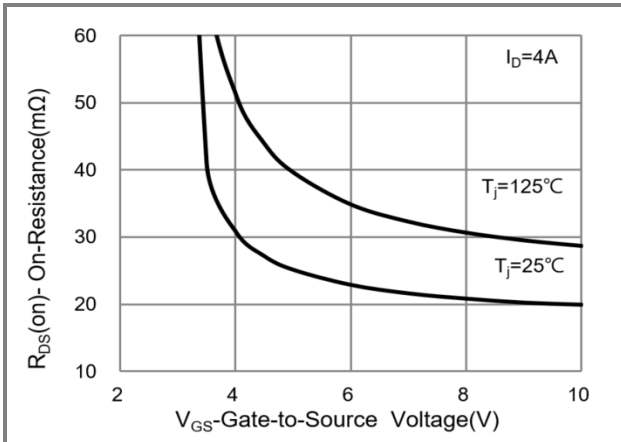


Fig.5 On-Resistance Variation with V_{GS}

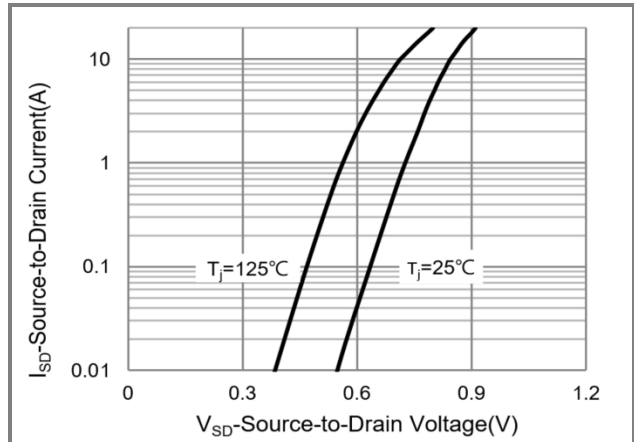


Fig.6 Source-Drain Diode Forward Voltage



PJQ5606

TYPICAL CHARACTERISTIC CURVES

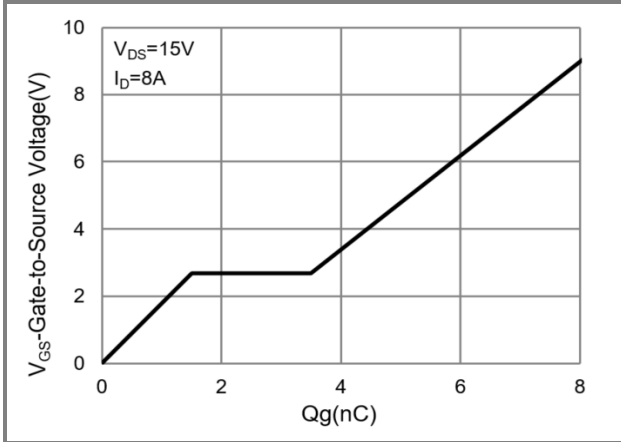


Fig.7 Gate-Charge Characteristics

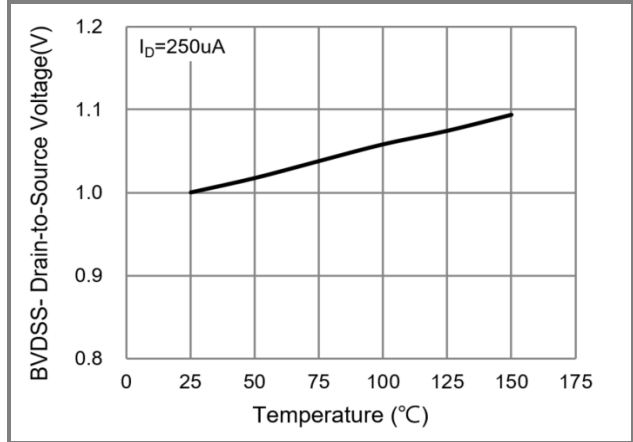


Fig.8 Breakdown Voltage Variation vs. Temperature

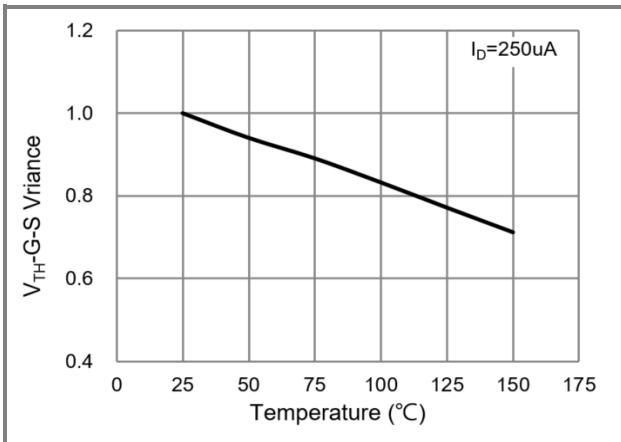


Fig.9 Threshold Voltage Variation with Temperature

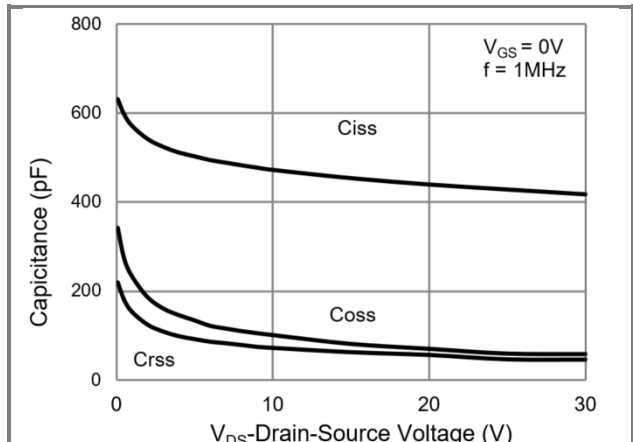


Fig.10 Capacitance vs. Drain-Source Voltage

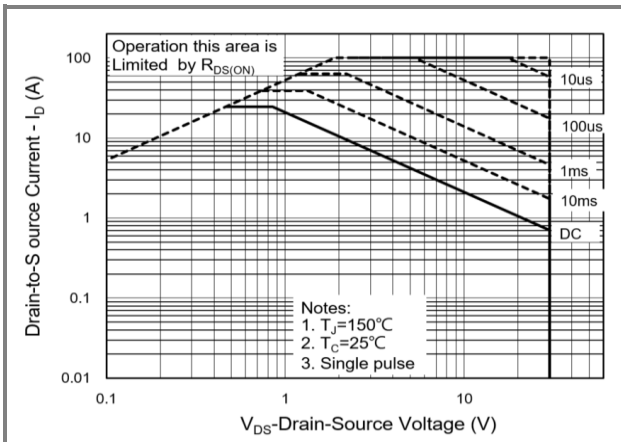


Fig.11 Maximum Safe Operating Area

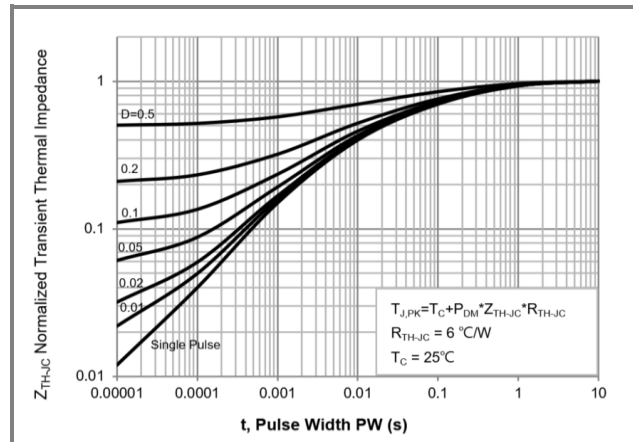


Fig.12 Normalized Transient Thermal Impedance



PJQ5606

P-CH TYPICAL CHARACTERISTIC CURVES

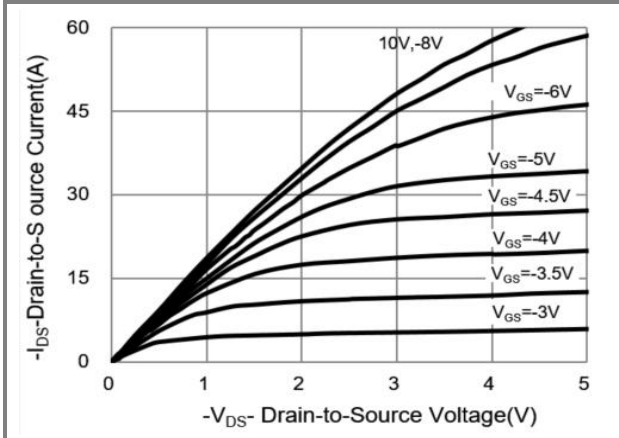


Fig.13 Output Characteristics

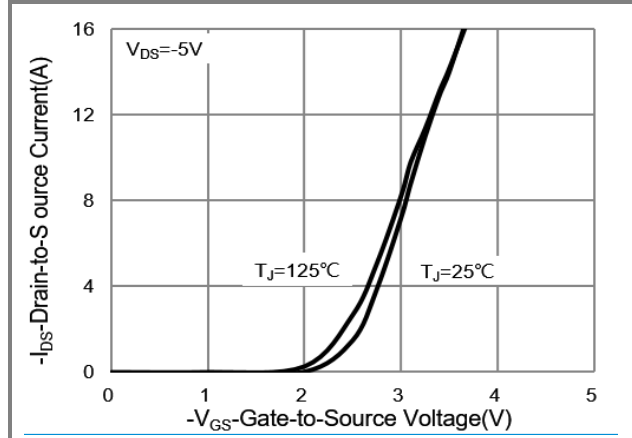


Fig.14 Transfer Characteristics

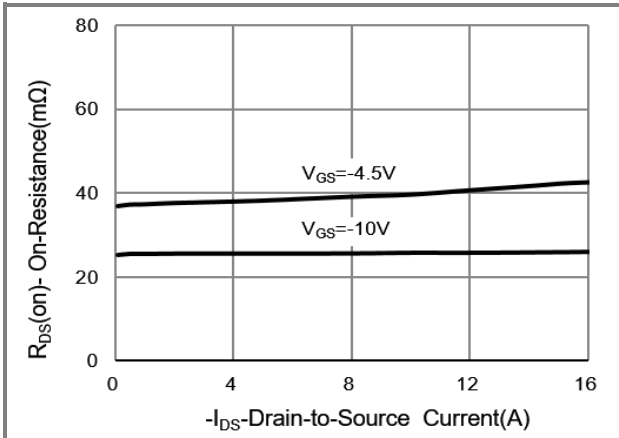


Fig.15 On-Resistance vs. Drain Current

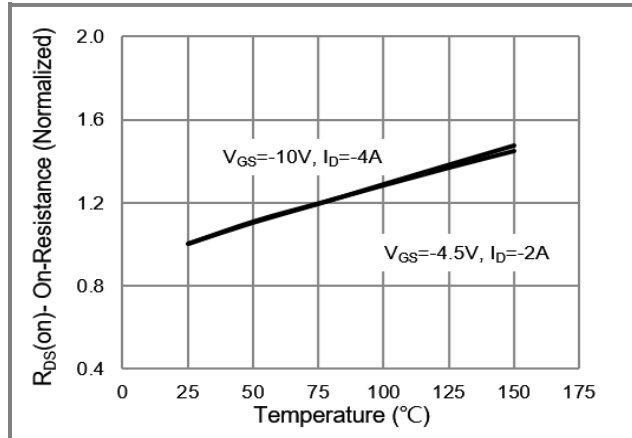


Fig.16 On-Resistance vs. Junction temperature

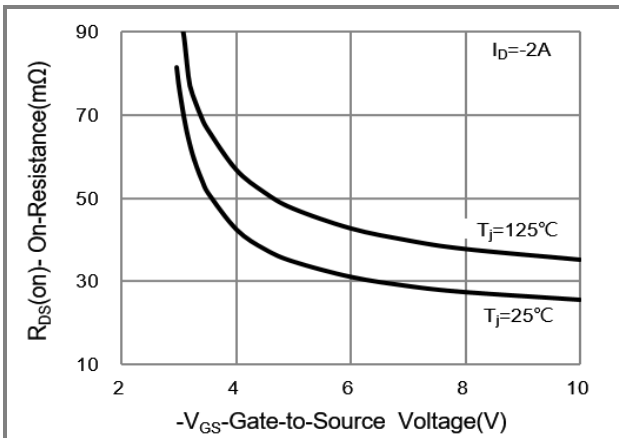


Fig.17 On-Resistance Variation with V_{GS}

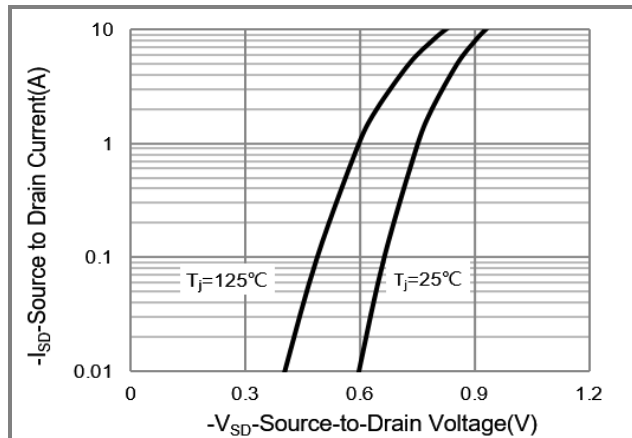


Fig.18 Source-Drain Diode Forward Voltage



PJQ5606

TYPICAL CHARACTERISTIC CURVES

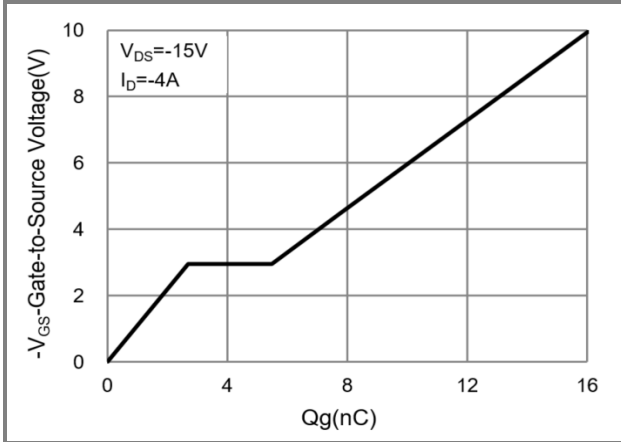


Fig.19 Gate-Charge Characteristics

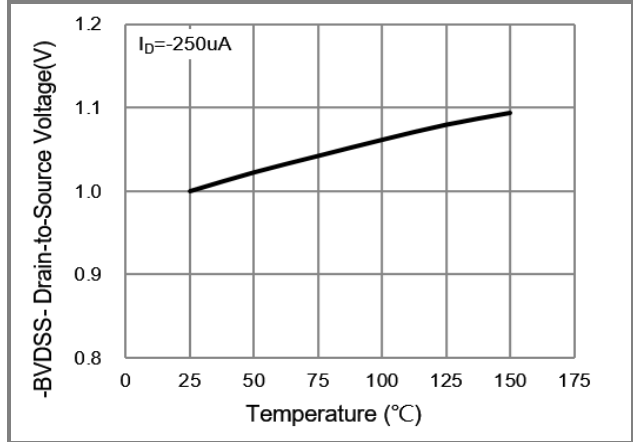


Fig.20 Breakdown Voltage Variation vs. Temperature

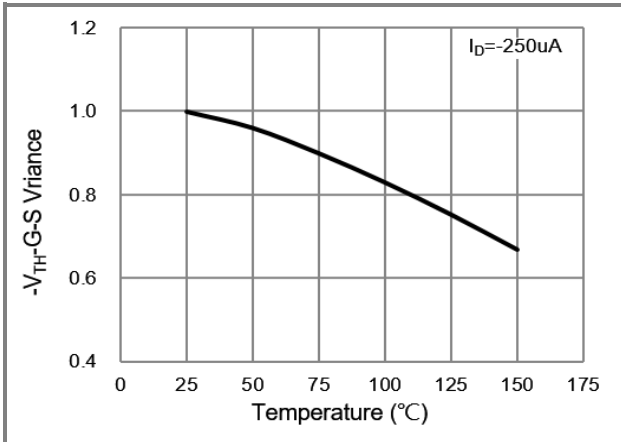


Fig.21 Threshold Voltage Variation with Temperature

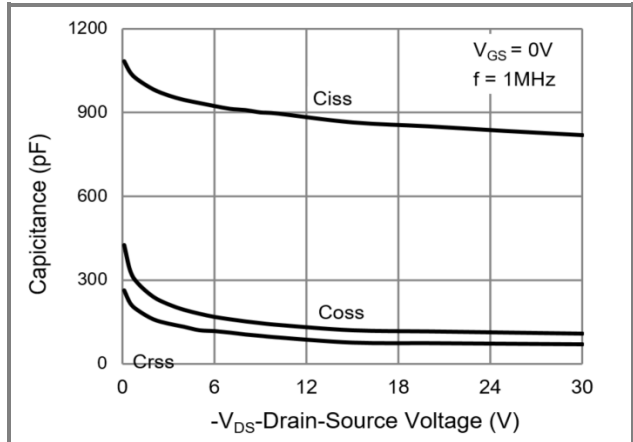


Fig.22 Capacitance vs. Drain-Source Voltage

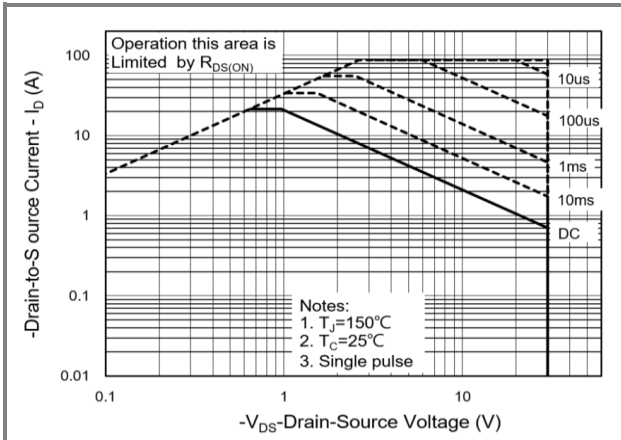


Fig.23 Maximum Safe Operating Area

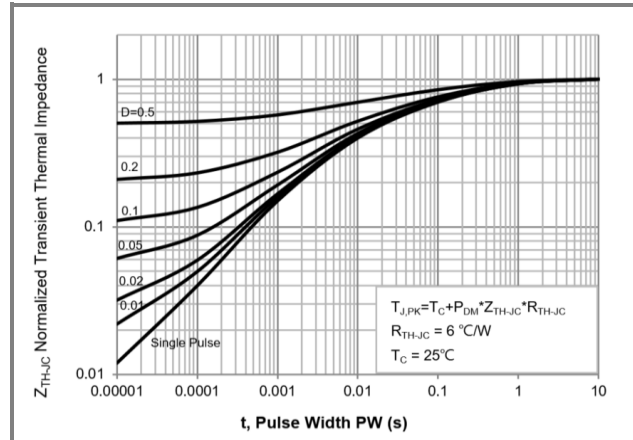


Fig.24 Normalized Transient Thermal Impedance

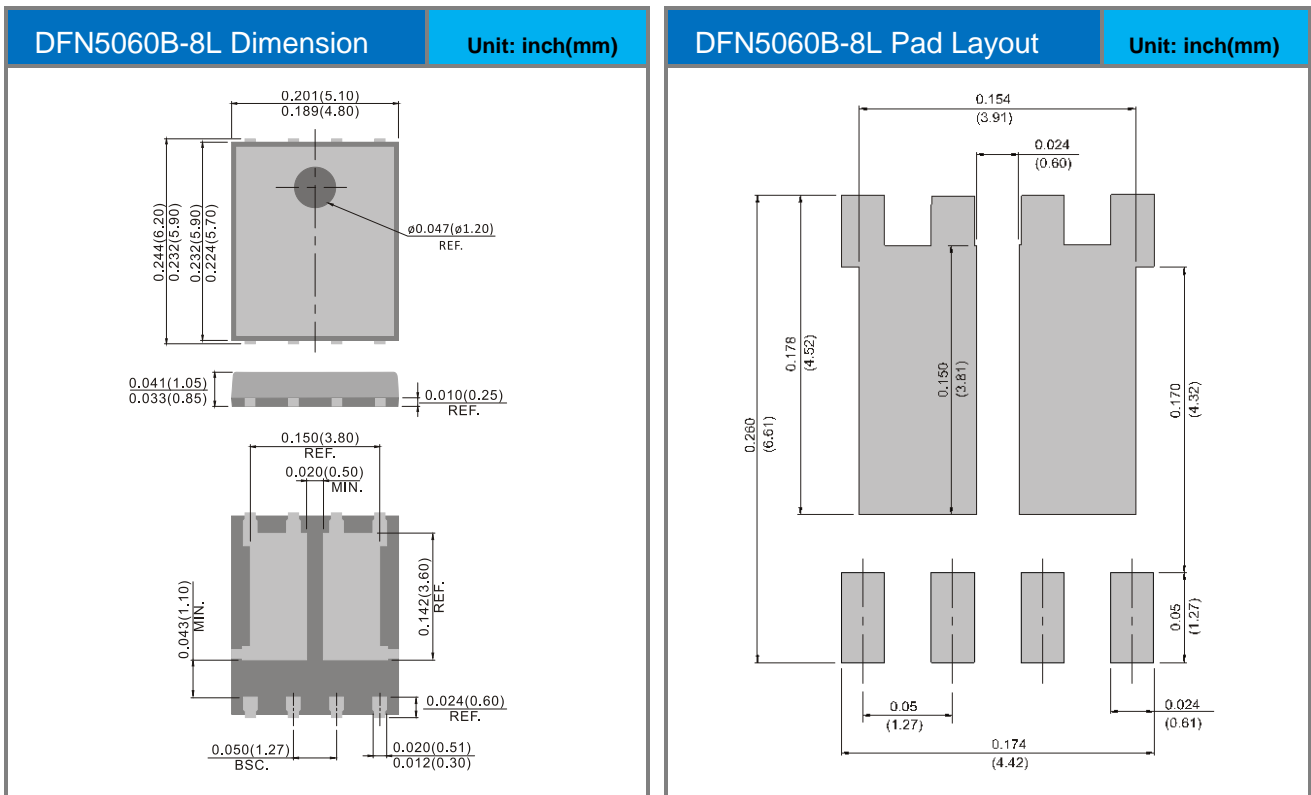


PJQ5606

Part No Packing Code Version

Part No Packing Code	Package Type	Packing Type	Marking	Version
PJQ5606_R2_00001	DFN5060B-8L	3000pcs / 13" reel	Q5606	Halogen free

Packaging Information & Mounting Pad Layout





PJQ5606

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