



PJQ5548V-AU

40V N-Channel Enhancement Mode MOSFET

Voltage

40 V

Current

45 A

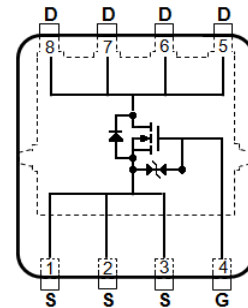
Features

- $R_{DS(ON)}$, $V_{GS}@10V$, $I_D@20A<10m\Omega$
- $R_{DS(ON)}$, $V_{GS}@7V$, $I_D@10A<12.4m\Omega$
- Excellent FOM
- Standard Level Drive
- AEC-Q101 qualified
- Lead free in compliance with EU RoHS 2.0
- Green molding compound as per IEC 61249 standard

Mechanical Data

- Case : DFN5060-8L Package
- Terminals : Solderable per MIL-STD-750, Method 2026
- Approx. Weight : 0.08 grams

DFN5060-8L



Maximum Ratings and Thermal Characteristics ($T_A=25^\circ\text{C}$ unless otherwise noted)

PARAMETER		SYMBOL	LIMIT	UNITS
Drain-Source Voltage		V_{DS}	40	V
Gate-Source Voltage		V_{GS}	± 20	V
Continuous Drain Current ^(Note 3)	$T_C=25^\circ\text{C}$	I_D	45	A
	$T_C=100^\circ\text{C}$		32	
Pulsed Drain Current ^(Note 1)	$T_C=25^\circ\text{C}$	I_{DM}	180	
Power Dissipation	$T_C=25^\circ\text{C}$	P_D	36	W
	$T_C=100^\circ\text{C}$		18	
Continuous Drain Current ^(Note 4)	$T_A=25^\circ\text{C}$	I_D	13.6	A
	$T_A=70^\circ\text{C}$		11.4	
Power Dissipation	$T_A=25^\circ\text{C}$	P_D	3.3	W
	$T_A=70^\circ\text{C}$		2.3	
Single Pulse Avalanche Energy ^(Note 5)		E_{AS}	42	mJ
Operating Junction and Storage Temperature Range		T_J, T_{STG}	-55~175	$^\circ\text{C}$
Thermal Resistance ^(Note 4)	Junction to Case	$R_{\theta JC}$	4.2	$^\circ\text{C/W}$
	Junction to Ambient	$R_{\theta JA}$	45	



PJQ5548V-AU

Electrical Characteristics (T_A=25°C unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNITS
Static						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V, I _D =250uA	40	-	-	V
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =50uA	2	2.8	3.5	
Drain-Source On-State Resistance	R _{DS(on)}	V _{GS} =10V, I _D =20A	-	8	10	mΩ
		V _{GS} =7V, I _D =10A	-	9.5	12.4	
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =40V, V _{GS} =0V	-	-	1	uA
Gate-Source Leakage Current	I _{GSS}	V _{GS} =±20V, V _{DS} =0V	-	-	±10	uA
		V _{GS} =±10V, V _{DS} =0V	-	-	±1	
Dynamic (Note 6)						
Total Gate Charge	Q _g	V _{DS} =32V, I _D =20A, V _{GS} =10V	-	9.5	-	nC
Gate-Source Charge	Q _{gs}		-	4.2	-	
Gate-Drain Charge	Q _{gd}		-	2.6	-	
Input Capacitance	C _{iss}	V _{DS} =25V, V _{GS} =0V, f=1MHz	-	673	-	pF
Output Capacitance	C _{oss}		-	176	-	
Reverse Transfer Capacitance	C _{rss}		-	29	-	
Gate resistance	R _g	f=1MHz	-	1.4	-	Ω
Turn-On Delay Time	t _{d(on)}	V _{DS} =32V, I _D =20A, V _{GS} =10V, R _G =3Ω (Note 2)	-	13	-	ns
Turn-On Rise Time	t _r		-	85	-	
Turn-Off Delay Time	t _{d(off)}		-	17	-	
Turn-Off Fall Time	t _f		-	38	-	
Drain-Source Diode						
Diode Forward Current	I _s	T _C =25°C	-	-	45	A
Pulsed Diode Forward Current	I _{SM}		-	-	180	
Diode Forward Voltage	V _{SD}	I _S =20A, V _{GS} =0V	-	0.9	1.3	V
Reverse Recovery Time	T _{rr}	V _{GS} =0V, I _S =20A	-	24	-	ns
Reverse Recovery Charge	Q _{rr}	di _S /dt=100A/us	-	14	-	nC

NOTES :

1. Pulse width≤100us, Duty cycle≤2%.
2. Essentially independent of operating temperature typical characteristics.
3. Chip capability with an R_{θJC}=4.2°C/W.
4. R_{θJA} is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. Mounted on a 1 inch² with 2oz.square pad of copper.
5. The test condition is L=0.5mH, I_{AS}=13A, V_{DD}=30V, V_{GS}=10V, Starting T_J=25°C.
6. Guaranteed by design, not subject to production testing.



PJQ5548V-AU

TYPICAL CHARACTERISTIC CURVES

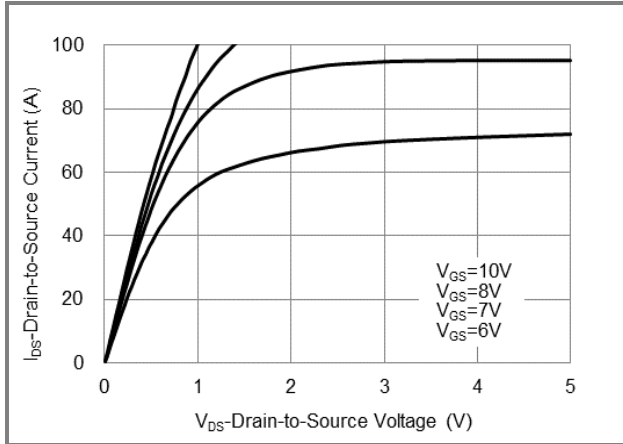


Fig.1 On-Region Characteristics

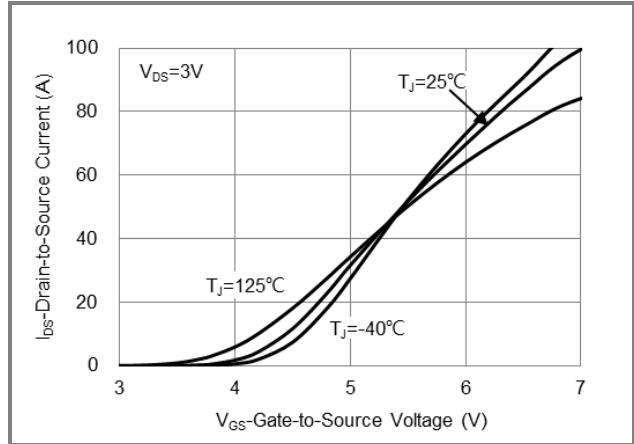


Fig.2 Transfer Characteristics

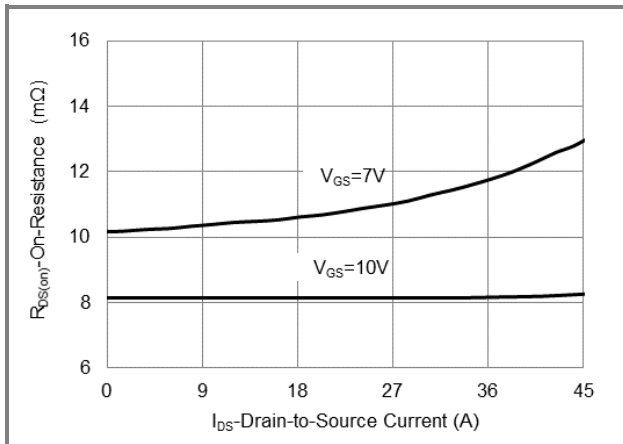


Fig.3 On-Resistance vs. Drain Current

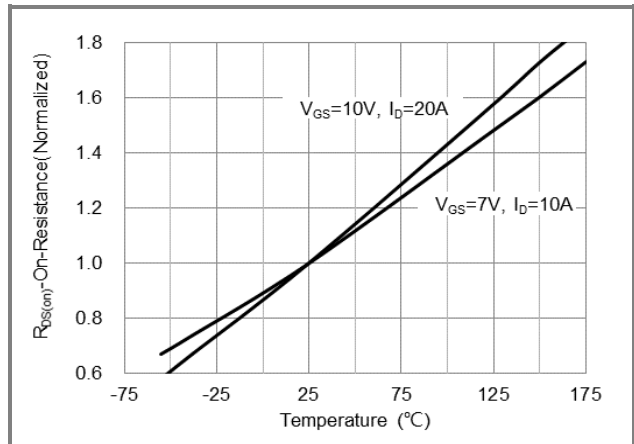


Fig.4 On-Resistance vs. Junction temperature

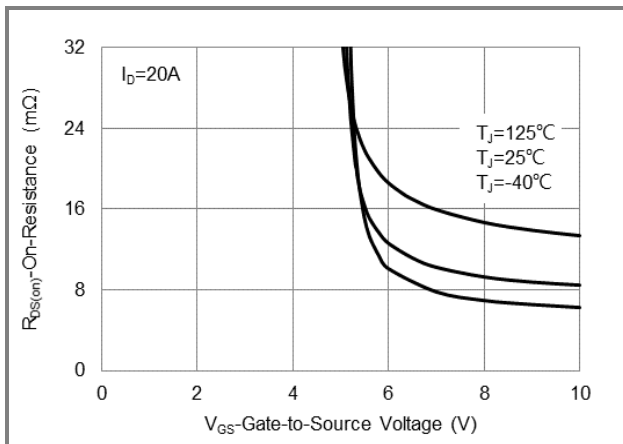


Fig.5 On-Resistance Variation with Vgs

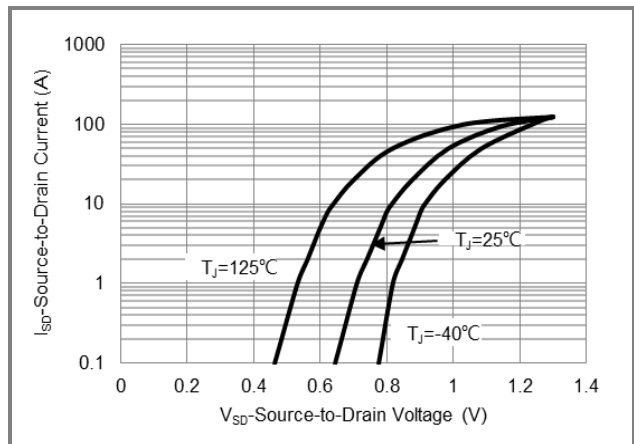


Fig.6 Source-Drain Diode Forward Voltage



PJQ5548V-AU

TYPICAL CHARACTERISTIC CURVES

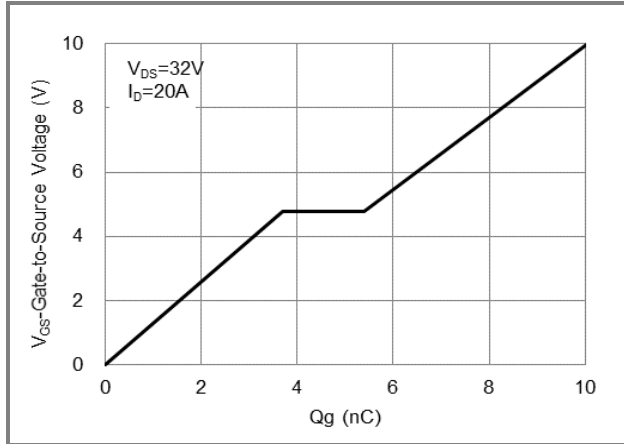


Fig.7 Gate-Charge Characteristics

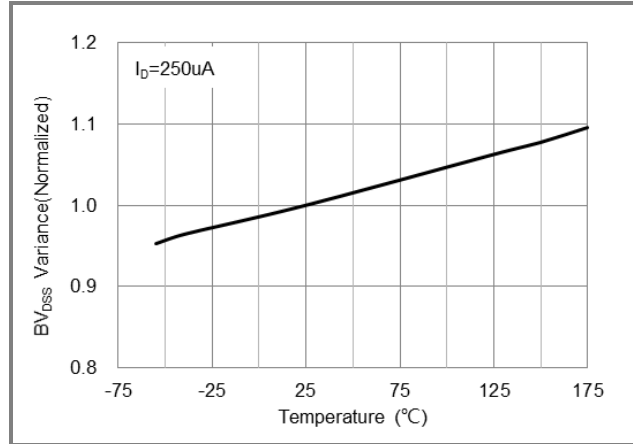


Fig.8 Breakdown Voltage Variation vs. Temperature

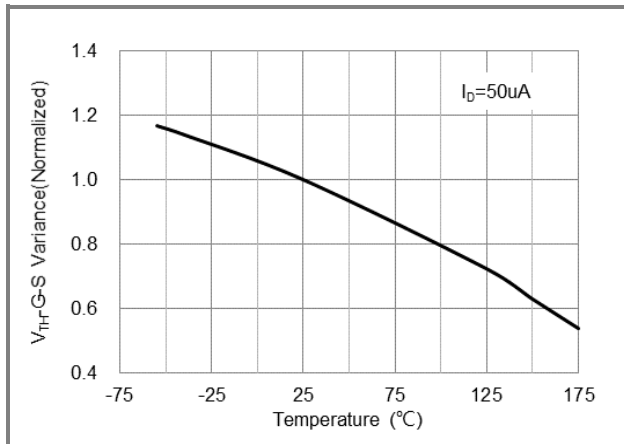


Fig.9 Threshold Voltage Variation with Temperature

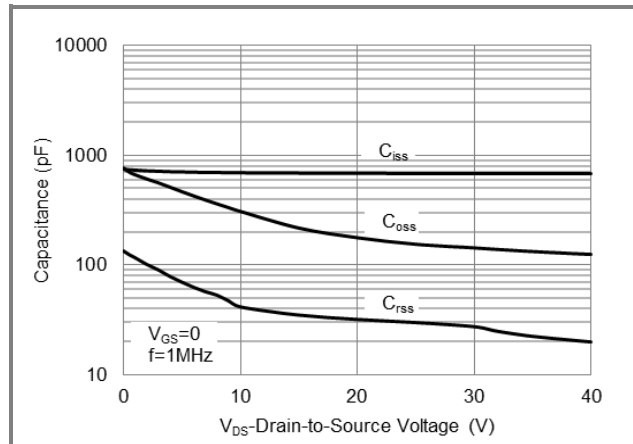


Fig.10 Capacitance vs. Drain-Source Voltage

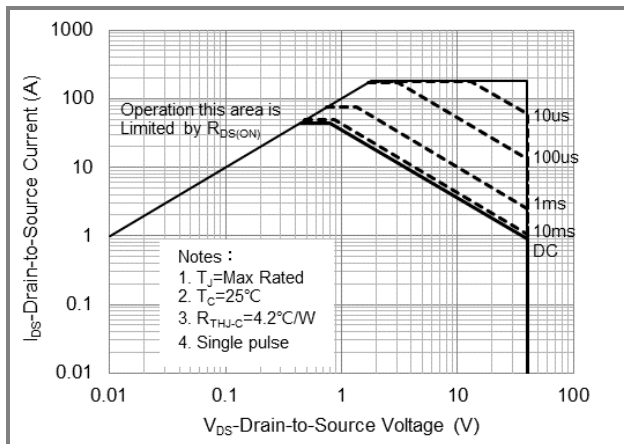


Fig.11 Maximum Safe Operating Area

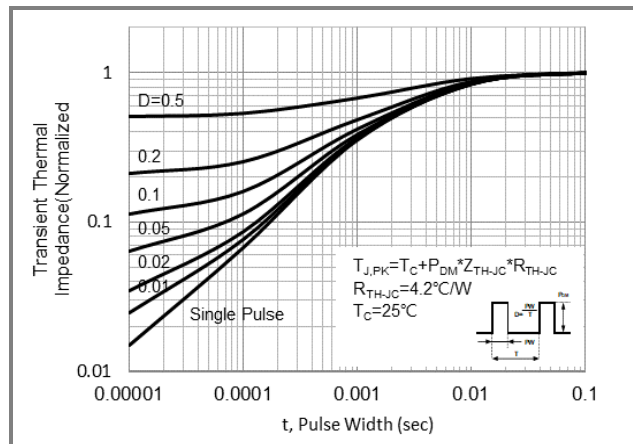


Fig.12 Normalized Transient Thermal Impedance

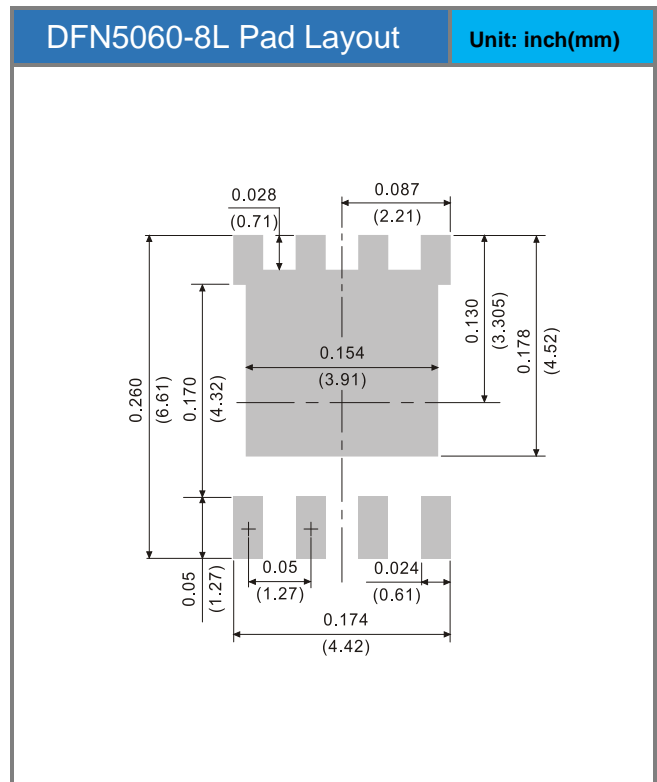
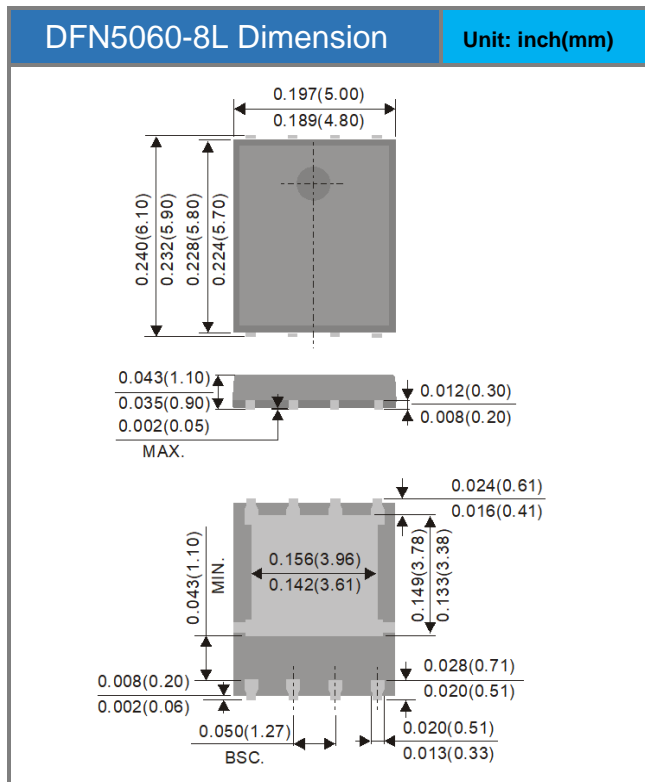


PJQ5548V-AU

Part No. Packing Code Version

Part No. Packing Code	Package Type	Packing Type	Marking	Version
PJQ5548V-AU_R2_002A1	DFN5060-8L	3K pcs / 13" reel	Q5548V	Halogen free RoHS compliant

Packaging Information & Mounting Pad Layout





PJQ5548V-AU

Disclaimer

- Reproducing and modifying information of the document is prohibited without permission from Panjit International Inc..
- Panjit International Inc. reserves the rights to make changes of the content herein the document anytime without notification. Please refer to our website for the latest document.
- Panjit International Inc. disclaims any and all liability arising out of the application or use of any product including damages incidentally and consequentially occurred.
- Panjit International Inc. does not assume any and all implied warranties, including warranties of fitness for particular purpose, non-infringement and merchantability.
- Applications shown on the herein document are examples of standard use and operation. Customers are responsible in comprehending the suitable use in particular applications. Panjit International Inc. makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.
- The products shown herein are not designed and authorized for equipments relating to human life and for any applications concerning life-saving or life-sustaining, such as medical instruments, aerospace machinery et cetera. Customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Panjit International Inc. for any damages resulting from such improper use or sale.
- Since Panjit uses lot number as the tracking base, please provide the lot number for tracking when complaining.

单击下面可查看定价，库存，交付和生命周期等信息

[>>Panjit\(强茂\)](#)