

PJD55N04S-AU

40V N-Channel Enhancement Mode MOSFET

Voltage 40 V **Current** 87 A

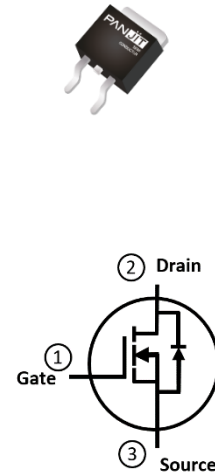
Features

- $R_{DS(ON)}$, $V_{GS}@10V$, $I_D@20A < 5.3m\Omega$
- $R_{DS(ON)}$, $V_{GS}@4.5V$, $I_D@20A < 7.4m\Omega$
- Excellent FOM
- Logic Level Drive
- AEC-Q101 qualified
- Lead free in compliance with EU RoHS 2.0
- Green molding compound as per IEC 61249 standard

Mechanical Data

- Case : TO-252AA Package
- Terminals : Solderable per MIL-STD-750, Method 2026
- Approx. Weight : 0.3217 grams

TO-252AA



Maximum Ratings and Thermal Characteristics ($T_A=25^\circ\text{C}$ unless otherwise noted)

PARAMETER		SYMBOL	LIMIT	UNITS
Drain-Source Voltage		V_{DS}	40	V
Gate-Source Voltage		V_{GS}	± 20	
Continuous Drain Current ^(Note 3)	$T_C=25^\circ\text{C}$	I_D	87	A
	$T_C=100^\circ\text{C}$		61	
Pulsed Drain Current ^(Note 1)	$T_C=25^\circ\text{C}$	I_{DM}	348	
Power Dissipation	$T_C=25^\circ\text{C}$	P_D	71	W
	$T_C=100^\circ\text{C}$		36	
Continuous Drain Current ^(Note 4)	$T_A=25^\circ\text{C}$	I_D	17.7	A
	$T_A=70^\circ\text{C}$		14.8	
Power Dissipation	$T_A=25^\circ\text{C}$	P_D	3	W
	$T_A=70^\circ\text{C}$		2.1	
Single Pulse Avalanche Energy ^(Note 5)		E_{AS}	49	mJ
Operating Junction and Storage Temperature Range		T_J, T_{STG}	-55~175	$^\circ\text{C}$
Thermal Resistance ^(Note 4)	Junction to Case	$R_{\theta JC}$	2.1	$^\circ\text{C/W}$
	Junction to Ambient	$R_{\theta JA}$	50	

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Electrical Characteristics (T_A=25°C unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNITS
Static						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V, I _D =250uA	40	-	-	V
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =50uA	1.1	1.7	2.3	
Drain-Source On-State Resistance	R _{DS(on)}	V _{GS} =10V, I _D =20A	-	4.2	5.3	mΩ
		V _{GS} =4.5V, I _D =20A	-	5.7	7.4	
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =40V, V _{GS} =0V	-	-	±1	uA
Gate-Source Leakage Current	I _{GSS}	V _{GS} =±20V, V _{DS} =0V	-	-	±100	nA
Dynamic (Note 6)						
Total Gate Charge	Q _g	V _{DS} =32V, I _D =20A, V _{GS} =10V	-	20	-	nC
Gate-Source Charge	Q _{gs}		-	3.1	-	
Gate-Drain Charge	Q _{gd}		-	6.4	-	
Input Capacitance	C _{iss}	V _{DS} =25V, V _{GS} =0V, f=1MHz	-	1328	-	pF
Output Capacitance	C _{oss}		-	276	-	
Reverse Transfer Capacitance	C _{rss}		-	31	-	
Gate resistance	R _g	f=1MHz	-	0.8	-	Ω
Turn-On Delay Time	t _{d(on)}	V _{DS} =32V, I _D =20A, V _{GS} =10V, R _G =3Ω (Note 2)	-	11	-	ns
Turn-On Rise Time	t _r		-	3	-	
Turn-Off Delay Time	t _{d(off)}		-	28	-	
Turn-Off Fall Time	t _f		-	5	-	
Drain-Source Diode						
Diode Forward Current	I _S	T _C =25°C	-	-	87	A
Pulsed Diode Forward Current	I _{SM}		-	-	348	
Diode Forward Voltage	V _{SD}	I _S =20A, V _{GS} =0V	-	0.85	1.3	V
Reverse Recovery Time	T _{rr}	V _{GS} =0V, I _S =20A	-	23	-	ns
Reverse Recovery Charge	Q _{rr}	dI _S /dt=100A/us	-	15	-	nC

NOTES :

1. Pulse width ≤ 100us, Duty cycle ≤ 2%.
2. Essentially independent of operating temperature typical characteristics.
3. Chip capability with an R_{θJC}=2.1°C/W.
4. R_{θJA} is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. Mounted on a 1 inch² with 2oz.square pad of copper.
5. The test condition is L=0.5mH, I_{AS}=14A, V_{DD}=30V, V_{GS}=10V, Starting T_J=25°C. the chip is about to carry I_{AS}=28A.
6. Guaranteed by design, not subject to production testing.

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TYPICAL CHARACTERISTIC CURVES

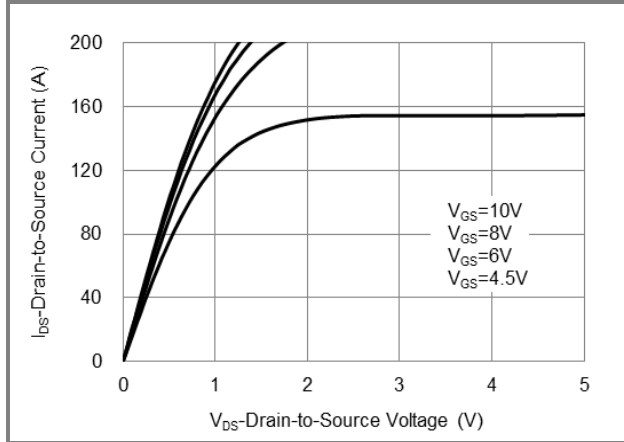


Fig.1 On-Region Characteristics

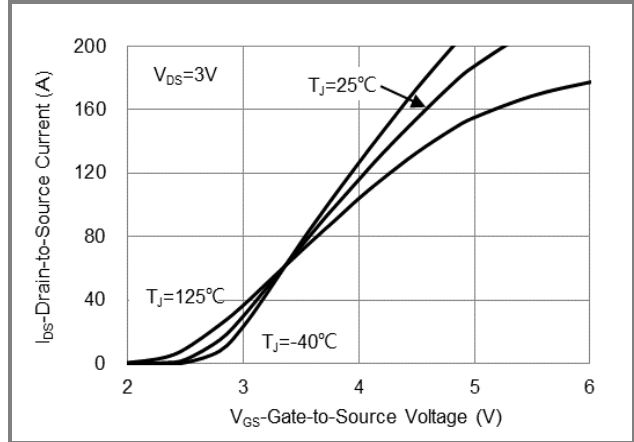


Fig.2 Transfer Characteristics

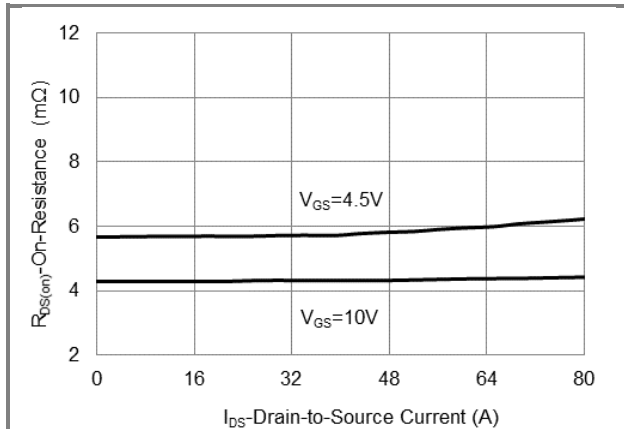


Fig.3 On-Resistance vs. Drain Current

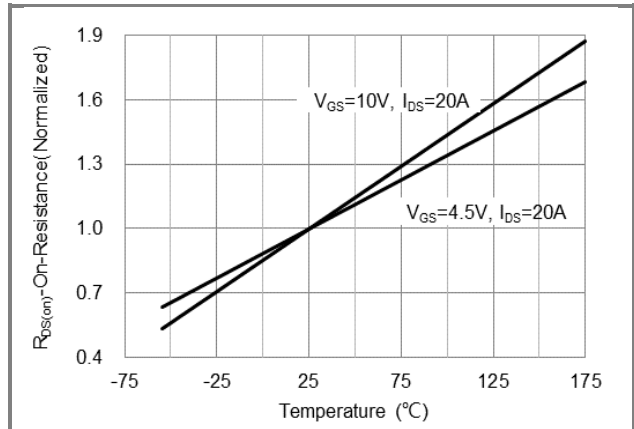


Fig.4 On-Resistance vs. Junction temperature

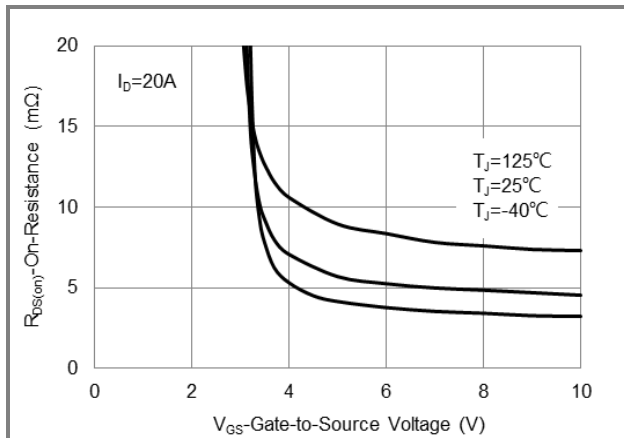


Fig.5 On-Resistance Variation with Vgs

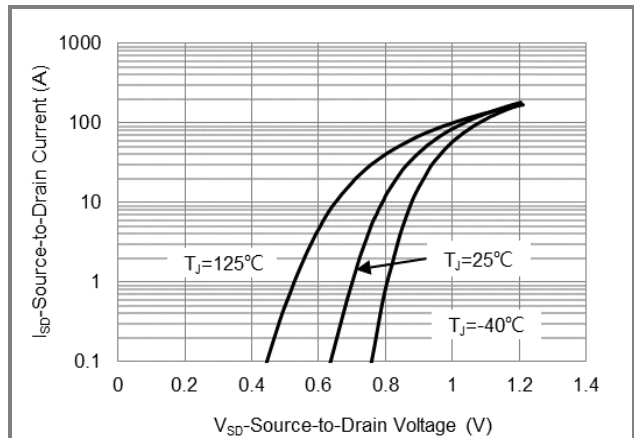


Fig.6 Source-Drain Diode Forward Voltage

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TYPICAL CHARACTERISTIC CURVES

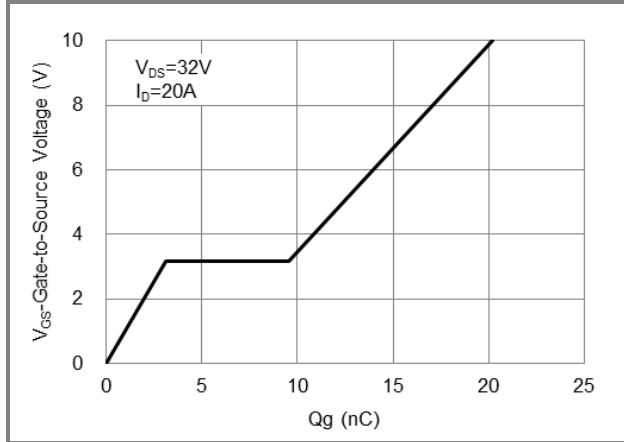


Fig.7 Gate-Charge Characteristics

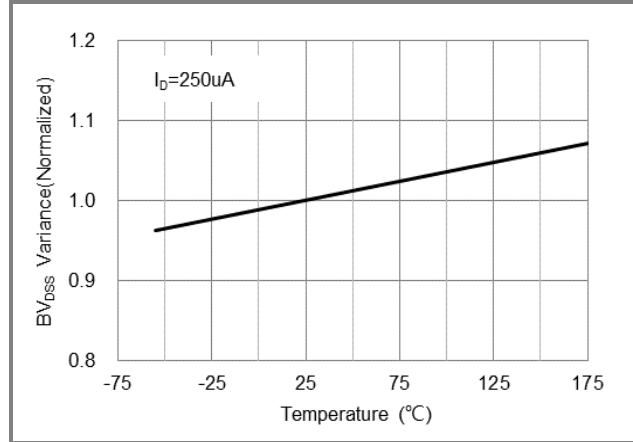


Fig.8 Breakdown Voltage Variation vs. Temperature

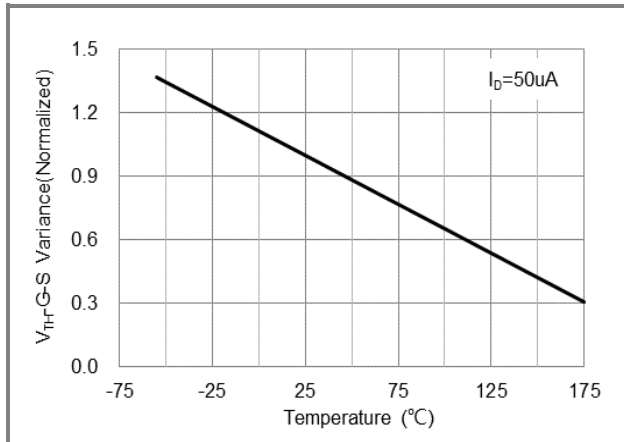


Fig.9 Threshold Voltage Variation with Temperature

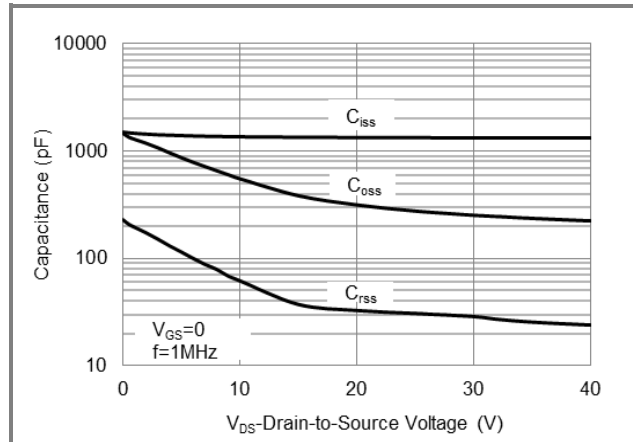


Fig.10 Capacitance vs. Drain-Source Voltage

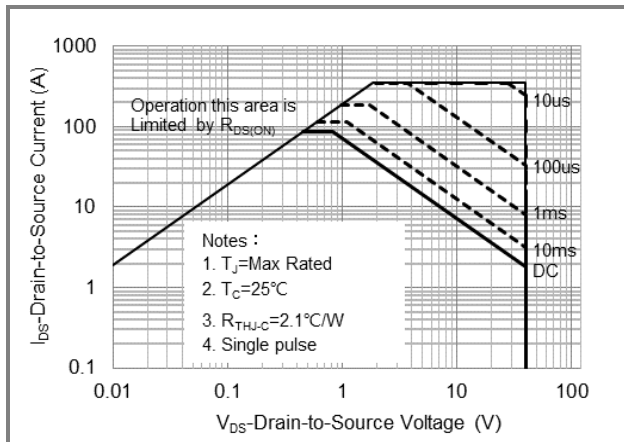


Fig.11 Maximum Safe Operating Area

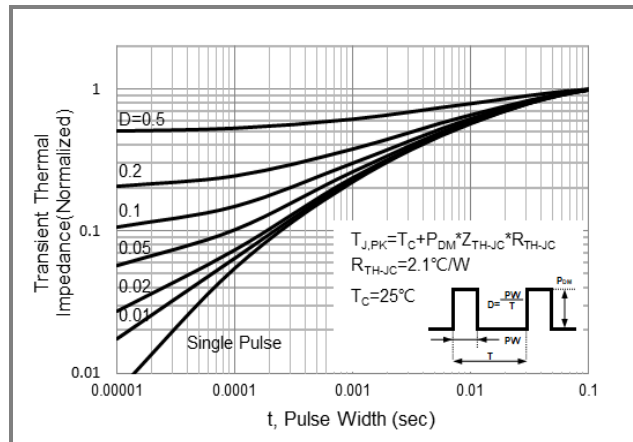


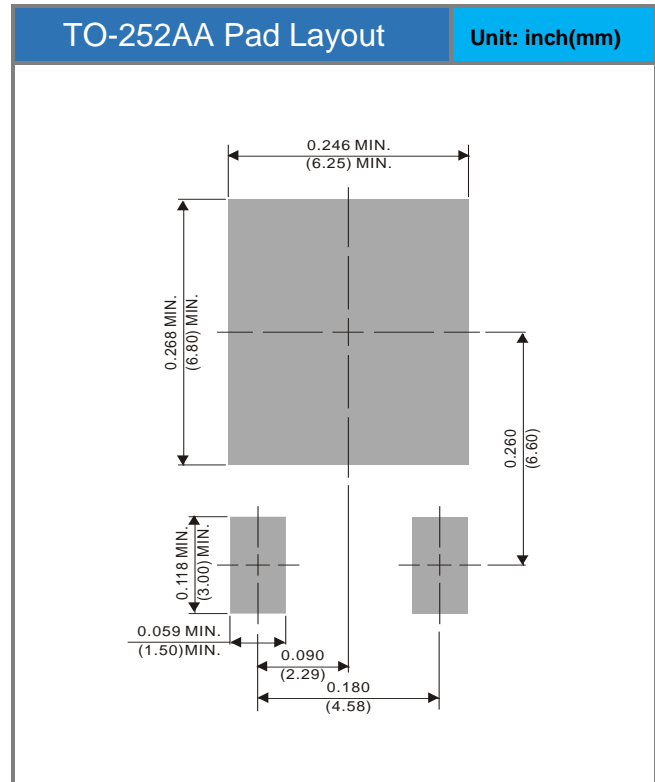
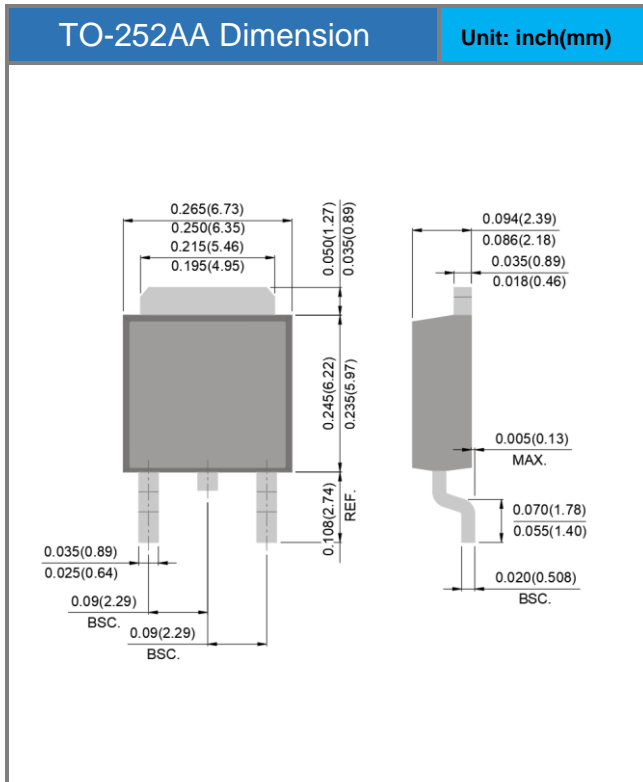
Fig.12 Normalized Transient Thermal Impedance

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Product and Packing Information

Part No.	Package Type	Packing Type	Marking
PJD55N04S-AU	TO-252AA	3K pcs / 13" reel	D55N04S

Packaging Information & Mounting Pad Layout



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