PAN	JIT
	SEMI CONDUCTOR

### 60V P-Channel Enhancement Mode MOSFET

Current

-1.9A

#### Features

Voltage

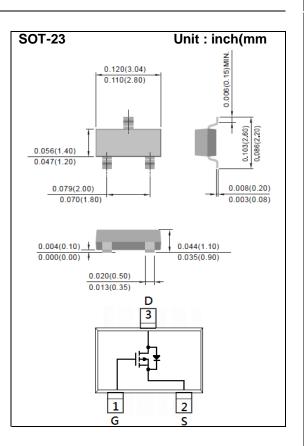
• Rds(on) , Vgs@-10V, Id@-1.9A<190mΩ

-60 V

- Rds(on) , Vgs@-4.5V, Id@-1.5A<240mΩ
- Advanced Trench Process Technology
- Specially Designed for Switch Load, PWM Application, etc
- Lead free in compliance with EU RoHS 2011/65/EU directive.
- Green molding compound as per IEC61249 Std. (Halogen Free)

#### **Mechanical Data**

- Case: SOT-23 Package
- Terminals : Solderable per MIL-STD-750, Method 2026
- Approx. Weight: 0.0003 ounces, 0.0084 grams
- Marking: A61



### **Maximum Ratings and Thermal Characteristics** (T<sub>A</sub>=25<sup>°</sup>C unless otherwise noted)

PARAMETER		SYMBOL	LIMIT	UNITS
Drain-Source Voltage		V <sub>DS</sub>	-60	V
Gate-Source Voltage		V <sub>GS</sub>	<u>+</u> 20	V
Continuous Drain Current	T <sub>A</sub> =25°C		-1.9	
	T <sub>A</sub> =70°C	I <sub>D</sub>	-1.5	A
Pulsed Drain Current (Note 1)		I <sub>DM</sub>	-7.6	А
Power Dissipation	T <sub>A</sub> =25°C	_	1.25	
	T <sub>A</sub> =70°C	P <sub>D</sub>	0.8	W
Single Pulse Avalanche Energy (Note 5)		E <sub>AS</sub>	32	mJ
Operating Junction and Storage Temperature Range		TJ,TSTG	-55~150	°C
Typical Thermal resistance - Junction to Ambient <sup>(Note 6)</sup>		R <sub>θJA</sub>	100	°C/W



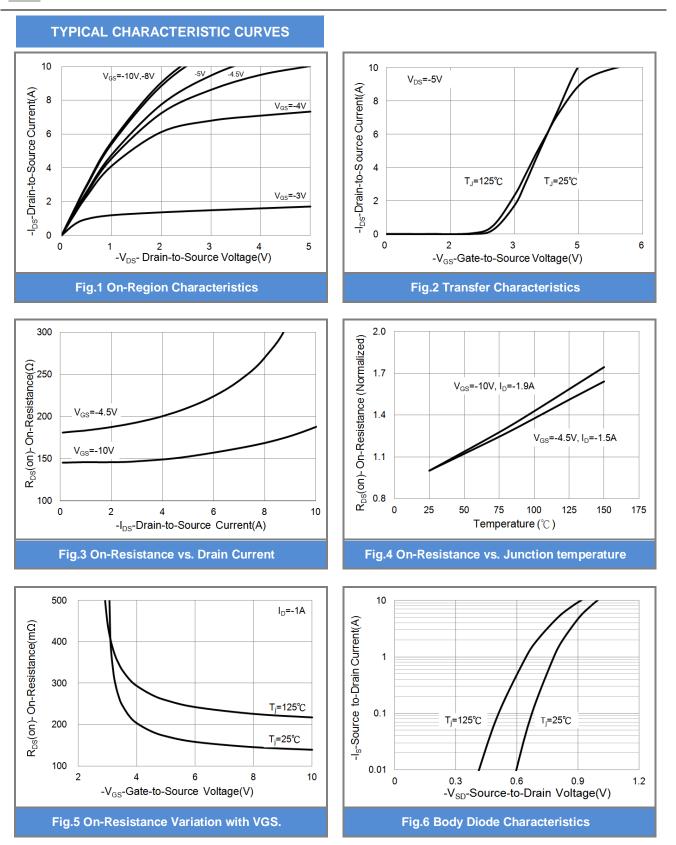
## **Electrical Characteristics** ( $T_A=25^{\circ}C$ unless otherwise noted)

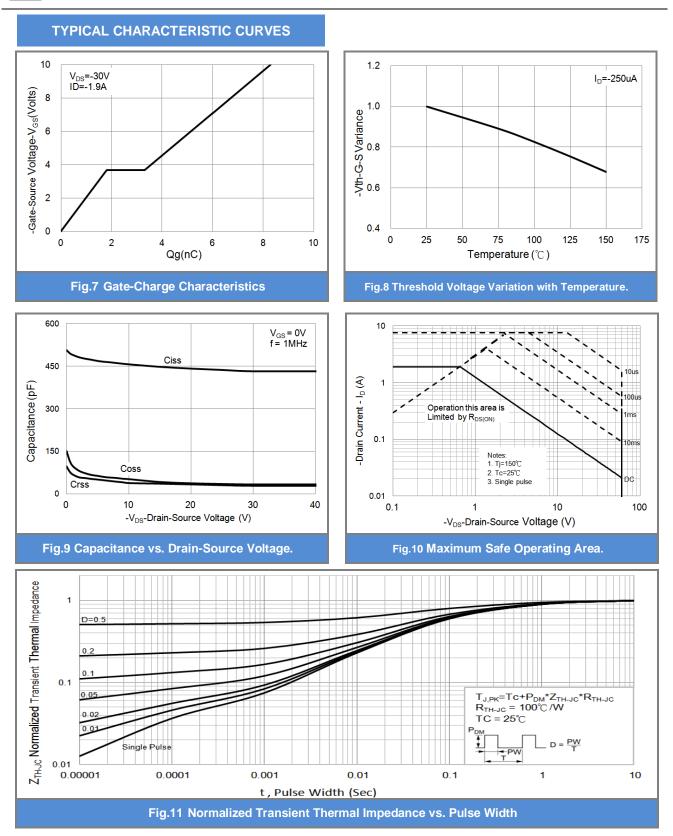
PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNITS
Static						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> =0V, I <sub>D</sub> =-250uA	-60	-	-	V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}$ , $I_{D}=-250$ uA	-1.0	-1.88	-2.5	V
Drain-Source On-State Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> =-10V, I <sub>D</sub> =-1.9A	-	140	190	
		V <sub>GS</sub> =-4.5V, I <sub>D</sub> =-1.5A	-	190	240	mΩ
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =-60V, V <sub>GS</sub> =0V	-	-	-1	uA
Gate-Source Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> = <u>+</u> 20V, V <sub>DS</sub> =0V	-	-	<u>+</u> 100	nA
Dynamic (Note 7)						
Total Gate Charge	$Q_{g}$	V <sub>DS</sub> =-30V, I <sub>D</sub> =-1.9A, V <sub>GS</sub> =-10V <sup>(Note 1,2)</sup>	-	8.3	-	nC
Gate-Source Charge	$Q_gs$		-	1.8	-	
Gate-Drain Charge	$Q_gd$		-	1.6	-	
Input Capacitance	Ciss	$V_{DS}$ =-30V, $V_{GS}$ =0V,	-	430	-	pF
Output Capacitance	Coss		-	33	-	
Reverse Transfer Capacitance	Crss	f=1.0MHZ	-	29	-	
Turn-On Delay Time	td <sub>(on)</sub>		-	5.1	-	ns
Turn-On Rise Time	tr	$V_{DD}$ =-30V, $I_{D}$ =-1.0A, $V_{GS}$ =-10V, $R_{G}$ =6 $\Omega$ <sup>(Note 1,2)</sup>	-	20	-	
Turn-Off Delay Time	td <sub>(off)</sub>		-	36	-	
Turn-Off Fall Time	tf	K <sub>G</sub> =012	-	11	-	
Drain-Source Diode						
Maximum Continuous Drain-Source					-1.5	A
Diode Forward Current	I <sub>S</sub>		-	-		
Diode Forward Voltage	$V_{SD}$	I <sub>S</sub> =-1.0A, V <sub>GS</sub> =0V	-	-0.78	-1.0	V

NOTES :

- 1. Pulse width300us, Duty cycle<2%</td>
- 2. Essentially independent of operating temperature typical characteristics.
- 3. The maximum current rating is package limited.
- 4. Repetitive rating, pulse width limited by junction temperature TJ(MAX)=150°C. Ratings are based on low frequency and duty cycles to keep initial TJ =25°C.
- 5. The test condition is L=1mH,  $I_{\text{AS}}{=}8A,\,V_{\text{DD}}{=}25V,\,V_{\text{GS}}{=}10V$
- 6. R<sub>OJA</sub> is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. Mounted on a 1 inch<sup>2</sup> with 2oz.square pad of copper.
- 7. Guaranteed by design, not subject to production testing.







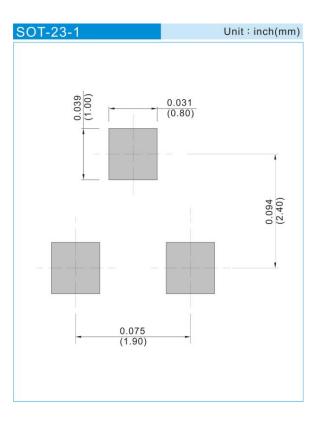




### PART NO PACKING CODE VERSION

Part No Packing Code	Package Type	Packing type	Marking	Version
PJA3461_R1_00001	SOT-23	3K pcs / 7" reel	A61	Halogen free
PJA3461_R2_00001	SOT-23	12K pcs / 13" reel	A61	Halogen free

### MOUNTING PAD LAYOUT







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