



PJD8N10

100V N-Channel MOSFET

Voltage

100 V

Current

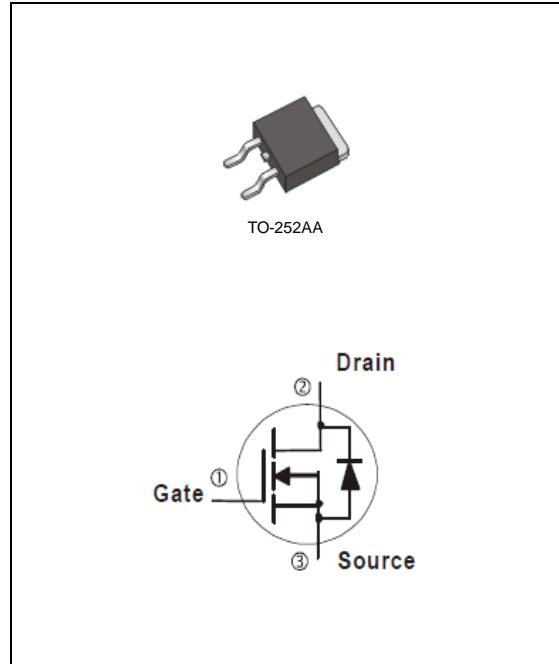
8 A

Features

- $R_{DS(ON)}, V_{GS}@10V, I_D@4.0A < 258m\Omega$
- $R_{DS(ON)}, V_{GS}@6V, I_D@2.0A < 268m\Omega$
- High switching speed
- Improved dv/dt capability
- Low Gate Charge
- Low reverse transfer capacitance
- Lead free in compliance with EU RoHS 2011/65/EU directive.
- Green molding compound as per IEC61249 Std.. (Halogen Free)

Mechanical Data

- Case: TO-252AA Package
- Terminals: Solderable per MIL-STD-750, Method 2026
- Approx. Weight: 0.0104 ounces, 0.297grams



Maximum Ratings and Thermal Characteristics ($T_A=25^\circ\text{C}$ unless otherwise noted)

PARAMETER		SYMBOL	LIMIT	UNITS
Drain-Source Voltage		V_{DS}	100	V
Gate-Source Voltage		V_{GS}	± 20	V
Continuous Drain Current	$T_C=25^\circ\text{C}$	I_D	8	A
	$T_C=100^\circ\text{C}$		5	
Pulsed Drain Current (Note 1)	$T_C=25^\circ\text{C}$	I_{DM}	16	
Power Dissipation	$T_C=25^\circ\text{C}$	P_D	31	W
	$T_C=100^\circ\text{C}$		12	
Continuous Drain Current	$T_A=25^\circ\text{C}$	I_D	2	A
	$T_A=70^\circ\text{C}$		1.6	A
Power Dissipation	$T_A=25^\circ\text{C}$	P_D	2.0	W
Power Dissipation	$T_A=70^\circ\text{C}$		1.3	
Single Pulse Avalanche Energy (Note 6)		E_{AS}	1.8	mJ
Operating Junction and Storage Temperature Range		T_J, T_{STG}	-55~150	$^\circ\text{C}$
Typical Thermal Resistance (Note 4,5)	Junction to Case	$R_{\theta JC}$	4.0	$^\circ\text{C/W}$
	Junction to Ambient	$R_{\theta JA}$	62.5	

- Limited only By Maximum Junction Temperature



PJD8N10

Electrical Characteristics ($T_A=25^\circ\text{C}$ unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNITS
Static						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=250\mu A$	100	-	-	V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	2.0	2.85	3.5	V
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=4A$	-	220	258	m Ω
		$V_{GS}=6V, I_D=2A$	-	220	268	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=100V, V_{GS}=0V$	-	-	1	μA
Gate-Source Leakage Current	I_{GSS}	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	± 100	nA
Dynamic (Note 7)						
Total Gate Charge	Q_g	$V_{DS}=60V, I_D=8A,$ $V_{GS}=10V$ (Note 2,3)	-	6.7	-	nC
Gate-Source Charge	Q_{gs}		-	2.1	-	
Gate-Drain Charge	Q_{gd}		-	1.1	-	
Input Capacitance	C_{iss}	$V_{DS}=25V, V_{GS}=0V,$ $f=1.0\text{MHz}$	-	378	-	pF
Output Capacitance	C_{oss}		-	26	-	
Reverse Transfer Capacitance	C_{rss}		-	20	-	
Turn-On Delay Time	$t_{d(on)}$	$V_{DS}=50V, R_L=6.25\Omega,$ $V_{GS}=10V, R_G=6\Omega$ (Note 2,3)	-	3.8	-	ns
Turn-On Rise Time	t_r		-	26	-	
Turn-Off Delay Time	$t_{d(off)}$		-	8.2	-	
Turn-Off Fall Time	t_f		-	3.7	-	
Drain-Source Diode						
Maximum Continuous Drain-Source Diode Forward Current	I_S	---	-	-	8	A
Diode Forward Voltage	V_{SD}	$I_S=1A, V_{GS}=0V$	-	0.78	1.2	V

NOTES:

1. Pulse width $\leq 300\mu s$, Duty cycle $\leq 2\%$
2. Essentially independent of operating temperature typical characteristics
3. Repetitive rating, pulse width limited by junction temperature $T_J(\text{MAX})=150^\circ\text{C}$. Ratings are based on low frequency and duty cycles to keep initial $T_J=25^\circ\text{C}$.
4. The maximum current rating is package limited
5. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. Mounted on a 1 inch² with 2oz. square pad of copper.
6. The test condition is $L=0.1\text{mH}$, $I_{AS}=6A$, $V_{DD}=25V$, $V_{GS}=10V$
7. Guaranteed by design, not subject to production testing



PJD8N10

TYPICAL CHARACTERISTIC CURVES

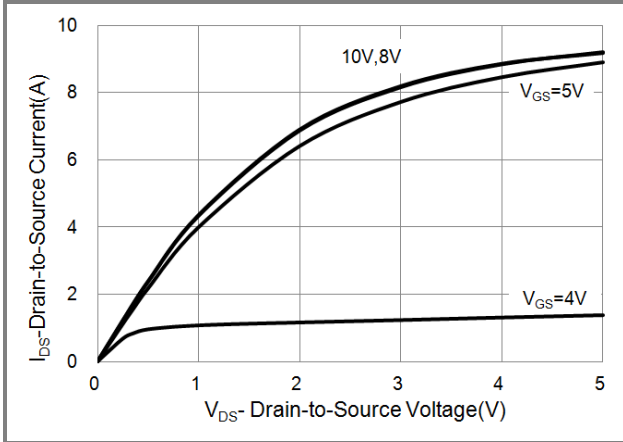


Fig.1 On-Region Characteristics

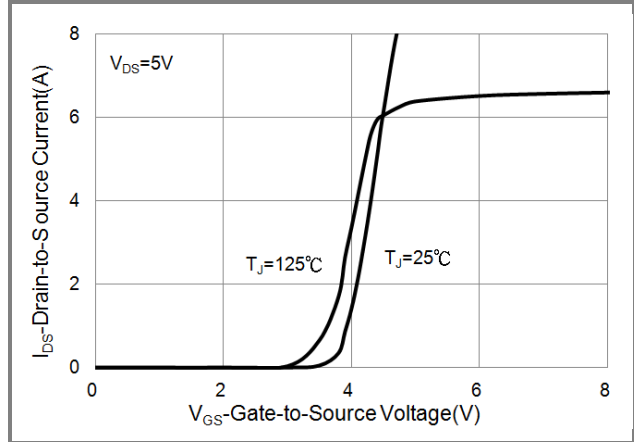


Fig.2 Transfer Characteristics

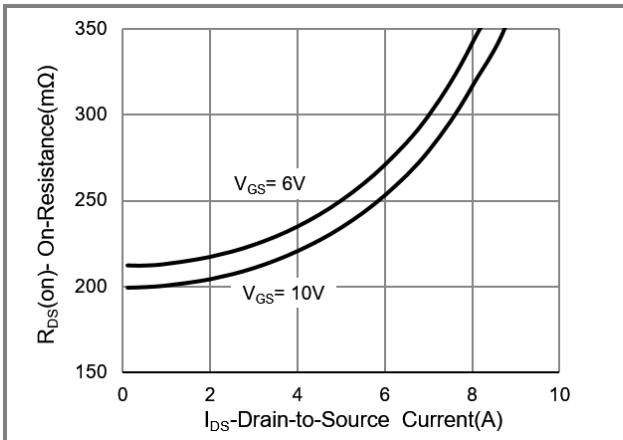


Fig.3 On-Resistance vs. Drain Current

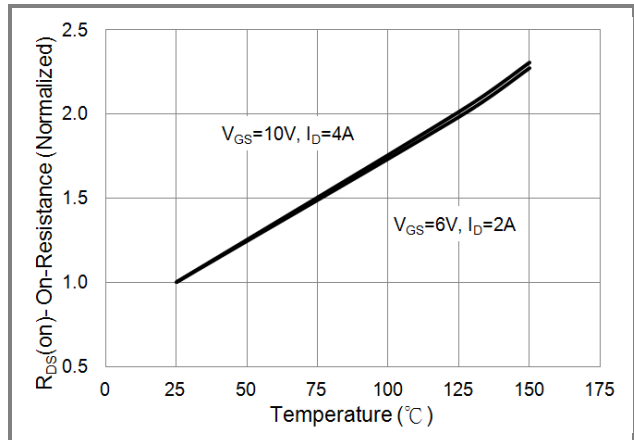


Fig.4 On-Resistance vs. Junction temperature

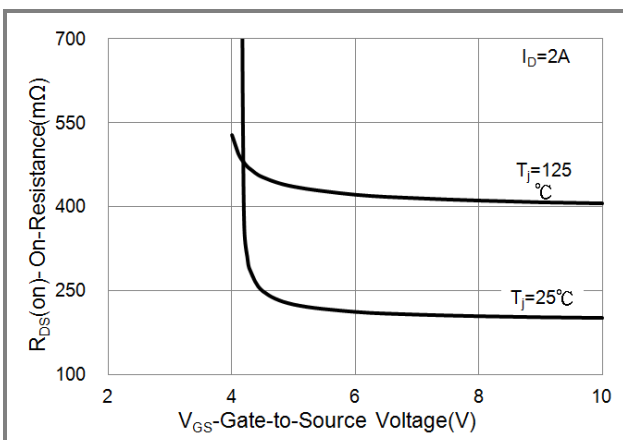


Fig.5 On-Resistance Variation with VGS.

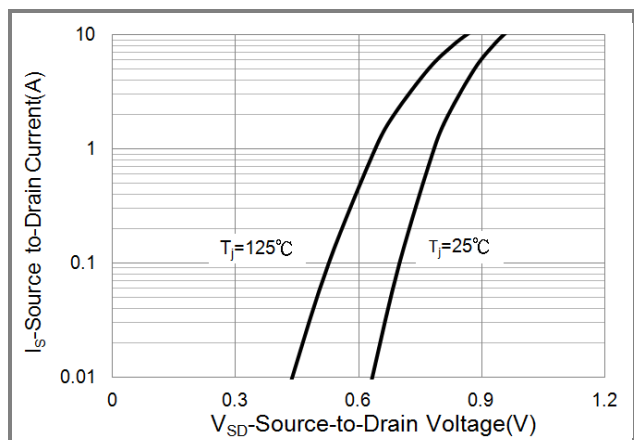


Fig.6 Body Diode Characteristics



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TYPICAL CHARACTERISTIC CURVES

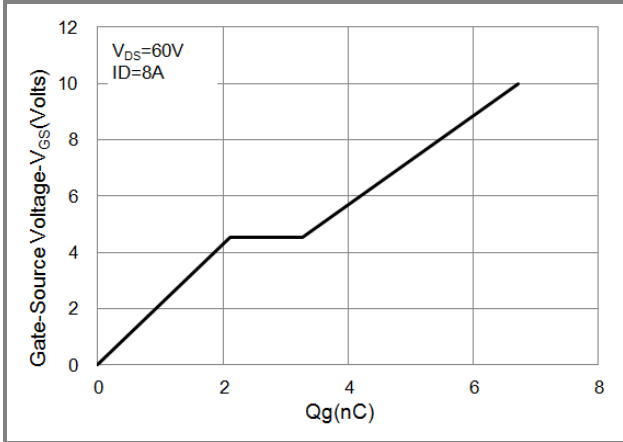


Fig.7 Gate-Charge Characteristics

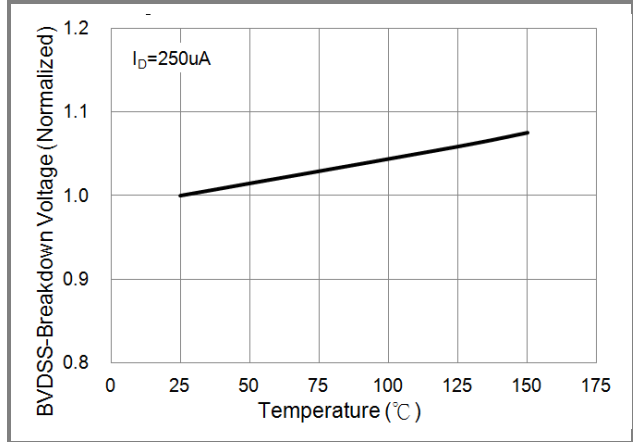


Fig.8 Breakdown Voltage Variation vs. Temperature

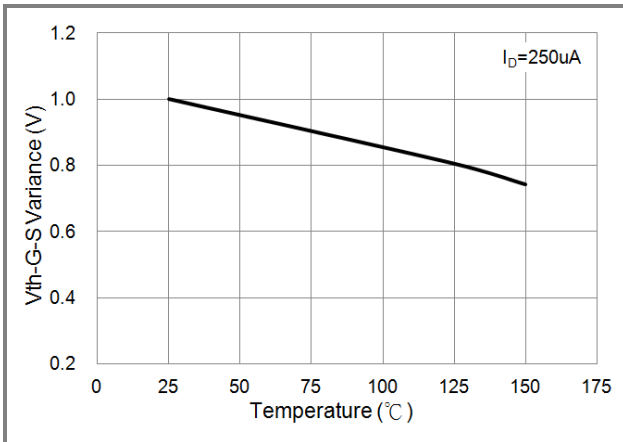


Fig.9 Threshold Voltage Variation with Temperature

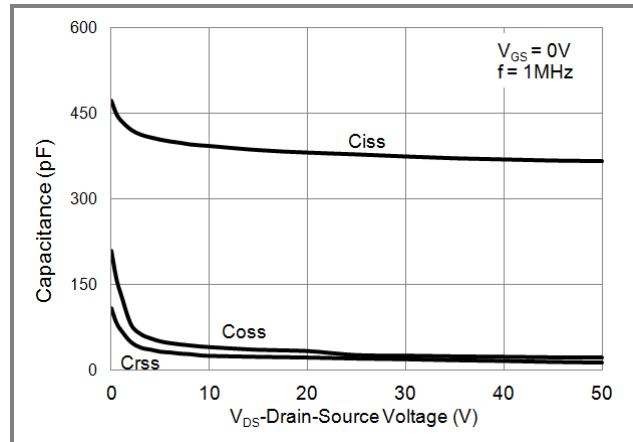


Fig.10 Capacitance vs. Drain-Source Voltage

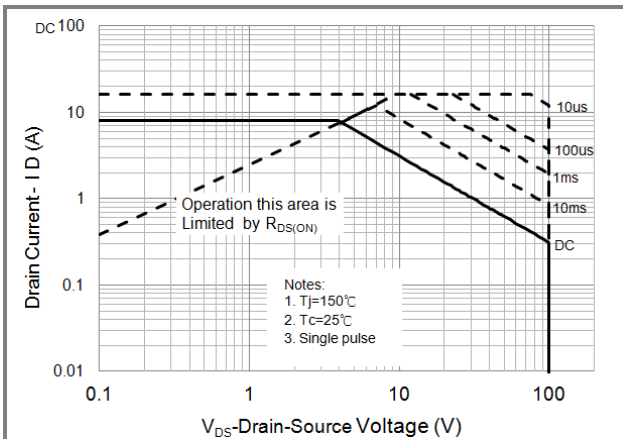


Fig.11 Maximum Safe Operating Area



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TYPICAL CHARACTERISTIC CURVES

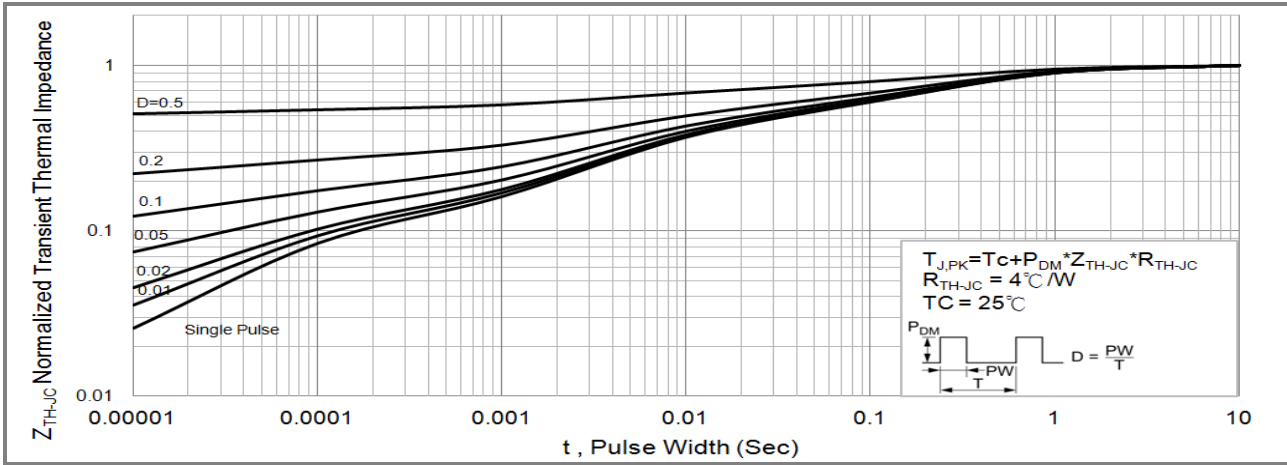
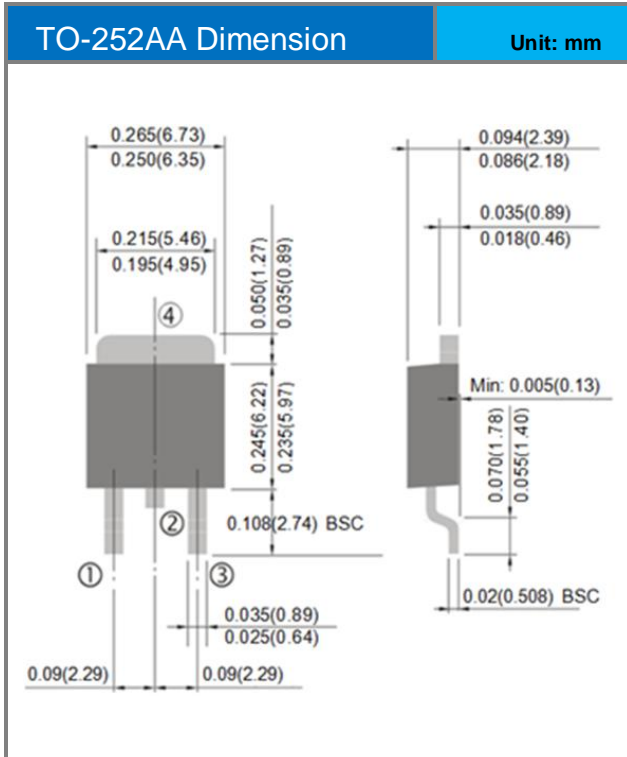


Fig.12 Normalized Thermal Transient Impedance



PJD8N10

Packaging Information



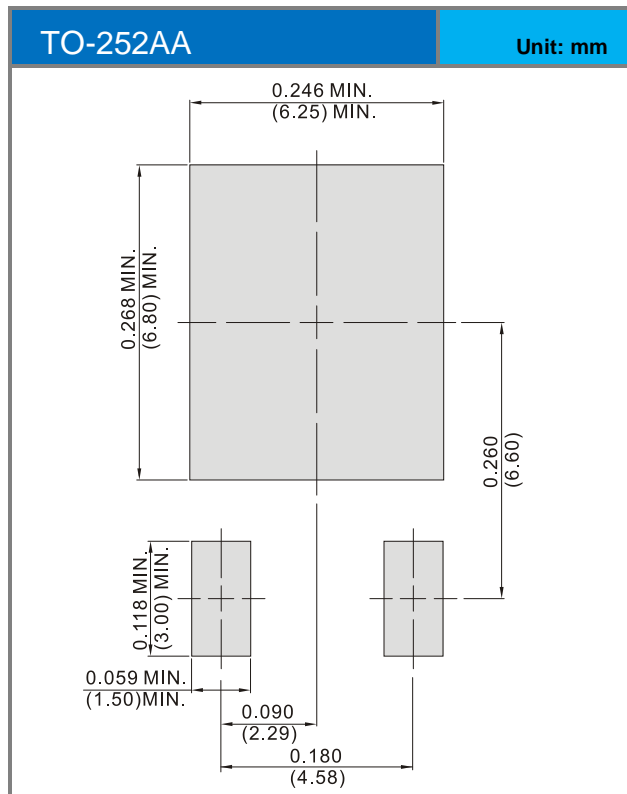


PJD8N10

PART NO PACKING CODE VERSION

Part No Packing Code	Package Type	Packing Type	Marking	Version
PJD8N10_L2_00001	TO-252AA	3,000pcs / 13" reel	D8N10	Halogen free

MOUNTING PAD LAYOUT





PJD8N10

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