



# PJQ4408P-AU

## 30V N-Channel Enhancement Mode MOSFET

<b>Voltage</b>	<b>30 V</b>	<b>Current</b>	<b>42 A</b>
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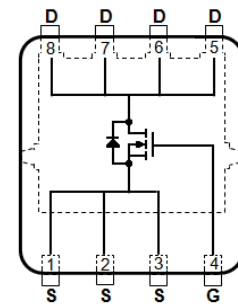
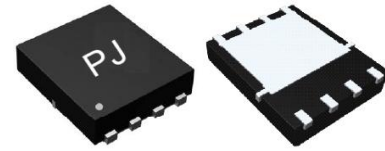
### Features

- $R_{DS(ON)}$ ,  $V_{GS}@10V$ ,  $I_D@16A < 9m\Omega$
- $R_{DS(ON)}$ ,  $V_{GS}@4.5V$ ,  $I_D@8A < 13m\Omega$
- High switching speed
- Improved dv/dt capability
- Low Gate Charge
- Low reverse transfer capacitance
- AEC-Q101 qualified
- Lead free in compliance with EU RoHS 2.0
- Green molding compound as per IEC 61249 Standard

### Mechanical Data

- Case: DFN3333-8L Package
- Terminals: Solderable per MIL-STD-750, Method 2026
- Approx. Weight: 0.001 ounces, 0.03 grams

DFN3333-8L



### Maximum Ratings and Thermal Characteristics ( $T_A=25^\circ\text{C}$ unless otherwise noted)

PARAMETER		SYMBOL	LIMIT	UNITS
Drain-Source Voltage		$V_{DS}$	30	V
Gate-Source Voltage		$V_{GS}$	+20	
Continuous Drain Current	$T_C=25^\circ\text{C}$	$I_D$	42	A
	$T_C=100^\circ\text{C}$		26	
Pulsed Drain Current <sup>(Note 1)</sup>		$I_{DM}$	168	
Power Dissipation	$T_C=25^\circ\text{C}$	$P_D$	35	W
	$T_C=100^\circ\text{C}$		14	
Continuous Drain Current	$T_A=25^\circ\text{C}$	$I_D$	10	A
	$T_A=70^\circ\text{C}$		8	
Power Dissipation		$P_D$	2.0	W
Power Dissipation			$T_A=70^\circ\text{C}$	
Operating Junction and Storage Temperature Range		$T_J, T_{STG}$	-55~150	$^\circ\text{C}$
Typical Thermal Resistance <sup>(Note 4,5)</sup>	Junction to Case	$R_{\theta JC}$	3.6	$^\circ\text{C/W}$
	Junction to Ambient	$R_{\theta JA}$	62.5	

- Limited only By Maximum Junction Temperature



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## Electrical Characteristics ( $T_A=25^\circ\text{C}$ unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNITS
<b>Static</b>						
Drain-Source Breakdown Voltage	$BV_{DSS}$	$V_{GS}=0V, I_D=250\mu A$	30	-	-	V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	1.0	1.7	2.5	
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=16A$	-	6.2	9	m $\Omega$
		$V_{GS}=4.5V, I_D=8A$	-	9.6	13	
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS}=30V, V_{GS}=0V$	-	-	1.0	$\mu A$
Gate-Source Leakage Current	$I_{GSS}$	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	$\pm 100$	nA
<b>Dynamic</b> (Note 6)						
Total Gate Charge	$Q_g$	$V_{DS}=15V, I_D=20A,$ $V_{GS}=4.5V$ (Note 2,3)	-	7.1	-	nC
Gate-Source Charge	$Q_{gs}$		-	3.1	-	
Gate-Drain Charge	$Q_{gd}$		-	2.0	-	
Input Capacitance	$C_{iss}$	$V_{DS}=25V, V_{GS}=0V,$ $f=1.0\text{MHz}$	-	763	-	pF
Output Capacitance	$C_{oss}$		-	132	-	
Reverse Transfer Capacitance	$C_{rss}$		-	81	-	
Turn-On Delay Time	$t_{d(on)}$	$V_{DS}=15V, I_D=15A,$ $V_{GS}=10V, R_G=6\Omega$ (Note 2,3)	-	5.4	-	ns
Turn-On Rise Time	$t_r$		-	86	-	
Turn-Off Delay Time	$t_{d(off)}$		-	20	-	
Turn-Off Fall Time	$t_f$		-	10	-	
<b>Drain-Source Diode</b>						
Maximum Continuous Drain-Source Diode Forward Current	$I_S$	---	-	-	42	A
Diode Forward Voltage	$V_{SD}$	$I_S=1A, V_{GS}=0V$	-	0.7	1	V

**NOTES :**

1. Pulse width  $\leq 300\mu s$ , Duty cycle  $\leq 2\%$
2. Essentially independent of operating temperature typical characteristics
3. Repetitive rating, pulse width limited by junction temperature  $T_{J(MAX)}=150^\circ\text{C}$ . Ratings are based on low frequency and duty cycles to keep initial  $T_J=25^\circ\text{C}$ .
4. The maximum current rating is package limited
5.  $R_{\theta JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. Mounted on a 1 inch<sup>2</sup> with 2oz.square pad of copper
6. Guaranteed by design, not subject to production testing.



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## TYPICAL CHARACTERISTIC CURVES

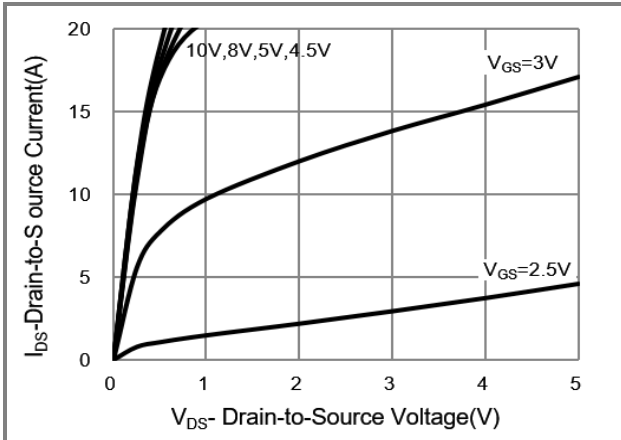


Fig.1 On-Region Characteristics

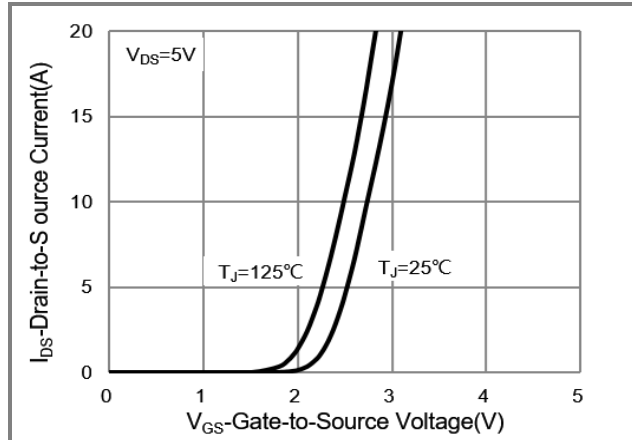


Fig.2 Transfer Characteristics

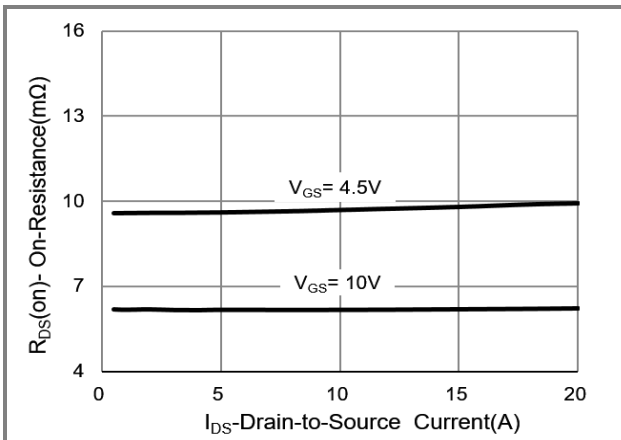


Fig.3 On-Resistance vs. Drain Current

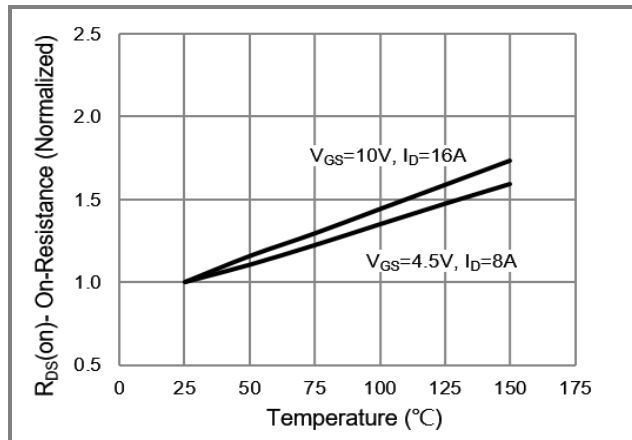


Fig.4 On-Resistance vs. Junction temperature

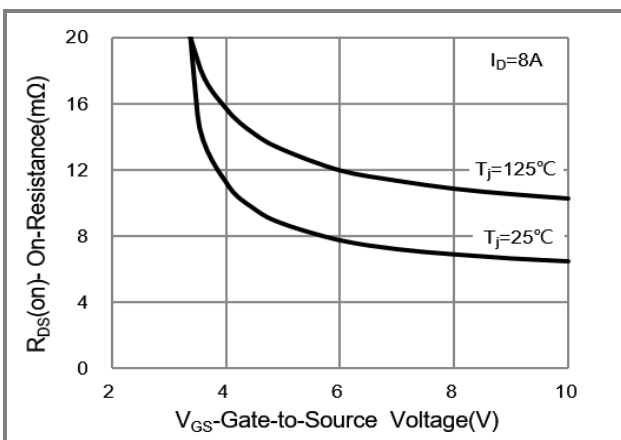


Fig.5 On-Resistance Variation with VGS.

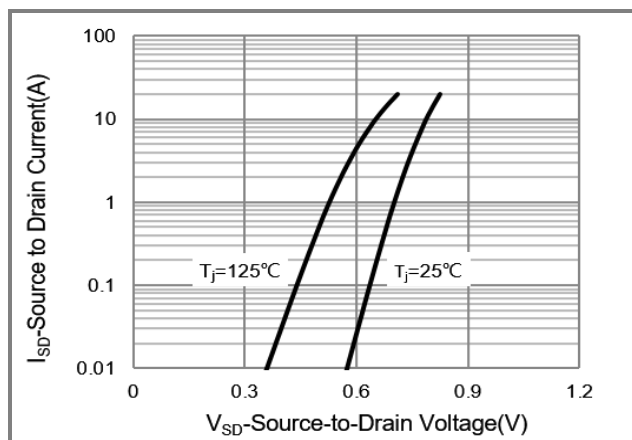


Fig.6 Source-Drain Diode Forward Voltage



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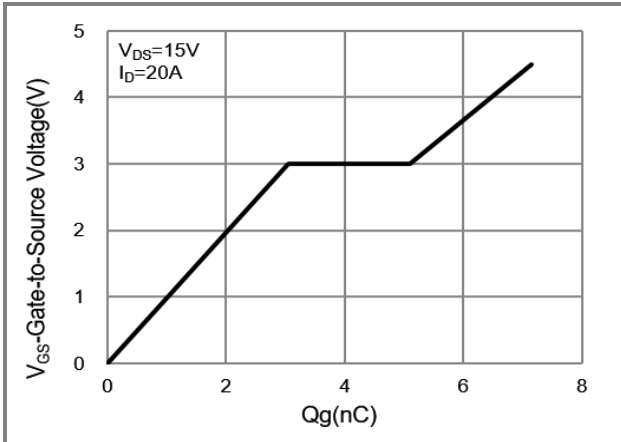


Fig.7 Gate-Charge Characteristics

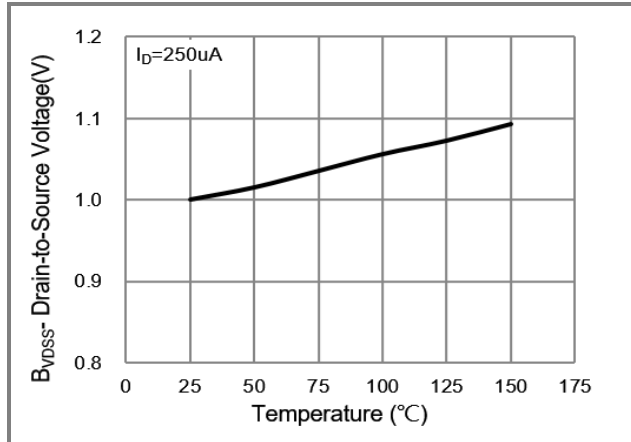


Fig.8 Breakdown Voltage Variation vs. Temperature.

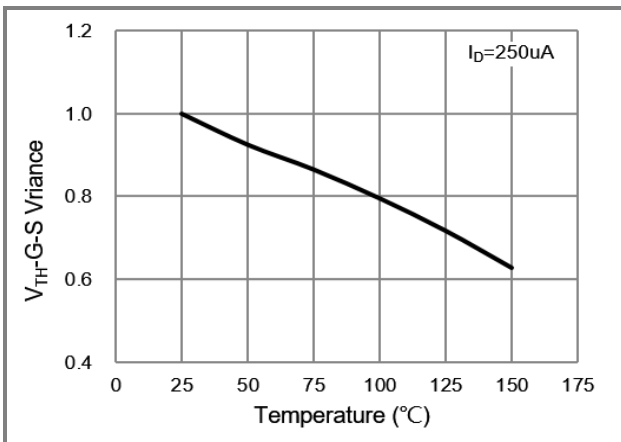


Fig.9 Threshold Voltage Variation with Temperature

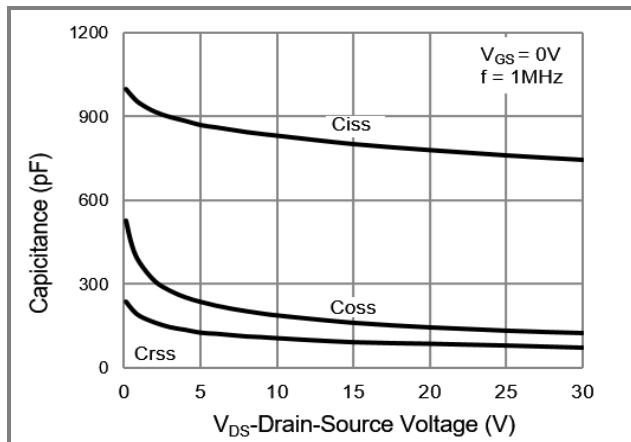


Fig.10 Capacitance vs. Drain-Source Voltage.

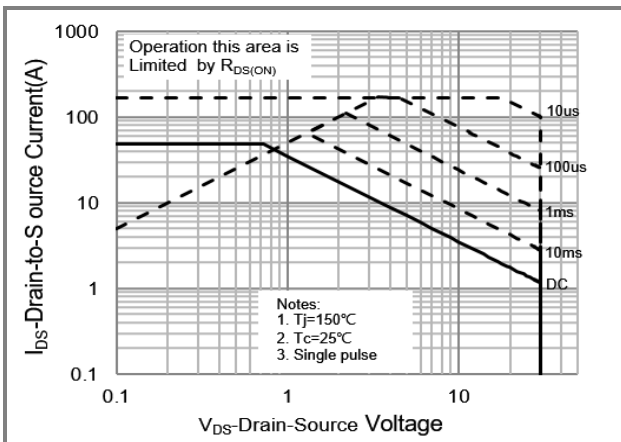


Fig.11 Maximum Safe Operating Area



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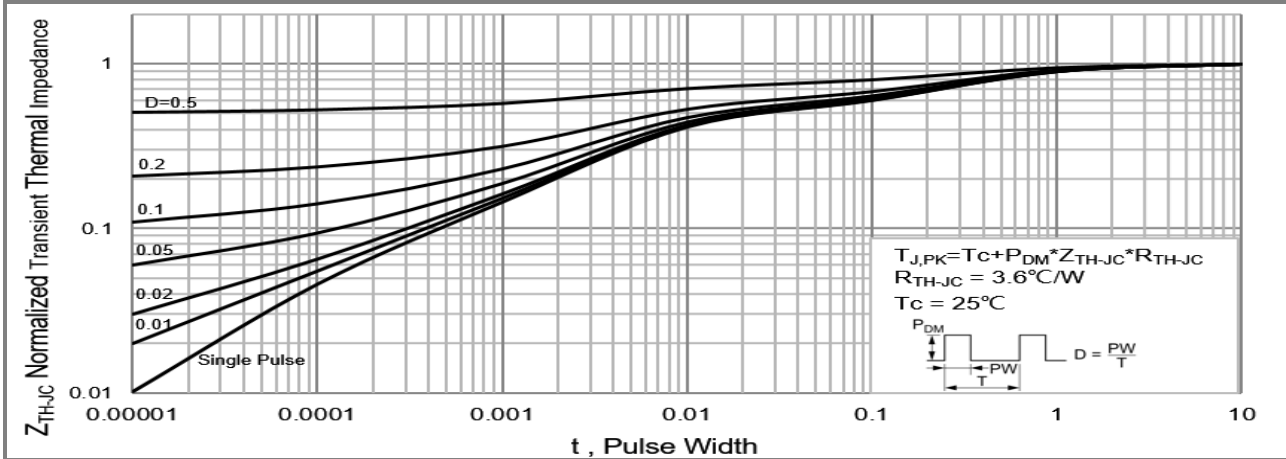


Fig.12 Normalized Transient Thermal Impedance vs. Pulse Width

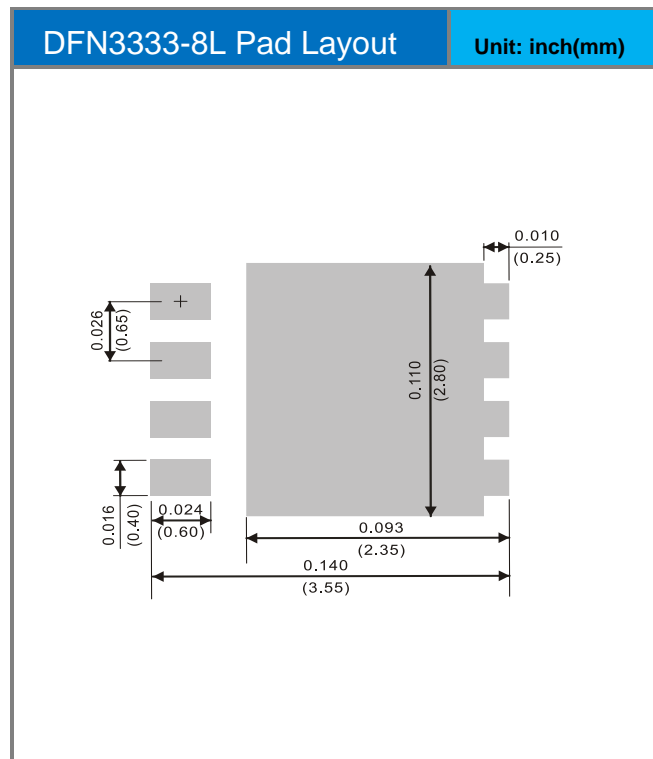
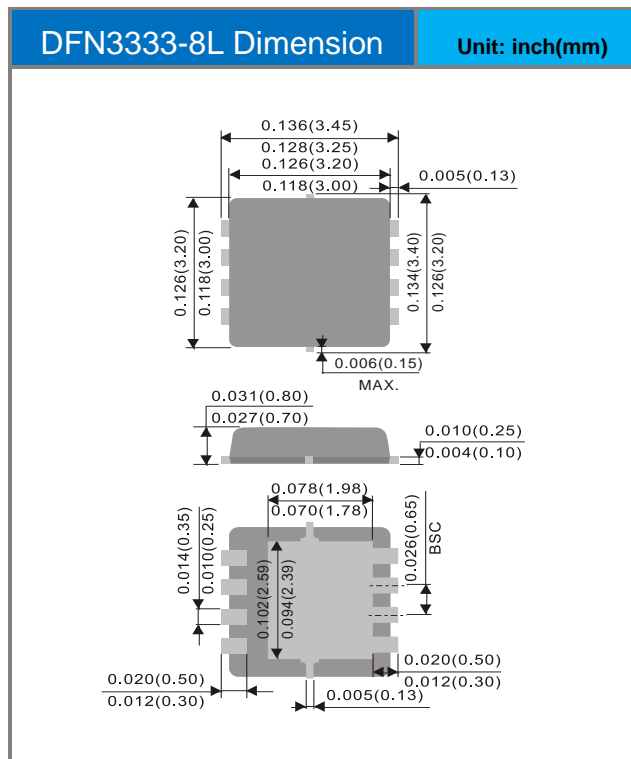


# PJQ4408P-AU

## Part No Packing Code Version

Part No Packing Code	Package Type	Packing Type	Marking	Version
PJQ4408P-AU_R2_000A1	DFN3333-8L	5K pcs / 13" reel	4408	Halogen free

## Packaging Information & Mounting Pad Layout





## PJQ4408P-AU

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