



PJQ5866A

60V N-Channel Enhancement Mode MOSFET

Voltage

60 V

Current

40 A

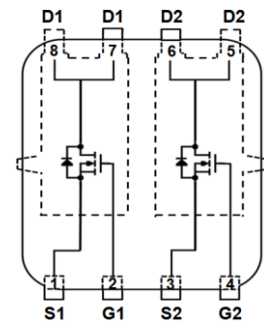
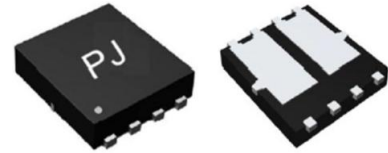
Features

- $R_{DS(ON)}$, $V_{GS}@10V$, $I_D@20A < 17m\Omega$
- $R_{DS(ON)}$, $V_{GS}@4.5V$, $I_D@10A < 20m\Omega$
- High switching speed
- Improved dv/dt capability
- Low reverse transfer capacitance
- Lead free in compliance with EU RoHS 2.0
- Green molding compound as per IEC 61249 standard

Mechanical Data

- Case: DFN5060B-8L Package
- Terminals: Solderable per MIL-STD-750, Method 2026
- Approx. Weight: 0.0035 ounces, 0.092 grams

DFN5060B-8L



Maximum Ratings and Thermal Characteristics ($T_A=25^\circ\text{C}$ unless otherwise noted)

PARAMETER		SYMBOL	LIMIT	UNITS
Drain-Source Voltage		V_{DS}	60	V
Gate-Source Voltage		V_{GS}	± 20	
Continuous Drain Current	$T_C=25^\circ\text{C}$	I_D	40	A
	$T_C=100^\circ\text{C}$		25	
Pulsed Drain Current (Note 1)	$T_C=25^\circ\text{C}$	I_{DM}	160	
Power Dissipation	$T_C=25^\circ\text{C}$	P_D	56	W
	$T_C=100^\circ\text{C}$		22	
Continuous Drain Current	$T_A=25^\circ\text{C}$	I_D	7.0	A
	$T_A=70^\circ\text{C}$		5.5	
Power Dissipation	$T_A=25^\circ\text{C}$	P_D	1.7	W
	$T_A=70^\circ\text{C}$		1.1	
Single Pulse Avalanche Energy (Note 6)		E_{AS}	45	mJ
Operating Junction and Storage Temperature Range		T_J, T_{STG}	-55~150	$^\circ\text{C}$
Typical Thermal Resistance (Note 4,5)	Junction to Case	$R_{\theta JC}$	2.2	$^\circ\text{C/W}$
	Junction to Ambient	$R_{\theta JA}$	73.5	

- Limited only By Maximum Junction Temperature



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Electrical Characteristics ($T_A=25^\circ\text{C}$ unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNITS
Static						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=250\mu A$	60	-	-	V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	1.0	1.7	2.5	
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=20A$	-	13	17	m Ω
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS}=4.5V, I_D=10A$	-	16	20	m Ω
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=60V, V_{GS}=0V$	-	-	1.0	μA
Gate-Source Leakage Current	I_{GSS}	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	± 100	nA
Dynamic (Note 7)						
Total Gate Charge	Q_g	$V_{DS}=30V, I_D=10A,$ $V_{GS}=4.5V$ (Note 1,2)	-	13.5	-	nC
Gate-Source Charge	Q_{gs}		-	4.8	-	
Gate-Drain Charge	Q_{gd}		-	4.9	-	
Input Capacitance	C_{iss}	$V_{DS}=25V, V_{GS}=0V,$ $f=1.0\text{MHz}$	-	1574	-	pF
Output Capacitance	C_{oss}		-	118	-	
Reverse Transfer Capacitance	C_{rss}		-	77	-	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD}=15V, I_D=1A,$ $V_{GS}=10V, R_G=6\Omega$ (Note 1,2)	-	11	-	ns
Turn-On Rise Time	t_r		-	11	-	
Turn-Off Delay Time	$t_{d(off)}$		-	35	-	
Turn-Off Fall Time	t_f		-	8.1	-	
Drain-Source Diode						
Maximum Continuous Drain-Source Diode Forward Current	I_S	---	-	-	40	A
Diode Forward Voltage	V_{SD}	$I_S=1A, V_{GS}=0V$	-	0.68	1	V

NOTES :

1. Pulse width $\leq 300\mu s$, Duty cycle $\leq 2\%$
2. Essentially independent of operating temperature typical characteristics.
3. Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}=150^\circ\text{C}$. Ratings are based on low frequency and duty cycles to keep initial $T_J=25^\circ\text{C}$.
4. The maximum current rating is package limited.
5. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. Mounted on a 1 inch² with 2oz. square pad of copper.
6. The test condition is $L=0.1\text{mH}$, $I_{AS}=30A$, $V_{DD}=25V$, $V_{GS}=10V$, Starting $T_J=25^\circ\text{C}$
7. Guaranteed by design, not subject to production testing.



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TYPICAL CHARACTERISTIC CURVES

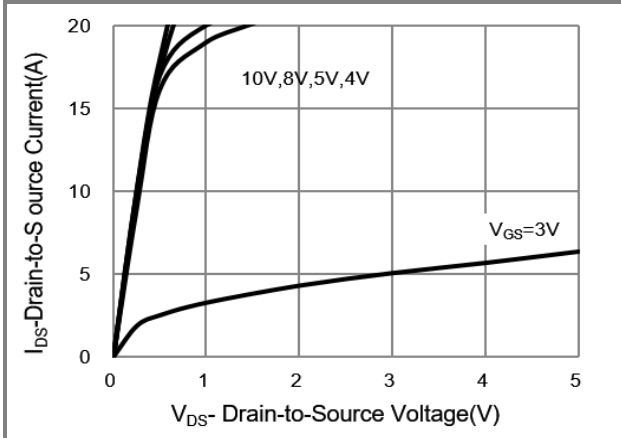


Fig.1 Output Characteristics

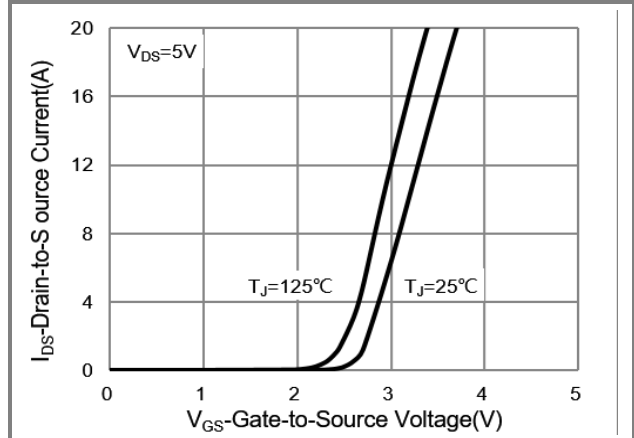


Fig.2 Transfer Characteristics

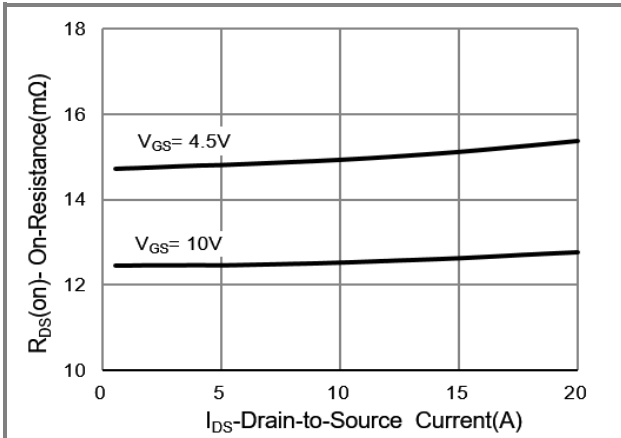


Fig.3 On-Resistance vs. Drain Current

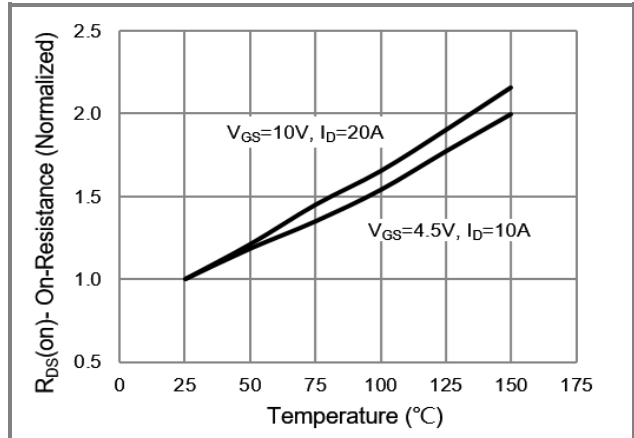


Fig.4 On-Resistance vs. Junction temperature

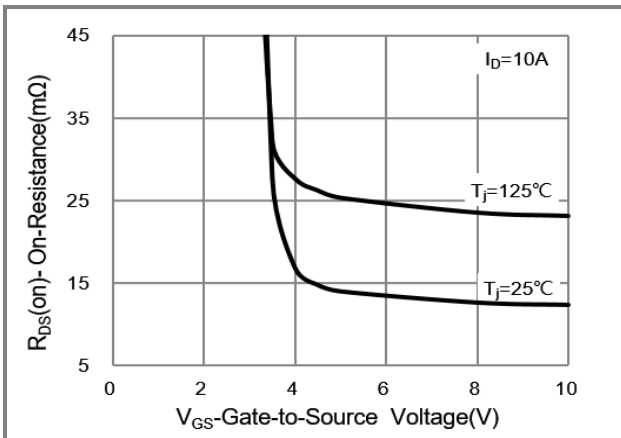


Fig.5 On-Resistance Variation with V_{GS}

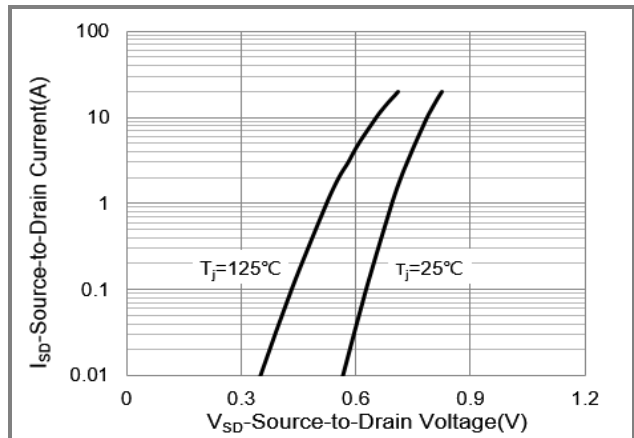


Fig.6 Source-Drain Diode Forward Voltage



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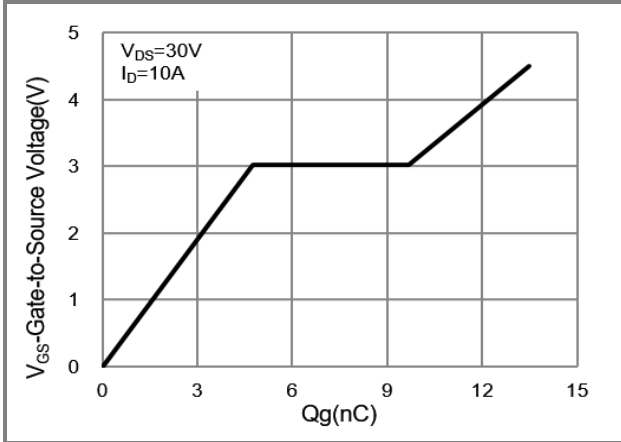


Fig.7 Gate-Charge Characteristics

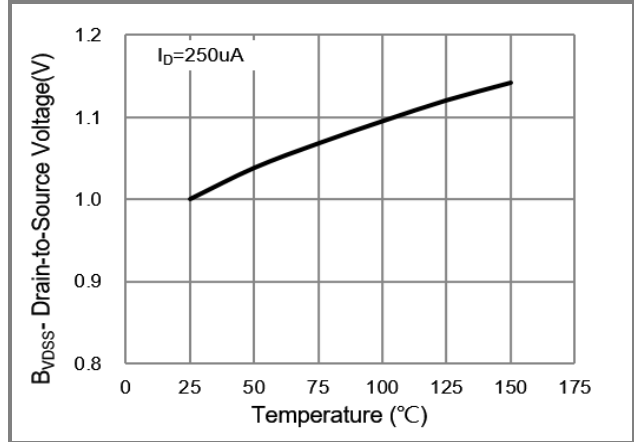


Fig.8 Breakdown Voltage Variation vs. Temperature

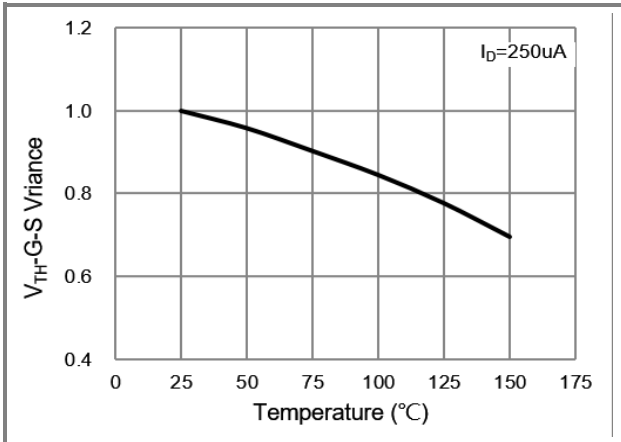


Fig.9 Threshold Voltage Variation with Temperature

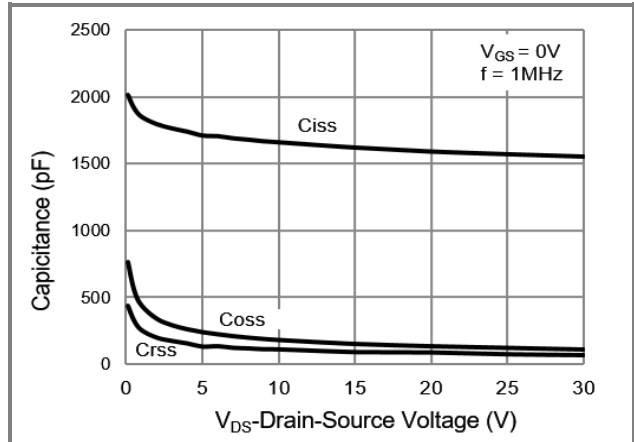


Fig.10 Capacitance vs. Drain-Source Voltage

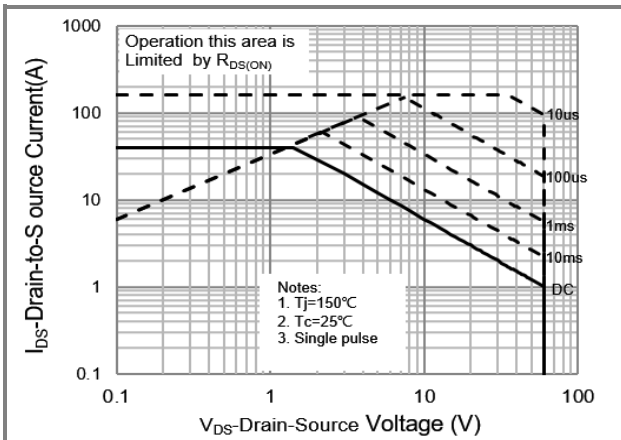


Fig.11 Maximum Safe Operating Area



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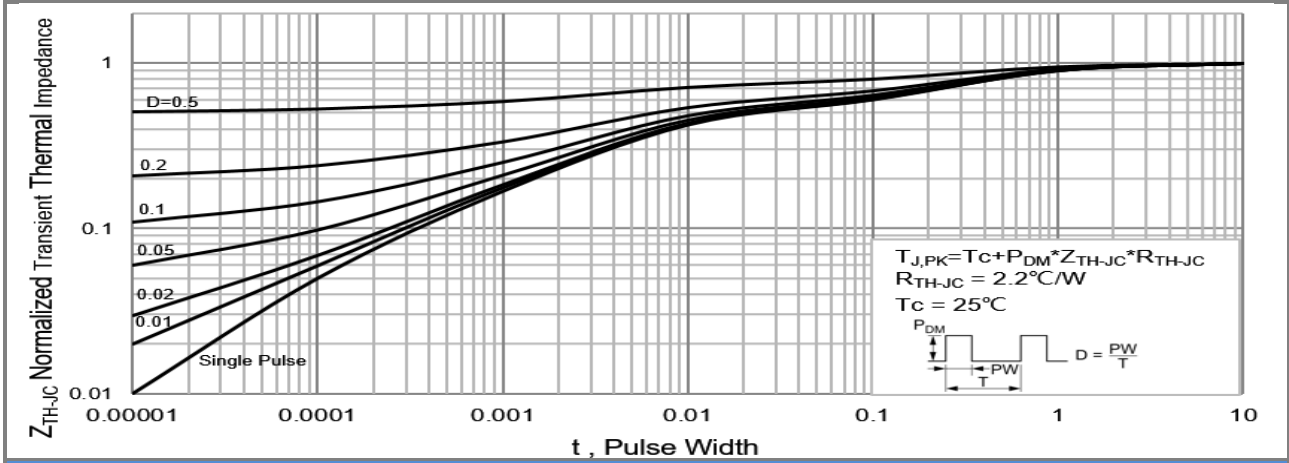


Fig.12 Normalized Transient Thermal Impedance vs. Pulse Width

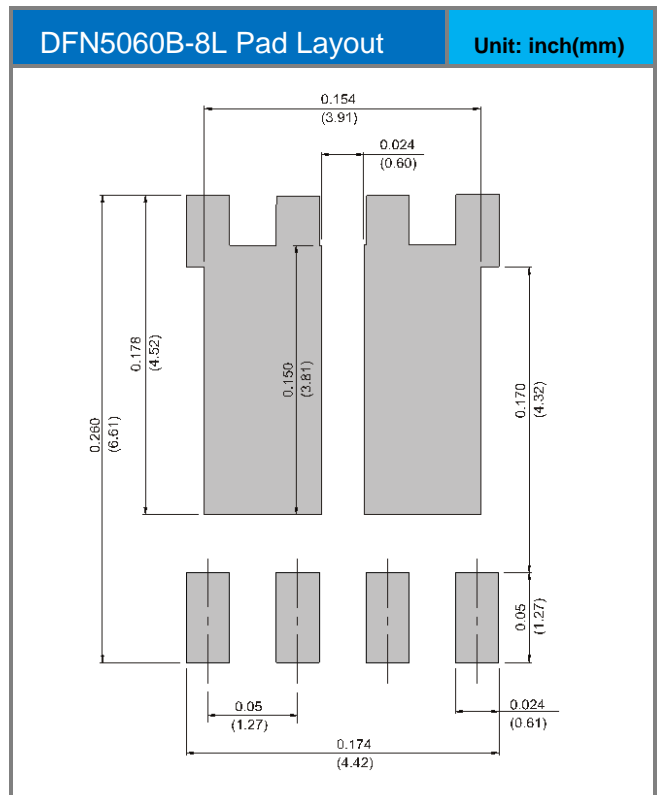
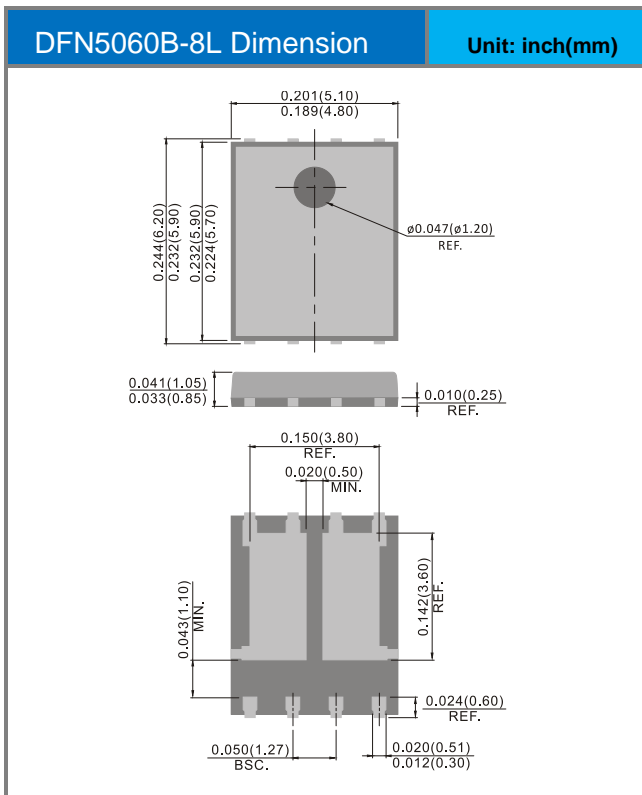


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Part No Packing Code Version

Part No Packing Code	Package Type	Packing Type	Marking	Version
PJQ5866A_R2_00001	DFN5060B-8L	3000pcs / 13" reel	Q5866A	Halogen free

Packaging Information & Mounting Pad Layout





PJQ5866A

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