ΡΛΝ	JIT
	SEMI
	CONDUCTOR

## 60V N-Channel Enhancement Mode MOSFET

Voltage

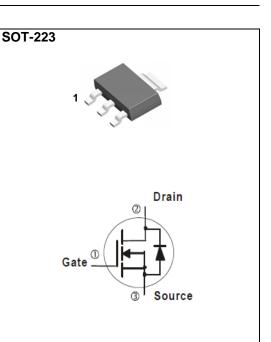
60 V Current

### Features

- $R_{DS(ON)}$ ,  $V_{GS}@10V$ ,  $I_D@3A<100m\Omega$
- $R_{DS(ON)}$ ,  $V_{GS}$ @4.5V,  $I_D$ @2A<110m $\Omega$
- Advanced Trench Process Technology
- High density cell design for ultra low on-resistance
- AEC-Q101 qualified
- Lead free in compliance with EU RoHS 2.0
- Green molding compound as per IEC 61249 standard

### **Mechanical Data**

- Case : SOT-223 Package
- Terminals : Solderable per MIL-STD-750, Method 2026
- Approx. Weight : 0.043 ounces, 0.123grams



### **Maximum Ratings and Thermal Characteristics** ( $T_A=25^{\circ}C$ unless otherwise noted)

4 A

PARAMETER		SYMBOL	LIMIT	UNITS	
Drain-Source Voltage		V <sub>DS</sub>	60	V	
Gate-Source Voltage		$V_{GS}$	<u>+</u> 20		
Continuous Drain Current (Note 4)	T <sub>A</sub> =25°C	- I <sub>D</sub>	4		
	T <sub>A</sub> =70°C		3.2	А	
Pulsed Drain Current (Note 1)		I <sub>DM</sub>	8	1	
Power Dissipation	T <sub>A</sub> =25°C	P <sub>D</sub>	3.7	W	
	T <sub>A</sub> =70°C		2.6		
Operating Junction and Storage Te	emperature Range	T <sub>J</sub> ,T <sub>STG</sub>	-55~175	°C	
Typical Thermal Resistance - Junction to Ambient <sup>(Note 4,5)</sup>		R <sub>θJA</sub>	40.3	°C/W	

• Limited only By Maximum Junction Temperature

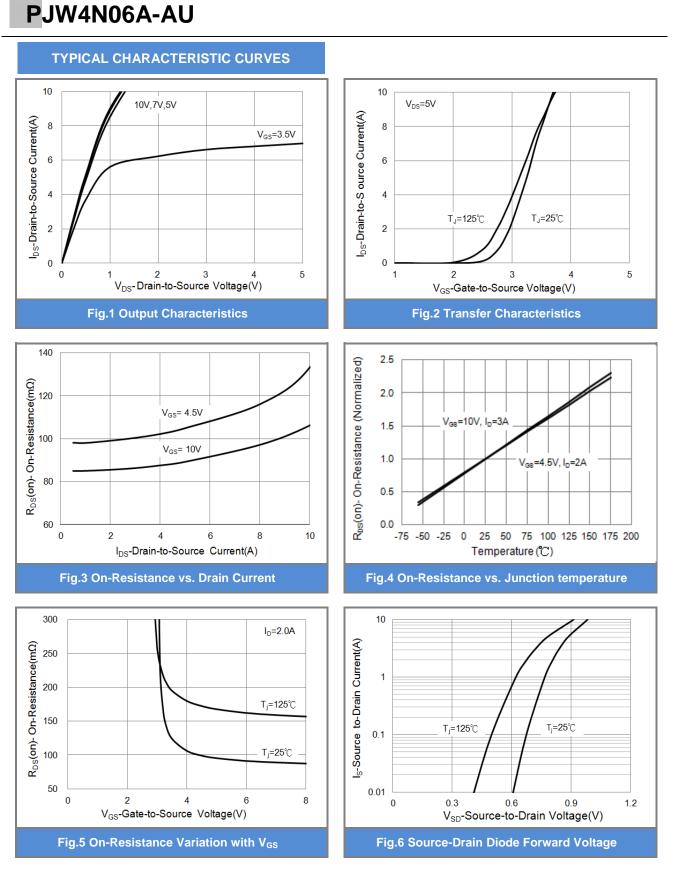


## **Electrical Characteristics** ( $T_A=25^{\circ}C$ unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNITS
Static			·			
Drain-Source Breakdown Voltage	$BV_{DSS}$	V <sub>GS</sub> =0V, I <sub>D</sub> =250uA	60	-	-	V
Gate Threshold Voltage	V <sub>GS(th)</sub>	$V_{DS}=V_{GS}$ , $I_{D}=250$ uA	1	1.86	2.5	
Drain-Source On-State Resistance	_	V <sub>GS</sub> =10V, I <sub>D</sub> =3A	-	85	100	mΩ
	R <sub>DS(on)</sub>	V <sub>GS</sub> =4.5V, I <sub>D</sub> =2A	-	95	110	
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =48V, V <sub>GS</sub> =0V	-	-	1	uA
Gate-Source Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> = <u>+</u> 20V, V <sub>DS</sub> =0V	-	-	<u>+</u> 100	nA
Dynamic (Note 6)						
Total Gate Charge	Qg	V <sub>DS</sub> =48V, I <sub>D</sub> =3A, V <sub>GS</sub> =4.5V <sup>(Note 2,3)</sup>	-	5.1	-	
Gate-Source Charge	Q <sub>gs</sub>		-	1.2	-	nC
Gate-Drain Charge	Q <sub>gd</sub>		-	1.9	-	
Input Capacitance	Ciss	· V <sub>DS</sub> =15V, V <sub>GS</sub> =0V, · f=1MHZ	-	509	-	pF
Output Capacitance	Coss		-	39	-	
Reverse Transfer Capacitance	Crss		-	26	-	
Turn-On Delay Time	td <sub>(on)</sub>		-	1.6	-	
Turn-On Rise Time	tr	$V_{DD}=30V, I_{D}=3A,$ $V_{GS}=10V,$	-	7.3	-	-
Turn-Off Delay Time	td <sub>(off)</sub>		-	25	-	ns
Turn-Off Fall Time	t <sub>f</sub>	$R_{G}=3.3\Omega^{(Note 2,3)}$	-	14	-	
Drain-Source Diode						
Maximum Continuous Drain-Source					4	•
Diode Forward Current	I <sub>S</sub>		-	-	4	A
Diode Forward Voltage	$V_{SD}$	I <sub>S</sub> =1A, V <sub>GS</sub> =0V	-	0.8	1.2	V

NOTES :

- 1. Pulse width</br>
- 2. Essentially independent of operating temperature typical characteristics.
- Repetitive rating, pulse width limited by junction temperature T<sub>J(MAX)</sub>=150°C. Ratings are based on low frequency and duty cycles to keep initial T<sub>J</sub> =25°C.
- 4. The maximum current rating is package limited.
- 5.  $R_{\Theta JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. Mounted on a 1 inch<sup>2</sup> with 2oz.square pad of copper.
- 6. Guaranteed by design, not subject to production testing.



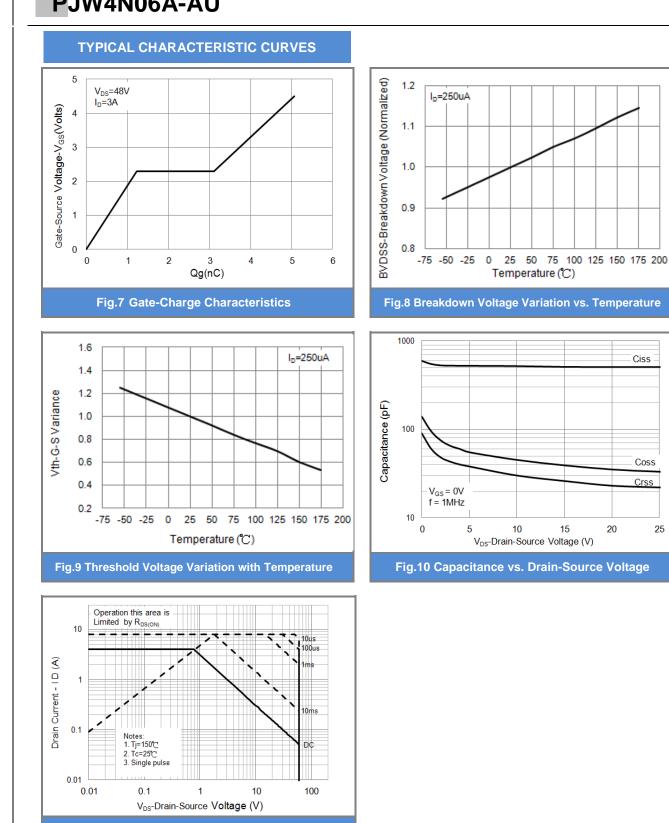
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April 2,2019-REV.02

Fig.11 Maximum Safe Operating Area

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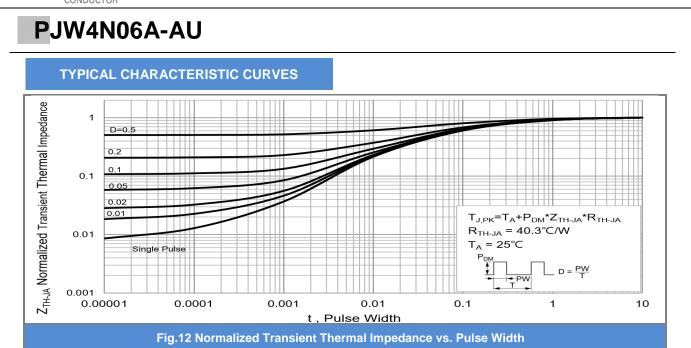
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# PJW4N06A-AU







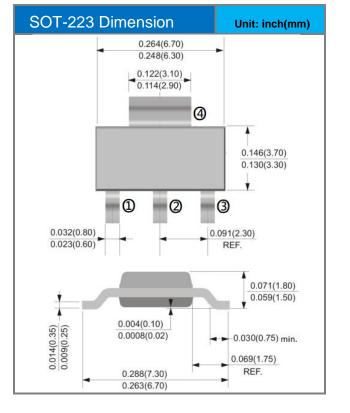


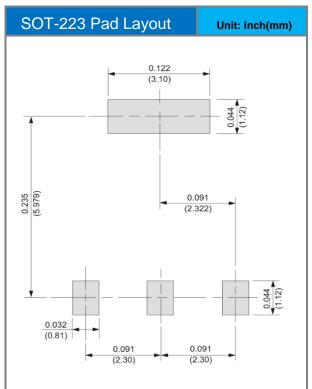


### Part No Packing Code Version

Part No Packing Code	Package Type	Packing Type Marking		Version
PJW4N06A-AU_R2_000A1	SOT-223	2,500pcs / 13" reel	W4N06A	Halogen free

## Packaging Information & Mounting Pad Layout







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