Security Level: 3

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Originator: FAE/Zhiqiang Yang		

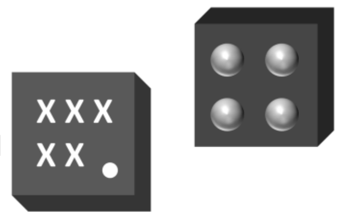
REVISION RECORD

Rev.	Date	Originator	Change Description
A	21/02/2023	Zhiqiang Yang	Preliminary Version

3-Axis Single Chip Magnetic Sensor

QMC6309

The QMC6309 is a three-axis magnetic sensor, which integrates magnetic sensors and signal condition ASIC into one silicon chip. This wafer level chip scale package (WLCSP) is targeted for applications such as e-compass, map rotation, gaming and personal navigation in mobile and wearable devices.



The QMC6309 is based on state-of-the-art, high resolution, magneto-resistive technology. Along with the custom-designed 16-bit ADC ASIC, it offers the advantages of low noise, high accuracy, low power consumption, offset cancellation and temperature compensations. QMC6309 enables 1° to 2° compass heading accuracy. The I²C serial bus allows for easy interface.

The QMC6309 is in a 0.8x0.8x0.5mm^3 surface mount 4-pin WLCSP package.

FEATURES

- 3-Axis Magneto-Resistive Sensors in a 0.8x0.8x0.5 mm^3 WLCSP, Guaranteed to Operate Over an Extended Temperature Range of -40 °C to +85 °C.
- 16 Bit ADC With Low Noise AMR Sensors Achieves 2 milli-Gauss Field Resolution
- Wide Magnetic Field Range (±32 Gauss)
- Temperature Compensated Data Output
- Built-In Self-Test
- Wide Range Operation Voltage (2.5V to 3.6V) and low Power Consumption less 10uA at 1Hz ODR
- Lead Free Package Construction
- Software and Algorithm Support Available

BENEFIT

- Small Size for Highly Integrated Products. Signals Have Been Digitized and Calibrated.
- Enables 1° To 2° Degree Compass Heading Accuracy, Allows for Pedestrian Navigation and LBS Applications
- Maximizes Sensor's Full Dynamic Range and Resolution
- Automatically Maintains Sensor's Sensitivity Under Wide Operating Temperature Range
- Enables Low-Cost Functionality Test After Assembly in Production
- Compatible with Battery Powered Applications
- RoHS Compliance
- Compassing Heading, Hard Iron, Soft Iron, and Auto Calibration Libraries Available

CONTENTS

1 INTERNAL SCHEMATIC DIAGRAM

1.1 Internal Schematic Diagram

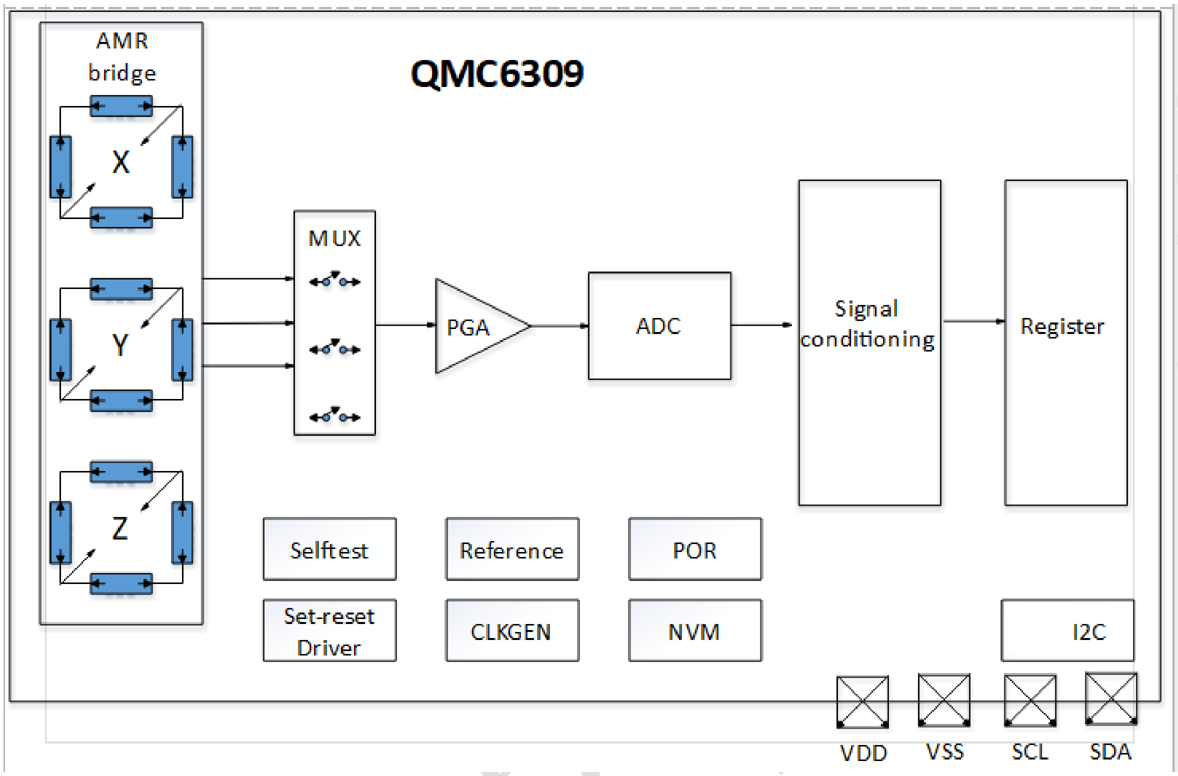


Figure 1. Block Diagram

1.2 Block Functions

Table 1. Block Functions

Block	Function
AMR bridge	3-axis magnetic sensor
MUX	Multiplexer for sensor channels
PGA	Programmable gain amplifier for sensor signals
ADC	Analog-to-Digital converter
Signal conditioning	Digital blocks for magnetic signal calibration and compensations
I2C	Interface logic data I/O
NVM	Non-volatile memory
Register	Internal register
Selftest	Internal driver to generate self-test stimulus
Set-reset Driver	Internal driver to initialize magnetic sensor
Reference	Voltage/current reference for internal biasing
CLKGEN.	Internal oscillator for internal operation
POR	Power on reset

2 SPECIFICATIONS AND I/O CHARACTERISTICS

2.1 Product Specifications

Table 2. Specifications (Tested and specified at 25°C, VDD=3.3V, except stated otherwise.)

Parameter	Conditions		Min	Typ	Max	Unit
Supply Voltage	VDD		2.5	3.3	3.6	V
Suspend Mode Current	Total Current on VDD			1.8		μA
Normal Mode Current [1]	Low power and high power mode	ODR=1Hz		6/10		uA
		ODR=10Hz		30/100		uA
		ODR=50Hz		150/500		uA
		ODR=100Hz		300/1000		uA
		ODR=200Hz		600/2000		uA
Continuous Mode Current[3]	OSR1=1	Maximum ODR: 1500Hz		3500		uA
Sensor Field Range	Full Scale		-32		32	Gauss
Sensitivity[2],[3]	±32G		-5		5	%
	Field Range = ±32G			1000		LSB/G
	Field Range = ±16G			2000		LSB/G
	Field Range = ±8G			4000		LSB/G
Linearity[3]	Field Range = ±32G Happlied= ±16G			0.6		%FS
Hysteresis[3]	3 sweeps across ±32G			0.03		%FS
Offset[4]			-1		1	Gauss
Sensitivity Tempco[3]	Ta = -40°C~85°C				±0.05	%/°C
Digital Resolution	Field Range = ±32G			1.0		mGauss
Field Resolution[3]	OSR=8,8			2.5		mGauss
	OSR=8,4			3.5		mGauss
	OSR=8,2			5.0		mGauss
	OSR=8,1			7.0		mGauss
X-Y-Z Orthogonality[3]	Sensitivity Directions			90±1	90±3	Degree
Operating Temperature			-40		85	°C
ESD	HBM		2000			V
	CDM		500			V

Notes:
1. The Normal Mode Current differs at different OSR1 setting. The value of low power mode is measured at OSR1=1 setting， and the value of high power mode is measured at OSR1=8.
2. Sensitivity is calibrated at zero field; it is slightly decreased at high fields.
3. Based on 3lots characterization results at continuous mode
4. Null Field Output

2.2 Absolute Maximum Ratings

Table 3. Absolute Maximum Ratings (VSS=0)

Parameter	MIN.	MAX.	Unit
VDD	-0.5	5	V
Storage Temperature	-40	125	°C
Exposed to Magnetic Field (all directions)		10000	Gauss
Reflow Classification	MSL 1, 260 °C Peak Temperature		

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes

2.3 I/O Characteristics

Table 4. I/O Characteristics (VDD =VDDIO= 3.3V，Tested at 25°C)

Parameter(Units)	Symbol	Min.	Typ.	Max.	Unit
High Level Input Voltage	V_{IH}	0.7*VDDIO			V
Low Level Input Voltage	V_{IL}	-0.5		0.3*VDDIO	V
Hysteresis of Schmitt Trigger Input [1]	V_{HYS}	0.1*VDDIO			V
Input Leakage, All Inputs	I_{IL}	-10		10	uA
High Level output Voltage [2]	V_{OH}	0.8*VDDIO			V
Low Level output Voltage [3]	V_{OL}			0.2*VDDIO	V

Notes:
1. Schmitt trigger input (reference value for design).
2. Output is Push-Pull.
3. Output is Open-Drain and Push-Pull. Connect a pull-up resistor externally in Open-Drain mode.

3 PACKAGE PIN CONFIGURATIONS

3.1 Package 3-D View

Arrow indicates direction of magnetic field that generates a positive output reading in normal measurement configuration.

< QMC6309 >

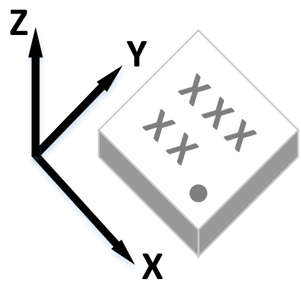


Figure 2. Package 3-D View

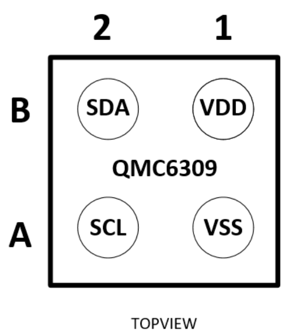


Figure 3. Package Top View

Table 5. Pin Configurations

PIN No.	PIN NAME	I/O	TYPE	Function
A1	VSS	-	-	Ground
A2	SCL	I	CMOS	I2C serial clock line
B1	VDD	-	Power	Supply Voltage
B2	SDA	I/O	CMOS	I2C serial data line

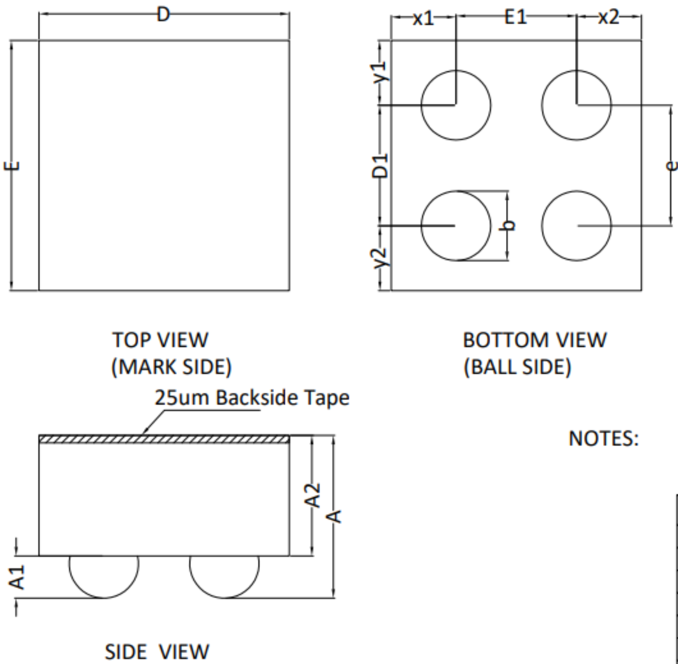
3.2 Package Outlines

3.2.1 Package Type

WLCSP

3.2.2 Package Size

0.8mm (Length)*0.8mm (Width)*0.5mm (Height)



NOTES:

COMMON DIMENSIONS
(UNITS OF MEASURE=MILLMETER)

SYMBOL	MIN	NOM	MAX
A	0.500	0.540	0.580
A1	0.110	0.140	0.170
A2	0.375	0.400	0.425
D	0.770	0.790	0.810
E	0.770	0.790	0.810
D1		0.400BSC	
E1		0.400BSC	
e		0.400BSC	
b	0.200	0.230	0.260
x1		0.215REF	
x2		0.215REF	
y1		0.215REF	
y2		0.215REF	

Figure 4. Package Size

3.2.3 Marking

Tracking code: $X_1X_2X_3X_4X_5$

$X_1X_2X_3X_4$= Package Lot
X_5= Supplier code
●= Pin1 Identifier

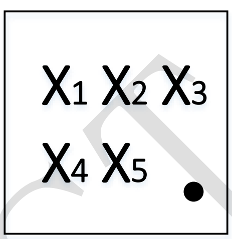


Figure 5. Chip Marking

4 EXTERNAL CONNECTION

4.1 Recommended External Connection

4.1.1 I2C Bus interface

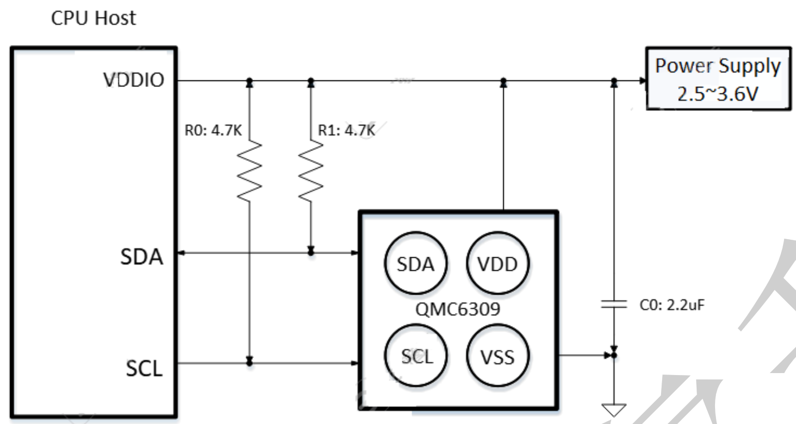


Figure 6. When VDDIO is the same as VDD

4.2 Mounting Considerations

The following is the recommend printed circuit board (PCB) footprint for the QMC6309. Due to the fine pitch of the pads, the footprint should be properly centered in the PCB.

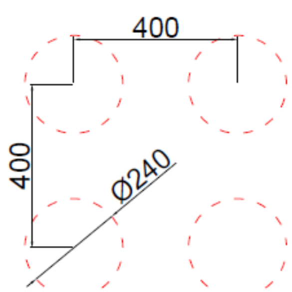


Figure 7. QMC6309 PCB footprint

4.3 Layout Considerations

Besides keeping all components that may contain ferrous materials (nickel, etc.) away from the sensor on both sides of the PCB, it is also recommended that there is no conducting copper line under/near the sensor in any of the PCB layers.

4.3.1 Solder Paste

A 4-mil stencil and 100% paste coverage is recommended for the electrical contact pads.

4.3.2 Reflow Assembly

This device is classified as MSL 1 with 260°C peak reflow temperature. Reference IPC/JEDEC standard J-STD-033 for additional information.

No special reflow profile is required for QMC6309, which is compatible with lead eutectic and lead-free solder paste reflow profiles. QST recommends adopting solder paste manufacturer's guidelines. Hand soldering is not recommended.

4.3.3 External Capacitors

The external capacitors C0 should be ceramic type with low ESR characteristics. The exact ESR value is not critical, but values less than 200 milli-ohms are recommended. Reservoir capacitor C0 is nominally 2.2 μF in capacitance. Low ESR characteristics may not be in many small SMT ceramic capacitors (0402), so be prepared to up-size the capacitors (0201) to gain low ESR characteristics.

5 BASIC DEVICE OPERATION

5.1 Anisotropic Magneto-Resistive Sensors

QMC6309 magneto-resistive sensor circuit consists of tri-axial sensors and application specific support circuits to measure magnetic fields. With a DC power supply is applied to the sensor two terminals, the sensor converts any incident magnetic field in the sensitive axis directions to a differential voltage output.

The device has an offset cancellation function to eliminate sensor and ASIC offsets. It also applies a self-aligned magnetic field to restore magnetic state before each measurement to ensure high accuracy. Because of these features, the QMC6309 doesn't need to calibrate every time in most of application situations. It may need to be calibrated once in a new system or a system changes a new battery.

5.2 Power Management

There are only one power supply pins to the device. VDD provides power for all the internal analog and digital functional blocks and I/O.

When the device is powered on, all registers are reset by POR (Power-On-Reset), then the device transits to the suspend mode and waits for further commands.

Table 6 provides references for two power states.

Table 6: Power States

Power State	VDD	Power State description
1	0V	Device Off, No Power Consumption
2	2.5V~3.6V	Device On, Enters Suspend Mode after POR, waiting for further commands

5.3 Power On/Off Time

After the device is powered on, some time periods are required for the device fully functional. The external power supply requires a time period for voltage to ramp up (PSUP), it is less than~10 milli-second. However, it isn't controlled by the device. The Power-On-Reset time period (PORT) includes time to reset all the logics, load values in NVM to proper registers, enter the standby mode and get ready for analogy measurements. The power on/off time related to the device is in Table 7.

Table 7. Time Required for Power On/Off

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Power supply rise time[1]	PSUP	Time Period that VDD changes from 0.2V to Operating Voltage			10	mS
POR Completion Time[1]	PORT	Time Period After VDD at Operating Voltage to Ready for I²C Command[2]			3	mS
Power off Voltage[1]	SDV	Voltage that Device Considered to be Power Down[2].			0.2	V
Power on Interval[1]	PINT	Time Period Required for Voltage Lower than SDV to Enable Next POR[2]	100			uS

Notes:
1. Reference value for design

2. When POR circuit detects the rise of VDD voltage, it resets internal circuits and initializes the registers. After reset, QMC6309 transits to Suspend Mode.

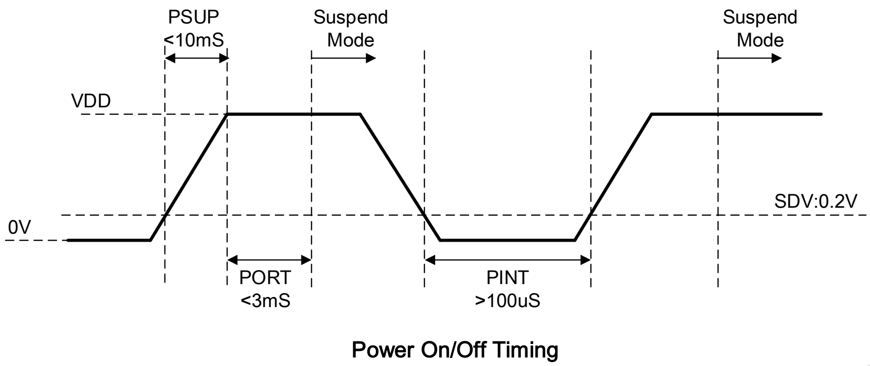


Figure 8. Power On/Off Timing

5.4 Communication Bus Interface I²C and Its Addresses

This device will be connected to a serial interface bus as a slave device under the control of a master device, such as the processor. Control of this device is carried out via I²C.

This device is compliant with I²C Bus Specification. As an I²C compatible device, this device has a 7-bit serial address and supports I²C protocols. This device supports standard and fast speed modes, 100kHz and 400kHz, respectively. External pull-up resistors are required to support all these modes.

There are only one I²C address available. The default value is 7CH.
If more I²C address options are required, please contact factory.

5.5 Internal Clock

This device has an internal clock for internal digital logic functions and timing management. This clock is not available to external usage.

5.6 Temperature Compensation

This device has built-in Temperature sensor and Temperature compensation function. The compensated magnetic sensor data is placed in the Output Data Registers automatically.

6 MODES OF OPERATION

6.1 Modes Transition

The device has three different modes, controlled by register (0x0A), mode bits Mode[1:0]. The main purpose of these modes is for power management. The modes can be transited from one to another, as shown below, through I²C commands of changing mode bits. The default mode is Suspend Mode.

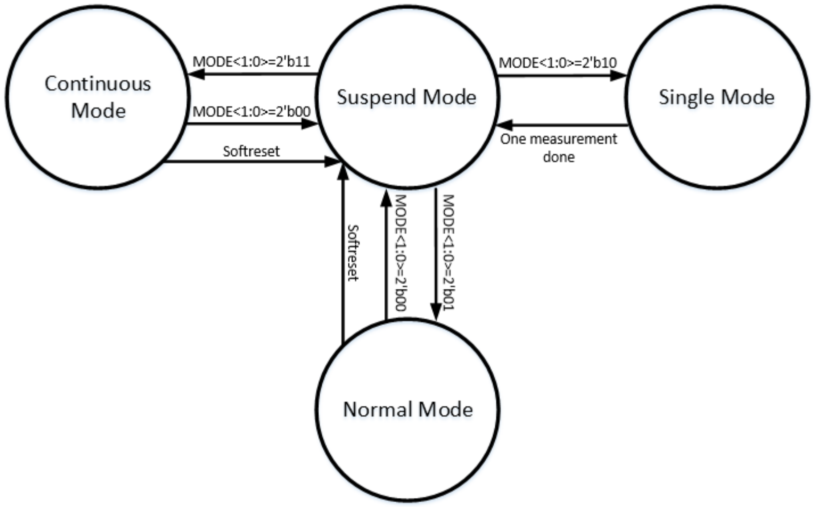


Figure 9. Modes Transition

6.2 Description of Modes

6.2.1 Normal Mode

During the Normal mode (MODE bits= 2'b01), the magnetic sensor continuously makes measurements and places measured data in data output registers. The field range register is controlled by RNG<1:0> in register 0BH and data output rate is controlled by ODR<1:0> in register 0AH. They should be set up properly for your applications in the normal mode.

6.2.2 Single Mode

During the Single Mode (MODE bits=2'b10), the whole chip runs only once and enter in the suspend mode after 1 measurement is finished.

6.2.3 Continuous Mode

During the Continuous Mode (MODE bits=2'b11), the whole chip runs all the time without sleep time, so the maximum ODR can be got at this mode. The self-test function can only be enabled in Continuous Mode and enters in Suspend Mode after the data is updated.

6.2.4 Suspend Mode

Suspend mode is the default magnetometer state upon POR and soft reset. Only few function blocks are activated in this mode which keeps power consumption as low as possible. In this state, register values are hold on by a lower power LDO, I2C interface is active, and all register read and write are allowed. There is no magnetometer measurement in this Mode.

7 APPLICATION EXAMPLES

7.1 Normal Mode Setup Example

- ✧ Write Register 0BH by 0x40 (Define Set/Reset mode, with Set/Reset On, Field Range 32Guass, ODR=200HZ)
- ✧ Write Register 0AH by 0x61 (Set Normal Mode, OSR1=8, OSR2=8)

7.2 Continuous Mode Setup Example

- ✧ Write Register 0BH by 0x00 (Define Set/Reset mode, with Set/Reset On, Field Range 32Guass)
- ✧ Write Register 0AH by 0x63 (Set Continuous Mode, OSR1=8,OSR2=8)

7.3 Self-test Example

- ✧ Write Register 0AH by 0x00 (Set Suspend Mode)
- ✧ Write Register 0AH by 0x03 (Set Continuous Mode)
- ✧ Waiting 20 millisecond until measurement ends
- ✧ Write Register 0EH by 0x80 (Set Selftest enable)
- ✧ Waiting 150 millisecond until measurement ends
- ✧ Check status register 09H[2] ,"1" means ready
- ✧ Read data Register 13H ~ 15H
- ✧ Self-test Judgment: If the delta value of each axis is in the range of following table, the chip is working properly.

	Selftest_X(13H)	Selftest_Y(14H)	Selftest_Z(15H)
Criteria （Unit:LSB）	-50 ~ -1	-50 ~ -1	-50 ~ -1

7.4 Suspend Mode Example

- ✧ Write Register 0AH by 0x00

7.5 Measurement Example

- ✧ Check status register 09H[0] ,"1" means ready
- ✧ Read data register 01H ~ 06H

7.6 Soft Reset Example

- ✧ Write Register 0BH by 0x80
- ✧ Write Register 0BH by 0x00

8 I2C COMMUNICATION PROTOCOL

8.1 I²C Timings

Below table and graph describe the I²C communication protocol times

Table 8. I²C Timings

Parameter	Symbol	Min.	Typ.	Max.	Unit
SCL Clock	f_{scl}	0	100	400	kHz
SCL Low Period	t_{low}	1.3			µS
SCL High Period	t_{high}	0.6			µS
SDA Setup Time	t_{sudat}	0.1			µS
SDA Hold Time	t_{hddat}	-		-	µS
Start Hold Time	t_{hdsta}	0.6			µS
Start Setup Time	t_{susta}	0.6			µS
Stop Setup Time	t_{susto}	0.6			µS
New Transmission Time	t_{buf}	1.3			µS
Rise Time	t_r (t_{rcl},t_{rdat})	0.02		0.3	µS
Fall Time	t_f (t_{fcl},t_{fdat})	0.02		0.3	µS

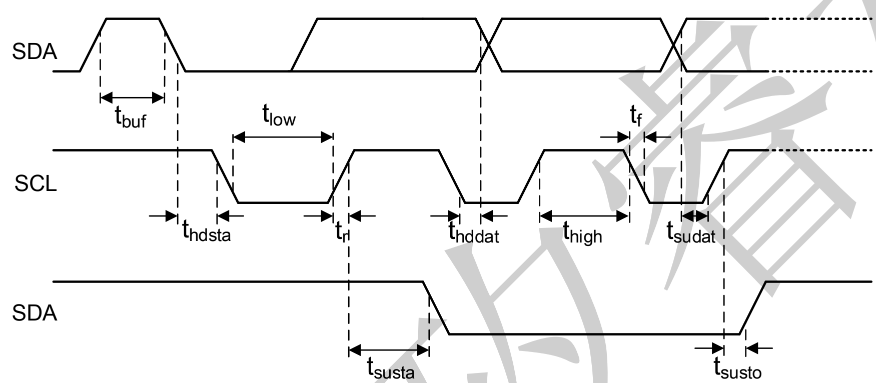


Figure 10. I²C Timing Diagram

8.2 I²C R/W Operation

8.2.1 Abbreviation

Table 9. Abbreviation

SACK	Acknowledged by slave
MACK	Acknowledged by master
NACK	Not acknowledged by master
RW	Read/Write

8.2.2 Start/Stop/Ack

START: Data transmission begins with a high to transition on SDA while SCL is held high. Once I²C transmission starts, the bus is considered busy.
STOP: STOP condition is a low to high transition on SDA line while SCL is held high.
ACK: Each byte of data transferred must be acknowledged. The transmitter must release the SDA line during the acknowledge pulse while the receiver must then pull the SDA line low so that it remains stable low during the high period of the acknowledge clock cycle.
NACK: If the receiver doesn't pull down the SDA line during the high period of the acknowledge clock cycle, it's recognized as NACK by the transmitter.

8.2.3 I2C Write

I²C write sequence begins with start condition generated by master followed by 7 bits slave address and a write bit (R/W=0). The slave sends an acknowledge bit (ACK=0) and releases the bus. The master sends the one-byte register address. The slave again acknowledges the transmission and waits for 8 bits data which shall be written to the specified register address. After the slave acknowledges the data byte, the master generates a stop signal and terminates the writing protocol.

Table 10. I²C Write

START	Slave Address							RW	SACK	Register Address (0x0A)								SACK	Data (0x01)								SACK	STOP
	1	1	1	1	1	0	0	0		0	0	0	0	1	0	1	0		0	0	0	0	0	0	0	1		

8.2.4 I2C Read

I²C read sequence consists of a one-byte I²C write phase followed by the I²C read phase. A start condition must be generated between two phases. The I²C write phase addresses the slave and sends the register address to be read. After slave acknowledges the transmission, the master generates again a start condition and sends the slave address together with a read bit (R/W=1). Then master releases the bus and waits for the data bytes to be read out from slave. After each data byte, the master has to generate an acknowledge bit (ACK = 0) to enable further data transfer. A NACK from the master stops the data being transferred from the slave. The slave releases the bus so that the master can generate a STOP condition and terminate the transmission.

Table 11. I²C Read

START	Slave Address							RW	SACK	Register Address (0x00)								SACK	
	1	1	1	1	1	0	0	0		0	0	0	0	0	0	0	0		
START	Slave Address							RW	SACK	Data (0x00)								NACK	STOP
	1	1	1	1	1	0	0	1		0	0	0	0	0	0	0	0		

9 REGISTERS

9.1 Register Map

The table below provides a list of the 8-bit registers embedded in the device and their respective function and addresses.

Chip ID is located at the address 00H, the default value is 90H. It can be used to recognize device.

Table 12. Register Map

Addr.	D7	D6	D5	D4	D3	D2	D1	D0	Access	POR /Soft Reset
00H	Chip ID								R Only	90H
01H	Data Output X LSB Register XOUT[7:0]								R Only	00H
02H	Data Output X MSB Register XOUT[15:8]								R Only	00H
03H	Data Output Y LSB Register YOUT[7:0]								R Only	00H
04H	Data Output Y MSB Register YOUT[15:8]								R Only	00H
05H	Data Output Z LSB Register ZOUT[7:0]								R Only	00H
06H	Data Output Z MSB Register ZOUT[15:8]								R Only	00H
09H	-	-	-	NVM_LOAD	NVM_RDY	ST_RDY	OVFL	DRDY	R Only	18H
0AH	OSR2[2:0]			OSR1[1:0]		-	MODE[1:0]		R/W	00H
0BH	SOFT_RST	ODR[2:0]			RNG[1:0]		SET/RESET MODE[1:0]		R/W	00H
0EH	SELF TEST	-	-	-	-	-	-	-	R/W	00H
13H	Data Output X Self-Test Register [7:0]								R Only	00H
14H	Data Output Y Self-Test Register [7:0]								R Only	00H
15H	Data Output Z Self-Test Register [7:0]								R Only	00H

9.2 Register Definition

9.2.1 Output Data Register

Registers 01H ~ 06H store the measurement data from each axis magnetic sensor in each working mode. In the normal mode, the output data is refreshed periodically based on the data update rate ODR setup in control registers 0AH. The data stays the same, regardless of reading status through I^2C, until new data replaces them. Each axis has 16-bit data width in 2's complement, i.e., MSB of 02H/04H/06H indicates the sign of each axis. The output data of each channel saturates at -32768 and 32767.

Register 13H~15H store the X,Y and Z self-test data under self-test mode separately. The selftest data of each channel

Table 13. Output Data Register

Addr.	7	6	5	4	3	2	1	0
01H	Data Output X LSB Register XOUT[7:0]							

02H	Data Output X MSB Register XOUT[15:8]
03H	Data Output Y LSB Register YOUT[7:0]
04H	Data Output Y MSB Register YOUT[15:8]
05H	Data Output Z LSB Register ZOUT[7:0]
06H	Data Output Z MSB Register ZOUT[15:8]
13H	Selftest Output X Register XST[7:0]
14H	Selftest Output Y Register YST[7:0]
15H	Selftest Output Z Register ZST[7:0]

9.2.2 Status Registers1

There is one status register located in address 09H.
Register 09H has two bits indicating for status flags, the rest are reserved for factory use. The status registers are read only bits.

Table 14. Status Registers1

Addr.	7	6	5	4	3	2	1	0
09H	-	-	-	NVM_LOAD_DONE	NVM_RDY	ST_RDY	OVFL	DRDY

DRDY bit denotes the status of data, which is set when all three-axis data is ready and loaded to the output data registers in each mode. It is reset to "0" by reading the status register through I²C commands
DRDY: "0": no new data, "1": new data is ready

OVFL bit is set high when either axis code output exceeds the range of [-32000,32000] LSB and reset to "0" after the status register is read.
OVFL: "0": no data overflow occurs; "1": data overflow occurs.

ST_RDY denotes the status of built-in selftest measurement
ST_RDY: "0": selftest not done yet; "1": selftest is done, selftest data is ready for reading

NVM_RDY denotes the status of built-in Non-volatile Memory
NVM_RDY: "0": NVM not ready for access; "1": NVM ready for access

NVM_LOAD_DONE denotes the status of data loading from built-in Non-volatile Memory
NVM_LOAD_DONE: "0": data loading from NVM not finished; "1": data loading from NVM finished

9.2.3 Control Registers1

Control registers 1 is in address 0AH. It sets the operational modes (MODE) and over sampling rate (OSR).

Two bits of MODE registers can transfer mode of operations in the device, the four modes are Suspend Mode, Normal mode, Single Mode, and Continuous Mode. The default mode after Power-On-Reset (POR) is Suspend Mode. Suspend Mode should be added in the middle of mode shifting between Continuous Mode, Single Mode, and Normal Mode.

Over sample Rate (OSR1) registers are used to control bandwidth of an internal digital filter. Larger OSR1 value leads to smaller filter bandwidth, less in-band noise and higher power consumption. It could be used to reach a good balance between noise and power. Four over sample ratio can be selected, 8,4,2 or 1.

Another filter is added for better noise performance; The depth can be adjusted through OSR2. There are totally 5 levels selectable.

Table 15. Control Registers 1

Addr	7	6	5	4	3	2	1	0
0AH	OSR2<2:0>			OSR1<1:0>		-	MODE<1:0>	

Reg.	Definition	00	01	10	11
Mode	Mode Control	Suspend Mode	Normal Mode	Single Mode	Continuous Mode

Reg.	Definition	00	01	10	11
OSR1	Over Sample Ratio	8	4	2	1

Reg.	Definition	000	001	010	011	100	101	110	111
OSR2	Low Pass Filter	1	2	4	8	16	16	16	16

9.2.4 Control Registers2

Control registers 2 is in address 0BH. It controls soft reset, output data rate and set/reset mode.

Set/Reset Mode can be control by the register SET/RESET MODE. There are 3 modes for selection：SET AND RESET ON， SET ONLY ON and SET AND RESET OFF. In SET ONLY ON or SET AND RESET OFF mode, the offset is not renewed during measuring.

Field ranges of the magnetic sensor can be selected through the register RNG. The full-scale range is determined by the application environments. The lowest field range has the highest sensitivity, therefore, higher resolution.

The Output data rate is controlled by ODR registers. Four data update frequencies can be selected: 10Hz, 50Hz, 100Hz or 200Hz.

Soft reset can be done by setting the register SOFT_RST High. Soft reset can be invoked at any time of any mode. After setting High， the SOFT_RST bit will not be auto-cleared. So after the soft reset command 0BH=80， another command 0BH=00 is always needed.

Table 16. Control Registers2

Addr.	7	6	5	4	3	2	1	0
0BH	SOFT_RST	ODR[2:0]			RNG[1:0]		SET/RESET MODE<1:0>	

Reg.	Definition	00	01	10	11
SET/RESET MODE	Set and reset mode control	Set and reset on	Set only on	-	Set and reset off

Reg.	Definition	00	01	10	11
RNG	Full Scale Range(Guass)	32	16	8	32

Reg.	Definition	000	001	010	011	100	101	110	111
ODR	Output data Rate(Hz)	1	10	50	100	200	200	200	200

Reg.	Definition	0	1
SOFT_RST	Soft reset	No reset	Soft reset, restore default value of all registers

9.2.5 Control Registers3

Self-test function is added for verification of the signal-chain. When the function is enable through the bit selftest, an inner-built current is generated and an additional signal is added to the sensor, generating a difference in the 3 axis value.

There are 1 bit reserved for built-in selftest. only when the chip is under Continuous Mode, the selftest bit can be set high to enable the chip to enter selftest Mode; After the selftest is done and selftest is generated, this bit will be auto cleared.

3 bytes are addressed to store the selftest data. They are 13H for X axis,14H for Y axis and 15H for Z axis.

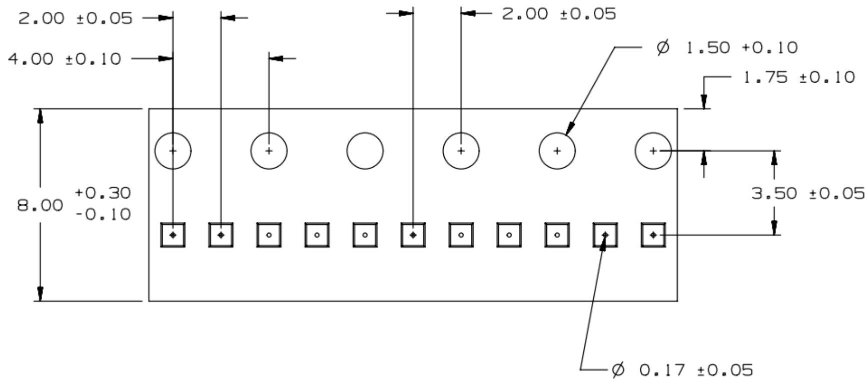
Table 17. Control Registers3

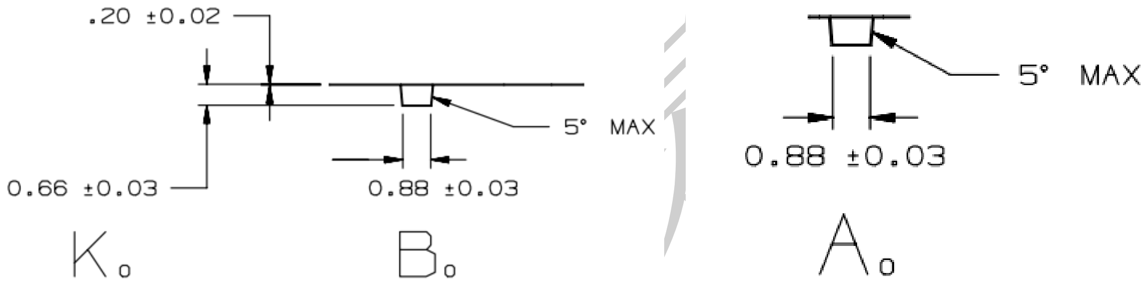
Addr	7	6	5	4	3	2	1	0
0EH	SELFTEST	-	-	-	-	-	-	-

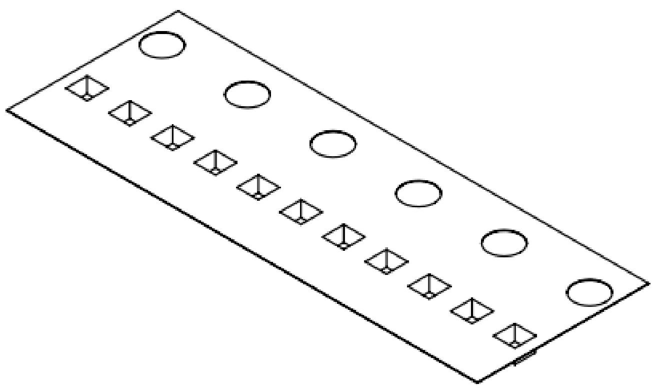
Reg.	Definition	0	1
SELFTEST	Selftest function control	Selftest disable	Selftest enable

10 TAPE AND REEL SPECIFICATION

QMC6309 is shipped in a standard carboard box. The box dimension for 1 reel is: L X W X H = cm x cm x cm.
The quantity is 5000pcs per reel, please handle with care

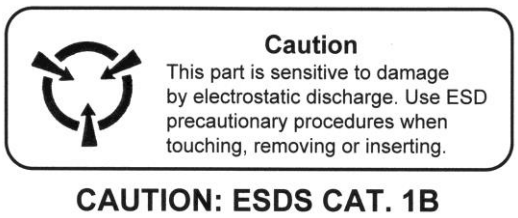






ORDERING INFORMATION

Ordering Number	Operating Temperature	Package	Packaging
QMC6309	-40°C ~ 85°C	WLCSP	Tape and Reel: 5k pieces/reel



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For more information on QST's Magnetic Sensors contact us at 86-21-69517300.

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