

QMI8658C DATASHEET

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QMI8658C Low Noise, Wide Bandwidth 6D Inertial Measurement Unit with Motion Co-Processor and Sensor Fusion

Features

- Low 15 mdps/√Hz gyroscope noise, low-latency, and wide bandwidth for performance applications such robotic vacuums, industrial tilt modules, pedestrian navigation and GNSS augmentation, 5G antenna stabilization, inertial navigation, and large industrial UAVs
- Low Noise 200µg/√Hz accelerometer
- Host (slave) interface supports MIPI™ I3C, I²C, and 3-wire or 4-wire SPI
- Accelerometer and gyroscope sensors feature signal processing paths with digitally programmable data rates and filtering
- Complete inertial measurement unit (IMU) with sensor fusion library with specified orientation accuracy of $\pm 3^{\circ}$ pitch and roll, $\pm 5^{\circ}$ yaw/heading
- High-performance XKF3™ 6/9-axis sensor fusion with in-run calibration for correction of gyroscope bias drift over-temperature and lifetime
- 3-axis gyroscope and 3-axis accelerometer in a small 2.5 x 3.0 x 0.86 mm 14-pin LGA package
- Integrated Gen 2 AttitudeEngine™ motion coprocessor with vector DSP performs sensor fusion at 1 kHz sampling rate, while outputting data to host processor at a lower rate – improving accuracy while reducing processor MIPS, power, and interrupt requirements
- Large 1536-byte FIFO can be used to buffer sensor data to lower system power dissipation
- Motion on demand technology for polling-based synchronization
- Large sensor dynamic ranges from $\pm 16^{\circ}/s$ to \pm 2048°/s for gyroscope and \pm 2 g to \pm 16 g for accelerometer
- Low power modes for effective power management
- Digitally programmable sampling rate and filters
- Embedded temperature sensor
- Wide extended operating temperature range (-40°C to 85°C)

Description

The QMI8658C is a complete 6D MEMS inertial measurement unit (IMU) with 9-axis sensor fusion and specified system level orientation accuracy. When using the QMI8658C in combination with the supplied XKF3 9D-sensor fusion, the system features an accurate ±3° pitch and roll orientation, and a ±5°yaw/heading typical specification.

With tight board-level gyroscope sensitivity of $\pm 3\%$, gyroscope noise density of 15 mdps/√Hz, and low latency, the QMI8658C is ideal for high performance consumer and for industrial applications.

The QMI8658C incorporates a 3-axis gyroscope and a 3-axis accelerometer. It provides a UI interface (supporting I3C, I²C and 3-wire or 4-wire SPI) .

The QMI8658C incorporates an advanced vector digital signal processor (DSP) motion co-processor called the AttitudeEngine. The AttitudeEngine efficiently encodes high frequency motion at high internal sampling rates, preserving full accuracy across lower-frequency output data rates.

This enables the application to utilize low output data rates (ODRs) or on-demand (host polling) while still acquiring accurate 3D motion data. The AttitudeEngine reduces the data processing and interrupt load on a host processor with no compromises in 3D motion tracking accuracy. The result is very low total system power in combination with high accuracy, which are essential to many portable and battery powered applications.

Applications

- **Toys**
- **Drones**
- E-bikes and scooters
- Motion-based remote controls and air mice

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1 General Information

1.1 Ordering Information

Table 1. Ordering Information

1.2 Marking Information

Figure 1. Top Mark

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1.4 Interface Operating Modes

The QMI8658C can operate in below mode, as shown in the Figure below.

Default mode of operation. In this mode, the QMI8658C is a slave device to a host processor that communicates to it using one of the following interfaces: I²C, I3C, and SPI (3-wire or 4-wire modes). This slave relationship to the host is the same for all operating modes. In Mode 1, the secondary interface is not enabled.

1.5 Application Diagrams

The typical application diagrams are shown in this section.

Note: As there is internal 200Kohm pull-up resistor, pull SDO/SA0 low will cost more current then pull it high.

1.6 Package & Pin Information

The pinout of the QMI8658C is shown in the figure below. The pin names and functionality are detailed in the table that follows. The pin functionality is dictated by the part's operating mode, as described in the section above.

Table 2. Pin Definitions

Notes:

- 1. This pin has an internal 200 $K\Omega$ pull up resistor.
2. The internal pull-up resistor can be disabled by
- 2. The internal pull-up resistor can be disabled by CTRL9 command (CTRL_CMD_SET_RPU). Refer to [5.9.5](#page-42-0) for details.
- 3. Refer to Section [12](#page-56-0) for detailed configuration information.

1.7 Recommended External Components

Note:

4. R_{pu} resistors are only needed when the Host Serial Interface is configured for l^2C (se[e I2C Interface](#page-63-0) section). They are not needed when the Host Serial Interface is configured for SPI or I3C. If pull-up resistors are used on SCL and SDA, then SPI, I3C and I²C Modes are all possible. If a pull-down resistor is used on SA0, an alternate slave address is used for I²C. SPI and I3C modes will be unaltered with the use of pull-up resistors for I²C. Additionally, a suitable pull up resistance (R_{pu}) value should be selected, accounting for the tradeoff between current consumption and rise time.

2 QMI8658C Architecture

QMI8658C is a smart sensor that combines a highperformance IMU with a powerful Single Instruction Multiple Data (SIMD) based Vector DSP motion coprocessor referred to as the AttitudeEngine™ (AE).

Included sensor fusion software (XKF3) allows the device to achieve orientation accuracies of $\pm 3^\circ$ for pitch and roll and $±5°$ for yaw/heading.

The QMI8658C includes a microcontroller for data scheduling, combined with Direct Memory Access (DMA) in order to allow efficient data shuttling on the chip. Multi-channel data is easily processed at rates up to 1 kHz.

An internal block diagram is shown in [Figure 2.](#page-5-1) The MEMS elements are amplified and converted by $\Sigma \Delta$ A/D converters, which are synchronized to a common clock so that all the motion measurements of acceleration, angular rate and magnetic heading are sampled at the same time minimizing any skew between channels. The data is then sent to a signal processing chain that accomplishes decimation, filtering, and calibration.

Once the data has been processed, it can be sent to the host processor depending on additional configuration settings, such as enabling the FIFO or using the AttitudeEngine.

2.1 AttitudeEngine Mode Overview

Brief descriptions of the major functions of the AttitudeEngine are discussed below. Note that the AttitudeEngine may be enabled or disabled and configured using the CTRL6 register.

- **Calibration**: The QMI8658C applies continuous onchip calibration of all the sensors (accelerometer, gyroscope, and magnetometer) including scale, offset, and temperature calibration. When used in conjunction with a sensor fusion filter (such as the XKF3) running on the host processor, estimated sensor errors can be updated in-use, allowing sensor calibration to be performed in the background without any host intervention. This offloads computationally expensive per-sample recalibration from the host processor to the QMI8658C
- **Sample Synchronization: The QMI8658C** automatically provides highly synchronous output between the various IMU accelerometer and gyroscope channels by using fully parallel ΣΔconverters. The QMI8658C also provides time synchronization of data between the IMU and the external magnetometer.
- **Motion Encoder:** The on-chip motion encoder performs 32-bit high-speed dead reckoning calculations at 1 kHz data rates allowing accurate capture of high frequency and coning effects. Orientation and velocity increments are calculated with full coning and sculling compensation and the magnetic field vector from the external magnetometer is rotated to the sensor frame of reference. This allows the lossless encoding (compression) of 6D motion to a low output data rate, while maintaining the accuracy provided by the 1 kHz input and data processing rate. Motion data encoded by the AttitudeEngine is available at a user programmable data rate (1 Hz to 64 Hz). The orientation and velocity increments from the AttitudeEngine are suitable for any 3D motion tracking application (orientation, velocity, and position) and may be further fused by the user with information from other sources such as a GNSS receiver or barometer in an optimal estimator.
- **Motion on Demand (MoD)**: The QMI8658C allows the host to access encoded motion data asynchronously (polling) and on demand. The motion data in the AttitudeEngine (AE) mode remains accurate even at very low output data rates. This allows easy integration and synchronization with other sensors for state-of-theart applications such as rolling shutter camera stabilization, optical sensors software de-blurring, GNSS integration and augmented or virtual reality.

2.2 Advantages of the Attitude Engine Approach

The advantages of the AttitudeEngine (AE) approach over the traditional sensor approach are briefly discussed below.

- **Low-Power Architecture: Dead reckoning** calculations are performed with the AE vector DSP that is designed to perform essential calculations while achieving high accuracy and low power simultaneously. The AE approach enables a typical interrupt rate reduction to the host processor of 10x and can be up to 100x for some applications. This significantly enhances the operational life of battery powered devices without any compromises in 3D motion tracking accuracy.
- **High Performance:** The motion encoder and sample synchronizer enable highly accurate strap down integration that can be fully compensated for coning and sculling artifacts.

2.3 9D Sensor Fusion and Auto-Calibration using XKF3

XKF3 is a sensor fusion algorithm, based on Extended Kalman Filter theory that fuses 3D inertial sensor data (orientation and velocity increments) and 3D magnetometer, also known as '9D', data to optimally estimate 3D orientation with respect to an Earth fixed frame.

A license to use XKF3 in a CMSIS compliant library form for Cortex M0+, M3, M4, M4F, for commercial purposes is provided with certain QST evaluation kits incorporating the QMI8658C.

A restricted-use license for use of XKF3 for commercial purposes is also granted for certain applications when XKF3 is used with the QMI8xxx series of IMUs, such as the QMI8658C/C family and the QMI8610.

XKF3 Features:

- Continuous Sensor Auto Calibration, No User Interaction Required
- High Accuracy, Real-Time, Low-Latency Optimal estimate of 3D Orientation, up to 1 kHz output data rate
- Ultra-low system power for 3D Orientation enabled by AttitudeEngine between 1 to 64 Hz output data rate without any degradation in accuracy
- Best-in-Class Immunity to Magnetic Distortions
- Best-in-Class Immunity to Transient Accelerations
- Flexible use Scenarios, North Referenced, Unreferenced
- Extensive Status Reporting for Smooth Integration in Applications
- Optimized Library for Popular Microcontrollers

Figure 10. Chip Orientation Coordinate System

2.4 Frames of Reference and Conventions for Using QMI8658C

The QMI8658C uses a right-handed coordinate system as the basis for the sensor frame of reference. Acceleration (a_x, a_y, a_z) are given with respect to the X- Y-Z coordinate system shown above. Increasing accelerations along the positive X-Y-Z axes are considered positive. Angular Rate $(\omega_x, \omega_y, \omega_z)$ in the counterclockwise direction around the respective axis are considered positive.

[Figure 10](#page-14-1) shows the various frames of reference and conventions for using the QMI8658C.

3 System, Electrical and Electro-Mechanical Characteristics

3.1 Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions. Stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Table 4. Absolute Maximum Ratings

Notes:

5. This is a mechanical shock (g) sensitive device. Proper handling is required to prevent damage to the part.

6. This is an ESD-sensitive device. Proper handling is required to prevent damage to the part.

3.2 Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for device operation. Recommended operating conditions are specified to ensure optimal performance. QST does not recommend exceeding them or designing to Absolute Maximum Ratings.

Table 5. Recommended Operating Conditions

Notes:

7. There is no rising time limitation for VDD.

3.3 System Level Specifications

System level specifications are provided to give guidance on the system performance in a
recommended and typical configuration. The typical configuration. The recommended system configuration is the QMI8658C and optionally a supported 3D magnetometer used with a supported host processor, running the XKF3 9Dsensor fusion and having executed and stored the result of the "Board Level Calibration" routine. The system

performance specifications assume that good engineering practices for the placement conditions of the QMI8658C and 3D magnetometer are considered. For example, do not place the QMI8658C where strong vibrations may occur or could be amplified; do not place the 3D magnetometer where magnetic fields other than the Earth magnetic field may be measured. Typical numbers are provided below unless otherwise noted.

3.4 Electro-Mechanical Specifications

VDD = VDDIO = 1.8 V, T = 25° C unless otherwise noted.

Table 7. Accelerometer Electro-Mechanical Specifications

Note:

8. System Turn On Time starts once VDDIO and VDD are within 1% of Final Value.

Table 8. Gyroscope Electro-Mechanical Specifications

Note:

9. System Turn On Time starts once VDDIO and VDD are within 1% of Final Value

Table 9. Magnetometer and AttitudeEngine Range and Scale

3.5 Accelerometer Programmable Characteristics

VDD = VDDIO = 1.8 V, T = 25° C unless otherwise noted. Typical numbers are provided below unless otherwise noted. All frequencies are ±5% and are synchronized to the gyroscope oscillator ("drive") frequency.

There are two sources of ODR frequency of accelerometer based on the operation mode. If only accelerometer is enabled, the ODR frequency is derived from the internal oscillator. If both accelerometer and gyroscope (6DOF mode) are enabled, the ODR frequency is derived from the natural frequency of gyroscope, which will nominally be 0.94 multiply the ODR values of enabling accelerometer only. [Table 10](#page-19-1) shows the two sets of ODR frequency, which can be referenced for later descriptions in the datasheet. Refer to section [5.4](#page-30-0) for detailed ODR configuration.

Table 11. Accelerometer Filter Characteristics (Accelerometer only)[\(10\)](#page-19-2)

10. When only accelerometer is enabled, the ODR is derived from the internal oscillator.

Table 12. Accelerometer Filter Characteristics (6DOF)[\(11\)](#page-20-0)

Note:

11. When both accelerometer and gyroscope are enabled, all frequencies are ±5% and are synchronized to the nature frequency of gyroscope.

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QMI8658C

3.6 Gyroscope Programmable Characteristics

VDD = VDDIO = 1.8 V, T = 25°C, and represent typical numbers unless otherwise noted. All frequencies are $\pm 5\%$ and are synchronized to the gyroscope nature frequency.

Table 13. Gyroscope Filter Characteristics

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3.7 Electrical Characteristics

VDD = VDDIO = 1.8 V, T = 25° C unless otherwise noted.

[Table 14](#page-22-2) describes the names for the pins in different functions. The later descriptions will directly use the function name in different scenarios instead of the pin name.

Table 14. Pin Name Mapped to Function Name

Table 15. Electrical Subsystem Characteristics

3.7.1 **Current Consumption**

VDD = VDDIO = 1.8 V, T = 25°C unless otherwise noted. IDD Current refers to the current flowing into the VDD pin. Typical numbers are provided below.

Table 16. Current Consumption for Accelerometer Only Typical Sensor Mode (Gyroscope Disabled)

Table 17. Current Consumption for Gyroscope Only Typical Sensor Mode (Accelerometer Disabled)

Table 18. Current Consumption for 6DOF Typical Sensor Mode (Accelerometer and Gyroscope Enabled). VDD = VDDIO = 1.8V

Table 19. Current Consumption for 6DOF Attitude Engine Mode (without Magnetometer). VDD = VDDIO = 1.8V

Table 20. Current Consumption for 9DOF Attitude Engine Mode (with Magnetometer). VDD = VDDIO = 1.8V

3.8 Temperature Sensor

The QMI8658C is equipped with an internal 16-bit embedded temperature sensor that is automatically turned on by default whenever the accelerometer or gyroscope is enabled. The temperature sensor is used internally to correct the temperature dependency of calibration parameters of the accelerometer and gyroscope. The temperature compensation is optimal in the range of -40°C to 85°C with a resolution of 0.0625°C (1/16 °C) or inversely, 16 LSB/ °C.

The QMI8658C outputs the internal chip temperature that the HOST can read. The output is 16 bits, with a (1/256)°C per LSB resolution. To read the temperature, the HOST needs to access the TEMP register *(see TEMP_L and TEMP_H in Data Output Registers in [0.](#page-24-1)* The HOST should synchronize to the interrupt, INT2, signal to get valid temperature readings.

Table 21. Temperature Sensor Specifications

4 Register Map Overview

The QMI8658C UI registers enable programming and control of the inertial measurement unit and associated on-chip signal processing. These registers are accessed through the UI interface – either SPI (4 wires or 3 wires) I3C, or I²C.

4.1 UI Register Map Overview

UI register map may be classified into the following register categories:

- General Purpose Registers
- Setup and Control Registers: control various aspects of the IMU.
- Host Controlled Calibration Registers: control and configure various aspects of the IMU via the host command interface called CTRL9
- Count Register for time stamping the sensor samples
- FIFO Registers: to set up the FIFO and detect data availability and over-run.
- [Table 22](#page-25-2) for UI Interface: contain all data for 9D sensors to be accessed from the UI interface either I²C or SPI.

Table 22. UI Register Overview

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5 UI Sensor Configuration Settings and Output Data

5.1 Typical Sensor Mode Configuration and Output Data

In Typical Sensor Mode, QMI8658C outputs raw sensor values. The sensors are configured and read using the registers described below. The accelerometer and gyroscope can be independently configured. [Table 23](#page-28-2) summarizes these pertinent registers.

5.2 AttitudeEngine (AE) Mode Configuration and Output Data

In AE Mode, the QMI8658C outputs orientation (quaternion) and velocity increments.

Orientation increments are expressed in unit quaternion format. $dQ = [QW, QX, QY, QZ]$ where QW is the scalar component of the quaternion increment and QX, QY and QZ are the (imaginary) vector components of the unit quaternion. Velocity increments are expressed in vector format $dV = [VX, VY, VZ]$.

[Table 24](#page-29-2) summarizes the operation of the AttitudeEngine mode.

Table 24. AttitudeEngine Mode Configuration and Output Registers

5.3 General Purpose Register

Table 25. General Purpose Register Description

5.4 Configuration Registers

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This section describes the various operating modes and register configurations of the QMI8658C.

Table 26. Configuration Registers Description

Note:

12. The accelerometer low power mode is only available when the gyroscope is disabled

13. In 6DOF mode (accelerometer and gyroscope are both enabled), the ODR is derived from the nature frequency of gyroscope, refer to sectio[n 3.5](#page-19-0) for more information.

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5.5 FIFO Registers

Table 27. FIFO Control/Status/Data Registers

5.6 Status and Time Stamp Registers

Table 28. Status and Time Stamp Registers

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5.7 Sensor Data Output Registers

Table 29. Sensor Data Output Registers Description

Continued on the following page

[Table 29](#page-37-1) Sensor Data Output Registers Description (Continued)

[Table 29](#page-37-1) Sensor Data Output Registers Description (Continued)

Table 30. AttitudeEngine Modes and Output Table

5.8 Reset register

Table 31. Reset Register Description

5.9 CTRL 9 Functionality (Executing Pre-defined Commands)

5.9.1 **CTRL 9 Description**

The protocol for executing predefined commands from an external host processor on the QMI8658C is facilitated by using the Control 9 (CTRL9) register. The register is available to the host via the UI SPI/I²C/I3C bus. It operates by the host writing a pre-defined value (Command) to the CTRL9 register. The firmware of the QMI8658C evaluates this command and if a match is found it executes the corresponding pre-defined function. Once the function has been executed, the QMI8658C signals the completion of this by setting STATUSINT.bit7 to 1, and raising INT1 interrupt if CTRL8.bit7 == 0 . The host must acknowledge this by reading STATUSINT.bit7, This is the CmdDone bit. After this read, the QMI8658C clear the STATUSINT.bit7 to 0 and pulls down the INT1 interrupt if CTRL8.bit7 $== 0$. This command presentation from the host to the QMI8658C and the subsequent execution and handshake between the host and the QMI8658C will be referred to as the "*CTRL9 Protocol*".

There are three types of interactions between the host and QMI8658C that follow the CTRL9 Protocol.

WCtrl9: The host needs to supply data to QMI8658C prior to the Ctrl9 protocol. (**Write – Ctrl9 Protocol**)

Ctrl9R: The host gets data from QMI8658C following the Ctrl9 protocol. (**Ctrl9 protocol – Read**)

Ctrl9: No data transaction is required prior to or following the Ctrl9 protocol. (**Ctrl9**).

5.9.2 **WCtrl9 (Write – CTRL9 Protocol)**

- 1. The host needs to provide the required data for this command to the QMI8658C. The host typically does this by placing the data in a set of registers called the CAL buffer. Eight CAL registers are used; the following table provides the name and addresses of these registers.
- 2. Write Ctrl9 register 0x0a with the appropriate Command value.
- 3. The Device will set STATUSINT.bit7 to 1, and raise $INT1 (if $CTRL8.bit7 == 0$), once it has executed the$ appropriate function based on the command value.
- The host must acknowledge this by reading STATUSINT.bit7 (CmdDone) which is reset to 0 on reading the register, completing the CTRL9 transaction. And INT1 is pulled low upon the register read if CTRL8.bit7 == 0.
- 5. If any data is expected from the device, it will be available at this time. The location of the data is specified separately for each of the Commands.

Table 32. CAL Register Addresses

5.9.3 **Ctrl9R (CTRL9 Protocol - Read)**

- 1. Write Ctrl9 register 0x0A with the appropriate Command value.
- 2. The Device will set STATUSINT.bit7 to 1, and raise INT1 (if CTRL8.bit7 == 0), once it has executed the appropriate function based on the command value.
- 3. The host must acknowledge this by reading STATUSINT.bit7 (CmdDone) which is then reset to 0 upon reading the register, completing the CTRL9 transaction. INT1 is pulled low upon the register read if $CTRL8.$ bit $7 == 0$.

Data is available from the device at this time. The location of the data is specified separately for each of the Commands.

5.9.4 **Ctrl9 (CTRL9 Protocol Acknowledge)**

- 1. Write CTRL9 register 0x0A with the appropriate Command value.
- 2. The Device set STATUSINT.bit7 to 1, and raise INT1 (if CTRL8.bit7 == 0), once it has executed the appropriate function based on the command value.
- 3. The host must acknowledge this by reading STATUSINT.bit7 (CmdDone) which is then reset to 0 upon reading the register, completing the CTRL9 transaction. INT1 is pulled low upon the register read if $CTRL8.$ bit $7 == 0$.

Table 33. CTRL9 Register CMND Values

5.9.5 **CTRL9 Commands in Detail**

CTRL_CMD_NOP

No Operation

CTRL_CMD_GYRO_BIAS

This CTRL9 Command is issued to copy bias_gx, bias_gy, bias_gz from CAL registers to FIFO and set GYROBIAS_PEND bit. CAL3_[H,L] is bias_gz, CAL2_[H,L] is bias_gy, CAL1_[H,L] is bias_gx.

CTRL_CMD_REQ_SDI

This CTRL9 command is used to retrieve motion data from the QMI8658C when Motion on Demand mode (MoD) is enabled. To enable MoD the device should have the AttitudeEngine orientation enabled. This can be done by enabling the AttitudeEngine by setting CTRL7 Bit 3 (sEN) to 1. Then the MoD mode can be enabled by setting CTRL6 Bit 7 (sMoD) to 1. The CTRL_CMD_REQ_MoD command is then issued by writing 0x0C to CTRL9 register 0x0A. This indicates to the QMI8658C that it is required to supply the motion data to the host. The device immediately makes available the orientation and velocity increments it has computed so far to the host by making them available at output registers 0x25 to 0x3D and raises the INT1 to indicate to the host that valid data is available.

CTRL_CMD_RST_FIFO

This CTRL9 command of writing 0x04 to the Ctrl9 register 0x0a allows the host to instruct the device to reset the FIFO.

CTRL_CMD_REQ_FIFO

This CTRL9 Command is issued when the host wants to get data from the FIFO. When the FIFO is enabled it will be indicated to the host by asserting INT2 and thus signaling that a flag condition (like FIFO full) has been reached and that data is available to be read by the host. This Command is issued by writing 0x05 to the CTRL9 register 0x0A. The device will raise INT1 to indicate that it is ready for a FIFO transaction. The host must read the STATUS1 register bit 0 (CmdDone). The device will direct the FIFO data to the FIFO_DATA register 0x17 until the FIFO is empty. Then the host must set FIFO_rd_mode to 0, which will cause the INT2 to be de-asserted.

CTRL_CMD_WRITE_WOM_SETTING

This CTRL9 Command is issued when the host wants to enable/modify the trigger thresholds or blanking interval of the Wake on Motion Feature of the device. Please refer to Section [9](#page-51-0) for details for setting up this feature. Once the specified CALx registers are loaded with the appropriate data, the Command is issued by writing 0x08 to CTRL9 register 0x0A.

CTRL_CMD_ACCEL_HOST_DELTA_OFFSET

This CTRL9 Command is issued when the host wants to manually change the accelerometer offset. Each delta offset value should contain 16 bits and the format is signed 4.12 (12 fraction bits). The user must write the offset to the following registers:

> Accel_Delta_X : {CAL1_H, CAL1_L} Accel Delta Y : {CAL2 H, CAL2 L} Accel_Delta_Z : {CAL3_H, CAL3_L}

Next, the Command is issued by writing 0x09 to CTRL9 register 0x0A. Note, this offset change is lost when the sensor is power cycled or the system is reset.

CTRL_CMD_GYRO_HOST_DELTA_OFFSET

This CTRL9 Command is issued when the host wants to manually change the gyroscope offset. Each delta offset value should contain 16 bits and the format is signed 11.5 (5 fraction bits). The user must write the offset to the following registers:

> Gyro_Delta_X : {CAL1_H, CAL1_L} Gyro_Delta_Y : {CAL2_H, CAL2_L} Gyro_Delta_Z : {CAL3_H, CAL3_L}

Next, the Command is issued by writing 0x0A to CTRL9 register 0x0A. Note, this offset change is lost when the sensor is power cycled or the system is reset.

CTRL_CMD_COPY_USID

This CTRL9 Command copies the following data into UI registers. It is initiated by the host writing 0x10 to CTRL9. After issuing the command, the data will be available for the host to read from the registers shown below:

> FW_Version byte $0 \rightarrow$ dQW_L FW_Version byte $1 \rightarrow$ dQW_H FW Version byte $2 \rightarrow$ dQX L USID_Byte_0 → dVX_L USID_Byte_1 → dVX_H USID_Byte_2 → dVY_L USID_Byte_3 → dVY_H USID_Byte_4 → dVZ_L USID_Byte_5 → dVZ_H

CTRL_CMD_SET_RPU

This CTRL9 Command is issued when the host wants to manually configure the IO pull-up resistors. Each bit controls a combination of resistors as shown below:

aux_rpu_dis: CAL1_L bit[0], SDX, SCX, RESV-NC(Pin 10)

icm_rpu_dis: CAL1_L bit[1], SDX

cs_rpu_dis: CAL1_L bit[2], CS

ics_rpu_dis: CAL1_L bit[3], SCL, SDA

The host writes the appropriate CAL1_L bit by issuing a WCtrl9 command with 0x11.

CTRL_CMD_AHB_CLOCK_GATING

When locking Mechanism is set (CTRL7.bit7 == 1(syncSmpl)), the CTRL_CMD_AHB_CLOCK_GATING should also be disabled to guarantee the locking mechanism of data reading, to prevent the possible misalignment.

CTRL_CMD_ON_DEMAND_CALIBRATION

This CTRL9 Command enables host to recalibrate the gyro sensitivity from time to time. The host must disable all the sensors by write 0x00 to CTRL7 first and then start the CTRL9 command process. During which, it is not necessary to place the device in quiet. The recalibrated parameters will be applied to the sensor data afterwards and will be lost if a power on reset or soft reset is implemented.

6 Interrupts

6.1 Overview

The QMI8658C has two Interrupt lines, INT1 and INT2. INT1 is used as a general-purpose interrupt. The details are described in the specific sections where INT1 and INT2 are used. The following provides a summary of the INT1 and INT2 usage. If syncSmpl $= 0$, then bit 1 of STATUSINT register will have the same value as INT1 and bit 0 of STATUSINT register will have the same value as INT2.

6.1.1 **Interrupt 1 (INT1)**

The following summarizes the use of INT1:

Set high for ~4 ms after reset to indicate that the chip is ready for normal operation.

If any operation has set INT1 it will always be cleared by reading STATUS1 register.

Used as part of the CTRL9 handshake protocol (*see sectio[n5.9\)](#page-40-1).*

When Wake on Motion (WoM) is enabled, INT1 can be selected to indicate WoM *(see section* [9](#page-51-0)*)***.**

INT1 can be used for motion detection event interrupt if CTRL8.bit is configured to 1, this bit will influence the any/no/sig-motion, pedometer, tap detection interrupt.

6.1.2 **Interrupt 2 (INT2)**

INT2 generally indicates data availability.

When Wake on Motion (WoM) is enabled, INT2 can be selected to indicate WoM *(see section* [9](#page-51-0)*)***.**

INT2 can be used for motion detection event interrupt if CTRL8.bit is configured to 0, this bit will influence the any/no/sig-motion, pedometer, tap detection interrupt. The source of interrupts will act with below interrupt in logic-OR.

The following indicates when INT2 will be asserted:

Register-Read Mode (FIFO Bypass Mode)

In Register-Read mode the accelerometer and gyroscope data are available in the Sensor Data Output registers (A[X,Y,Z]_[H,L]). The updating of these output registers and the functionality of the INT2 interrupt is controlled by the syncSmpl bit as described below.

With syncSmpl = 0 (refer t[o Table 26,](#page-30-1) CTRL7 register bit 7), INT2 is placed into edge trigger mode: the Sensor Data Output Registers are updated at the Output Data Rate (ODR), and INT2 is pulsed at the ODR. A rising edge on INT2 indicates that data is available and INT2 is cleared automatically after a short duration. It is the responsibility of the host to detect the rising edge and to latch the data before the next sample occurs. Note that the INT2 pulse width is dependent on the ODR and the sensor. It is not recommended to depend on the level to determine if INT2 has occurred.

With syncSmpl = 1 (refer t[o Table 26,](#page-30-1) CTRL7 register bit 7), INT2 is placed into level mode: The INT2 is asserted when data is available and remains asserted until the host reads STATUS0 register.

The device continues to refresh the output data until the STATUS0 register is read by host.

Once the STATUS0 is read by host the QMI8658C will deassert INT2 and stop refreshing the output data. Once the host detects INT2 has been deasserted it can start reading the output data.

Once the last byte of data has been read by the host (the QMI8658C keeps track) the QMI8658C will start updating the output register and set up the next INT2 when data is available in the output registers.

FIFO Enabled Mode *(see Section* [8](#page-49-0)*)*

When the FIFO is enabled in the **FIFO mode** (the mode bits in FIFO_CTRL register set to 01), INT2 is asserted when the FIFO is full or when the watermark is reached.

When the FIFO is enabled in the **Streaming Mode** (the mode bits in FIFO_CTRL register set to 10), INT2 is asserted when the watermark is reached but not when the FIFO is full because in the stream mode the FIFO will continue to fill by overwriting the oldest data in the FIFO.

INT2 is cleared in both the FIFO Mode and the Streaming Mode by clearing the FIFO_rd_mode bit in the FIFO_CTRL register. This is done as part of the CTRL9 command CTRL_CMD_REQ_FIFO.

Accelerometer and Gyroscope Self Test Modes *(see Section* [11](#page-55-0)*)*

INT2 is asserted to indicate availability of self-test data and is cleared by resetting the aST and gST bits in CTRL2 and CTRL3 registers, respectively.

7 Operating Modes

The QMI8658C offers a large number of operating modes that may be used to operate the device in a power efficient manner. These modes are described in

[Table 34](#page-45-1) and are shown in [Figure 11;](#page-47-0) they may be configured using the control (CTRL) registers.

Table 34. Operating Modes

[Table 34](#page-45-1) [Operating Modes](#page-45-1) (Continued)

QMI8658C

QMI8658C — 6D Inertial Measurement Unit with Motion Co-Processor

6D Inertial Measurement Unit with Motion Co-Processor

▪

7.1 General Mode Transitioning

Upon exiting the No Power state (i.e. on first applying power to the part) or exiting a Software Reset state, the part will enter the Power-On Default state. From there, the sensor can be configured in the various modes described in [Table 34](#page-45-1) and as shown in [Figure 11.](#page-47-0) The figure illustrates the timing associated with various mode transitions, and values for these times are given in the section below and i[n Table 7](#page-17-2) an[d Table 8.](#page-18-1)

7.2 Transition Times

The time it takes for data to be present after a mode switch will vary and depends on which mode has been selected. For example, the time it takes for retrieving data from the accelerometer after a mode switch is less than any mode that involves the gyroscope. The times t1, t2, t3 and t4, are defined as the time it takes from INT2 going high to data being present. The time, t5 is the time it takes to have a correct representation of the inertial state. t5 is variable and is associated with the user selected Output Data Rate (ODR). We have defined $t5 = (3/ODR)$ to generally represent that time.

t6 is the time it takes to go from a sensor powered state to a state where the sensors are off. This time depends on the Output Data Rate (ODR) and ranges from 1/ODR to 2/ODR.

t7 is the transition time between various states where the sensors are off.

t0 is the *System Turn On Time*, and is the time to enter the Power-On Default state from Software Reset, No Power, or Power down.

- Time t0 is the *System Turn on Time* and is 150ms seconds. This time only needs to be done once, upon transitioning from either a No Power or Power Down state, or whenever a reset is issued, which should not be done unless the intent is to have the device to go through its entire boot sequence (see the specification *System Turn On Time* in both [Table 7](#page-17-2) and [Table 8\)](#page-18-1).
- The *Gyro Turn on Time* (see [Table 8\)](#page-18-1) is comprised of t1 (the gyroscope wakeup time) and t5 (the part's filter settling time). t1 is typically 60 ms and t5 is defined as 3/ODR, where ODR is the output data rate in Hertz.
- The *Accel Turn on Time* (se[e Table 7\)](#page-17-2) is comprised of t2 (the accelerometer wakeup time) and t5 (the part's filter settling time). t2 is typically 3 ms, and t5 is defined as 3/ODR, where ODR is the output data rate in Hertz.
- Time t3 is the magnetometer wakeup time, which is typically 12 ms. Transitioning from the Power-On Default state to a Mag Only state or a Mag + Accel state takes the time $t3 + t5$, where $t5$ is defined as 3/ODR, where ODR is the output data rate in Hertz.
- The t7 transition is dependent on data transfer rates and is for I2C at 400 kHz is <100 µs for SPI at 11 Mbps is around 40 µs.

8 FIFO Description

8.1 Using the FIFO

The QMI8658C contains a programmable 1536-byte data buffer, which can be used as a FIFO buffer. The FIFO's operating mode and configuration are set via the FIFO_CTRL register. FIFO data may consist of gyroscope and accelerometer data and is accessible via the serial interfaces. The FIFO also supports burst reads. The host must complete its burst read prior to the next sensor data period. This time period is defined by the ODR selected. Depending on how many sensors are enabled, the host will need to read increments of 6, 12 or 18 bytes, corresponding to one, two and three sensors active at the same time. This feature helps reduce overall system power consumption by enabling the host processor to read and process the sensor data in bursts and then enter a low-power mode. The interrupt function may be used to alert when new data is available.

The FIFO size is configured using the FIFO_CTRL register. When the FIFO is enabled for two or more sensors, as is true for all modes that have multiple sensors active, the sensors must be set at the same Output Data Rate (ODR).

The FIFO is read through the I3C/I ²C/SPI interface by reading the FIFO_DATA register. Any time the Output Registers are read, data is erased from the FIFO memory.

The FIFO has multiple operating modes: Bypass, FIFO, and Streaming. The operating modes are set using the mode<1:0> bits in the FIFO_CTRL register.

Enabling FIFO

The FIFO is configured by writing to the FIFO_CTRL register and is enabled after the accelerometer and/or gyroscope are enabled. If the watermark function is enabled in the FIFO_CTRL register, pin INT2 is asserted when the FIFO watermark level is reached.

Reading Sensor Data from FIFO

Sensor data is read from the FIFO through the following command sequence. (For additional information, see CTRL9 description).

- Request access to FIFO data buffer by sending CTRL9 command 0x0D. This automatically sets FIFO rd mode bit to 1 in FIFO CTRL.
- Read FIFO DATA register to empty the FIFO.
- After FIFO is emptied, set FIFO_rd_mode bit to 0.

Note that when only the accelerometer or gyroscope is enabled, the sensor data format at the host interface is:

When 2 sensors are enabled, the sensor data format is:

When 3 sensors are enabled, the sequence will be extended to include the 6 corresponding magnetometer samples.

Bypass Mode

In Bypass mode (set in FIFO_CTRL), the FIFO is not operational and, therefore, remains empty. Sampled data from the gyroscope and/or Accelerometer are stored directly in the Sensor Data Output Registers. When new data is available, the old data is over-written.

FIFO Mode

In FIFO mode, data from the sensors are stored in the FIFO. The watermark interrupt, if enabled in FIFO_CTRL, is triggered when the FIFO is filled to the level specified by the value of wtm<1:0> in the FIFO_CTRL register. The FIFO continues filling until it is full. When full, the FIFO stops collecting data from the input channels. Data collection restarts when FIFO is emptied.

Streaming Mode

In Streaming mode (set in FIFO_CTRL), data from the gyroscope and accelerometer are stored in the FIFO. A watermark interrupt can be enabled and set as in FIFO mode. The FIFO continues filling until full. In this mode, the FIFO acts as a circular buffer, when full, the FIFO discards the older data as the new data arrives. Programmable watermark level events can be enabled to generate dedicated interrupts on the DRDY/INT2 pin (configured through the FIFO_CTRL register).

8.2 FIFO Register Description

Table 35. FIFO Registers Description

9 Wake on Motion (WoM)

9.1 Wake on Motion Introduction

The purpose of the Wake on Motion (WoM) functionality is to allow a system to enter a low power sleep state while the system is static and then to automatically awaken when moved. In this mode the system should use very little power, yet still respond quickly to motion.

It is assumed that the system host processor is responsible for configuring the QMI8658C correctly to place it into Wake on Motion mode, and that the system host processor will reconfigure the QMI8658C as necessary following a WoM interrupt.

Wake on Motion is configured through the CTRL9 command interface (see write-up for CTRL_CMD_WRITE_WOM_SETTING in Section [5.9.5](#page-42-0) [CTRL9 Commands in Detail\)](#page-42-0).

Table 36. Registers used for WoM

The threshold value is configurable to make the amount of motion required to wake the device controllable by the host application. The special threshold value of 0x00 can be used to disable the WoM mode, returning the interrupt pins to their normal functionality.

The interrupt initial value (1 or 0) and the interrupt pin used for signaling (INT1 or INT2) are selectable to make it easy for system integrators to use the WoM motion mode to wake the host processor from its deepest sleep level. Using the lowest power mode on many microcontrollers requires the use of special wake up pins that may have only a single polarity setting, and thus may not be useable for other special purposes such as timer captures.

The interrupt blanking time is a programmable number of accelerometer samples to ignore when starting WoM mode so that no spurious wake-up events are generated by startup transients.

9.2 Accelerometer Configuration

For additional tuning of the WoM responsiveness, the precise configuration of the accelerometer is left to the host. This gives the host processor the ability to program the desired sample rate and full-scale range.

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When a Wake on Motion event is detected the QMI8658C will set bit 2 (WoM) in the STATUS1 register. Reading STATUS1 by the host will clear the WoM bit and will reset the chosen interrupt line (INT1 or INT2, see previous section) to the value given by the WoM interrupt initial value (see previous section).

For each WoM event, the state of the selected interrupt line is toggled. This ensures that while the system is moved, the host processor will receive wakeup interrupts regardless of whether it uses high, low, positive- or negative-edge interrupts.

The QMI8658C stays in WoM mode until commanded to enter a new mode by the host processor.

9.4 Configuration Procedure

The host processor is responsible for all configurations necessary to put the QMI8658C into WoM mode. The specific sequence of operations performed by the host processor to enable WoM is shown in [Figure 13.](#page-51-5)

The WoM bit is cleared upon setting the WoM threshold to a non-zero value, and the selected interrupt pin is configured according to the settings. Special care has been taken that the WoM interrupt does not activate due to any transients when the accelerometer is first enabled. An interrupt blanking time is included that prevents such spurious interrupts to propagate.

9.5 Wake on Motion Control Registers

The WoM configuration is controlled by values written to the CAL1_x registers, as shown in [Table 36.](#page-51-6)

9.6 Exiting Wake on Motion Mode

To exit WoM mode the host processor must first clear CTRL7 to disable all sensors, and then write a threshold value of 0x0 for the WoM Threshold (see [Table 36,](#page-51-6) [Registers used for WoM\)](#page-51-6) and execute the WoM configuration CTRL9 command (see write-up for CTRL_CMD_WRITE_WOM_SETTING in Section [5.9.5](#page-42-0) [CTRL9 Commands in Detail\)](#page-42-0). On doing this the interrupt pins will return to their normal function. After zeroing the WoM Threshold the host processor may proceed to reconfigure the QMI8658C as normal, as in the case following a reset event.

c- Wait time equals to or higher than

f- When reading the last byte of data (GZ_H if gyro is enabled, or AZ_H if accel only is

g- To read next batch of data repeat steps 2 & 3. 4- To disable the sensor write 0x00 to CTRL7.

When the gyro is enabled the value of data_read_delay

ODR setting | ODR(Hz) | data_read_delay (usec) 0 7520 2 1 3760 2 2 1880 4 3 940 6 4 470 12 5 235 12 6 117.5 12 7 58.75 12 8 29.375 12

When the gyro is not enabled (accel only mode) the

ODR setting | ODR(Hz) | data_read_delay (usec)

value of data_read_delay is as follow:

data_read_delay (refer to [10.3\)](#page-53-3). d- At this time, the data will be locked.

enabled), the lock will be cleared.

(Enable back the AHB clock gating).

e- Read all sensor data.

10.3 Data_Read_Delay

is as follow:

10 Locking Mechanism

Locking Mechanism function can lock the sensor data and keep the values in data registers after the proper locking process, similar to the "shadow register", which enables host to read the locked data in unlimited delay without the risk of mixing the two consecutive data if reading happens at the time that the new data come and updating to the registers.

10.1 Set Locking Mechanism

The locking Mechanism is set when setting CTRL7.bit7 to "1" (syncSmpl).

Examples:

1- Enabling 6DOF in this mode:

write 0x83 to CTRL7.

2- Enable Accel Only in this mode:

write 0x81 to CTRL7.

After Enabling the sensor(s), the user needs to poll STATUSINT register before reading the sensor data for synchronization, refer t[o 10.2](#page-53-2) for more information.

Note: When using SPI (accel only mode with ODR less than 500Hz), I2C or I3C interfaces (in all ODRs), The user needs to disable the internal AHB clock gating by applying:

1- write 0x01 to CAL1_L register.

2- write 0x12(CTRL_CMD_AHB_CLOCK_GATING) to CTRL9 Register, follow the CTRL9 process.

After disabling the sensor, enable back the clock gating by:

- 1- write 0x00 to CAL1_L register.
- 2- write 0x12 to CTRL9 Register (CTRL_CMD_AHB_CLOCK_GATING), follow the CTRL9 process.

10.2 Reading sensor data

An example process of reading sensor data in locking mechanical mode is shown below:

- 1- Enable the sensor based on description in [10.1](#page-53-1) (Disable the AHB clock gating if needed)
- 2- Poll STATUSINT register:
	- a- Wait poll delay time.
	- b- Read STATUSINT register.

If the read value is not (0x01 or 0x03), repeat step 2.

If the value is (0x01 or 0x03) continue onto step 3.

3- Read data:

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10.4 On-The-Fly ODR changing

The on-the-fly ODR changing is supported, so host can change the ODR of sensor without disable the sensor.

An example sequence of change ODR without disable the sensor in locking mechanism is shown below:

- 1- Write CTRL2/CTRL3 to set the ODR's of accelerometer and gyroscope and full scales.
- 2- Write 0x83 (or 0x82) to CTRL7.
- 3- Read Sensor Data according [10.2.](#page-53-2)
- 4- Changing ODR on the fly:
	- a- Write 0x02 (or 0x03) to CTRL7(clear the syncSmpl bit).
	- b- Wait 700us.
	- c- Clear the lock in case if the data is still locked from previous ODR by reading GZ_H if gyroscope is enabled or AZ_H if accelerometer only is enabled.
	- d- Write CTRL2 / CTRL3 with the new ODR's.
	- e- Write 0x83 (or 0x82) to CTRL7.
- 5- Start poll and read Sensor Data using the new ODRs based o[n 10.2.](#page-53-2)
- 6- The new data will be stable in about 3~5 samples, so it is recommended to through away the first several samples at host side.

11 Performing Device Self Test

11.1 Accelerometer Self Test

The accelerometer Self Test is used to determine if the accelerometer is functional and working within acceptable parameters. It is implemented by applying an electrostatic force to actuate each of the three X, Y, and Z axis of the accelerometer. If the accelerometer mechanical structure responds to this input stimulus by sensing at least 200 mg, then the accelerometer can be considered functional within acceptable parameters. The accelerometer Self Test data is available to be read at registers dVX_L, dVX_H, dVY_L, dVY_H, dVZ_L and dVZ_H. The Host can initiate the Self Test at anytime by using the following procedure.

Procedure for accelerometer Self Test:

1- Make sure that the sensor is disabled. (CTRL7 = 0x00).

2- Set the bit aST to 1. $(CTRL2.bit7 = 1'b1)$

 The 16g Full Scale is always used for Accel Self Test, regardless to the aFS settings in CTRL2.

 The ODR setting in CTRL2 will be used for the Accel Self Test functionality.

3- Wait for QMI8658C to drive INT2 to "1".

4- Disable the Accel Self Test by clearing aST bit in CTRL2. (CTRL2.bit7 = 1'b0)

5- Wait for QMI8658C drive INT2 back to "0".

6- Read the Accel Self Test result:

 X channel: dVX_L and dVX_H (registers 81 and 82).

Y channel: dVY_L and dVY_H (registers 83 and 84).

 Z channel: dVZ_L and dVZ_H (registers 85 and 86).

 Read the 16 bits result in format (signed 5.11) from the according registers of X, Y & Z channels.

 If the absolute results of all three axes are higher than 200mg, the accelerometer can be consider functional. Otherwise, the accelerometer cannot be consider functional.

Here is an example of running accelerometer Self Test.

1- Write 0x00 to CTRL7.

2- Wait 1 msec.

3- Write 0x83 to CTRL2 (enable the Accel Self Test, and set 1KHz ODR).

4- Wait for INT2 is set to "1".

5- Write 0x03 to CTRL2 (disable the Accel Self Test).

6- Wait for INT2 to be cleared to "0".

7- Read final result from registers 81 up to 86 and compare.

11.2 Gyroscope Self Test

The gyroscope Self Test is used to determine if the gyroscope is functional and working within acceptable parameters. It is implemented by applying an electrostatic force to actuate each of the three X, Y, and Z axis of the gyroscope and measures the mechanical response on the corresponding X, Y, and Z axis. If the equivalent magnitude of the gyroscope output is greater than 300dps for each axis, the gyroscope can be considered as functional within acceptable parameters. The gyroscope Self Test data is available to be read at output registers dVX_L, dVX_H, dVY_L, dVY_H, dVZ_L & dVZ_H. The Host can initiate the Self Test anytime by using the following procedure.

Procedure for gyroscope Self Test:

1- Make sure that the sensor is disabled. (CTRL7 = 0x00).

2- Set the bit gST to 1. (CTRL3.bit7 = 1'b1).

 The 2048dps Full Scale and 1 KHz ODR is always used for gyroscope Self Test. The Full Scale and ODR portion in CTRL3 are ignored.

3- Wait for QMI8658C to drive INT2 to "1".

4- Disable the Gyro self test by clearing gST bit in CTRL3. (CTRL2.bit7 = 1'b0)

- 5- Wait for QMI8658C drive INT2 back to "0".
- 6- Read the Gyro Self Test result:
- X channel: dVX_L and dVX_H (registers 81 and 82).
- Y channel: dVY_L and dVY_H (registers 83 and 84).

Z channel: dVZ_L and dVZ_H (registers 85 and 86).

Read the 16 bits result in format (signed 12.4) from the according registers of X, Y & Z channels.

If the absolute results of all three axes are higher than 300dps, the gyroscope can be considered functional. Otherwise, the gyroscope cannot be considered functional.

Here is an example of running gyroscope Self Test.

1- Write 0x00 to CTRL7.

2- Wait 1 msec.

3- Write 0x83 to CTRL3 (enable the gyroscope Self Test).

4- Wait for INT2 is set to "1".

5- Write 0x03 to CTRL3(disable the gyroscope Self Test).

6- Wait for INT2 to be cleared to "0".

7- Read final result from registers 81 up to 86 and compare.

12 Host Serial Interface

QMI8658C Host Serial Interface supports MIPI I3C, I²C and SPI slave interfaces. For SPI, it supports both 3 wire and 4-wire modes. The basic timing characteristics for the interface are described below. Through the QMI8658C Host Serial Interface, the host can access, setup and control the QMI8658C Configuration Registers *(se[e Table 26\)](#page-30-1).*

12.1 Serial Peripheral Interface (SPI)

QMI8658C supports both 3-wire and 4-wire modes in the SPI slave interface. The SPI 4-wire mode uses two control lines (CS, SPC) and two data lines (SDI, SDO). The SPI 3-wire mode uses the same control lines and one bi-directional data line (SDIO). The SDI /SDIO pin is used for both 3- and 4-wire modes and is configured based on the mode selected. The SPI interface has been validated at 15 MHz and the timing parameters are measured at that interface frequency*.*

SPI transactions can be done in either Mode 0 (CPOL=0, CPHA=0) or Mode 3 (CPOL=1, CPHA=1). The interface automatically detects which mode is in use and configures clocking accordingly.

SPI 3- or 4-wire modes are configured by writing to bit-7 of CTRL1 register. 3-wire mode is selected when bit-7 is 1. The default configuration is 4-wire mode, i.e. bit-7 of CTRL1 is 0.

[Figure 15](#page-56-2) shows the SPI address and data formats.

SPI Features

Data is latched on the rising edge of the clock

In a typical SPI Master/Slave configuration the SPI master shares the SPI clock (SPC), the serial data input (SDI), and the Serial Data Output (SDO) with all the connected SPI slave devices. Unique Chip Select (CS) lines connect each SPI slave to the master.

[Figure 16](#page-56-3) and [Figure 17](#page-56-4) show typical multi-slave 4- and 3-wire configurations. The primary difference between the two configurations is that the SDI and SDO lines are replaced by the bi-directional SDIO line. The SDIO line

- Data should change on falling edge of clock
- Maximum frequency is 15 MHz
- Data is delivered MSB first
- Support single read/writes and multi cycle (Burst) read/writes**. NOTE:** burst writes to Configuration registers are NOT supported. These registers should be written in single cycle mode only**.**
- Supports 6-bit Address format and 8-bit data format
- ▪

Address Format

Read - indicates read (1) or write (0) transaction relative to the SPI master

Data Format

Figure 15. SPI Address and Data Format

is driven by the master with both address and data when it is configured for write mode. During read mode, the SDIO line is driven by the master with the address, and subsequently driven by the "addressed" slave with data.

[Figure 18](#page-57-0) and [Figure 19](#page-58-0) illustrate the waveforms for both 4-wire and 3-wire SPI read and write transactions. Note that CS is active during the entire transaction.

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12.1.1 **SPI Timing Characteristics**

The typical operating conditions for the SPI interface are provided in [Table 37.](#page-61-1) Please refer to [Table 5](#page-15-6) for the V_{IL}, V_{IH}, V_{OL}, V_{OH} definition to define the rising and falling edge condition of the timing symbols.

VDDIO = 1.8 V, T = 25° C unless otherwise noted.

Table 37. SPI Interface Timing Characteristics

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12.2 I ²C Interface

[Table 38](#page-63-1) provides the I²C interface timing characteristics while [Figure 23](#page-64-1) and [Figure 24](#page-64-2) illustrate the I²C timing for both fast and standard modes, respectively. Please refer to [Table 5](#page-15-6) for the V_{IL}, V_{IH}, V_{OL}, V_{OH} definition to define the rising and falling edge condition of the timing symbols.

During the slave device selection phase, the I²C master supplies the 7-bit I²C slave device address to enable the QMI8658C. When SA0 is pulled down externally, the 7 bit device address becomes 0x6B (0b1101011). In case of a slave device ID conflict, SA0 may be used to change bit-0 of the device address. The 7-bit device address for the QMI8658C is 0x6A (0b1101010) if SA0 is pulled up or left unconnected (internally there is a weak pull-up of 200 $K\Omega$).

During the slave register address phase bit-7 of the address is used to enable auto-increment of the target address. When bit-7 is set to 1 the target address is automatically incremented by one.

For additional technical details about the I²C standard, such as pull-up resistor sizing the user is referred to "UM10204 I²C-bus specification and user manual," published by NXP B.V.

Table 38. I ²C Timing Characteristics

Note:

14. C_B is the bus capacitance.

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Note:

15. Figure from JEDEC J-STD-020

Figure 26. Reflow Profile

13.3 Storage Specifications

QMI8658C storage specification conforms to IPC/JEDEC J-STD-020D.01 Moisture Sensitivity Level (MSL) 3. Floor life after opening the moisture-sealed bag is 168 hours with storage conditions: Temperature: ambient to ≤30°C and Relative Humidity: 60%RH.

14 Document Information

14.1 Revision History

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