

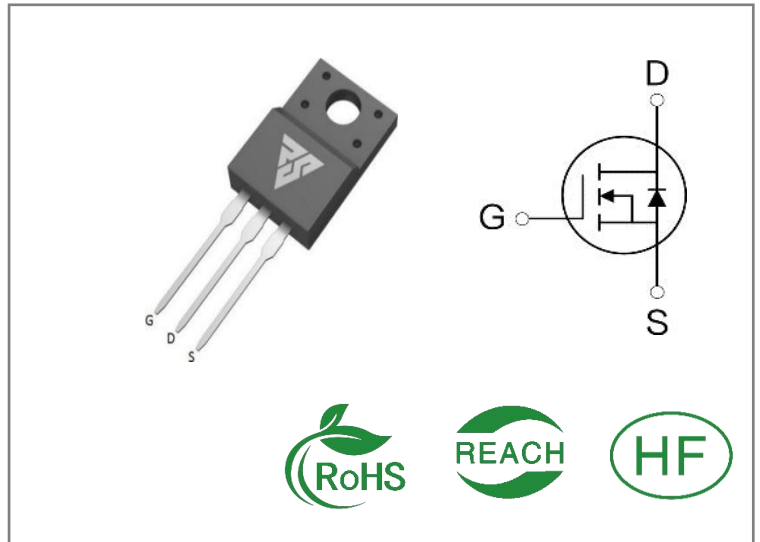
ID	R _{DS(ON)} (Typ)	VDSS
8A	0.75Ω	600V

Applications:

- Switch Mode Power Supply(SMPS)
- Uninterruptible Power Supply (UPS)
- Power Factor Correction (PFC)

Features:

- Fast switching speed
- 100% avalanche tested
- Improved dv/dt capability


Ordering Information

Part Number	Package	Marking	Packing	Qty.
RS8N60F	T0-220F	RS8N60F	Tube	50 PCS

Absolute Maximum Ratings Tc= 25°C unless otherwise specified

Symbol	Parameter	RS8N60F	Units
VDSS	Drain-to-Source Voltage	600	V
ID	Continuous Drain Current TC=25°C	8	A
IDM	Pulsed Drain Current (Note*1)	32	
PD	Power Dissipation	35	W
VGS	Gate- to- Source Voltage	±30	V
EAS	Single Pulse Avalanche Energy L = 10mH, VDD = 50V, RG = 25 Ω	240	mJ
TL TPKG	Maximum Temperature for Soldering	300 260	°C
	Leads at 0.063in(1.6mm)from Case for 10 seconds Package Body for 10 seconds		
TJ and TSTG	Operating Junction and Storage Temperature Range	-55 to 150	

* Drain Current Limited by Maximum Junction Temperature

Caution: Stresses greater than those listed in the“ Absolute Maximum Ratings” Table may cause permanent damage to the device.

Thermal Resistance

Symbol	Parameter	RS8N60F	Units	Test Conditions
R θ JC	Junction-to-Case	1.92	$^{\circ}\text{C} / \text{W}$	Drain lead soldered to water cooled heatsink, PD adjusted for a peak junction temperature of + 1 5 0 $^{\circ}\text{C}$
R θ JA	Junction-to-Ambient	62.5		1 cubic foot chamber, free air.

OFF Characteristics $T_J = 25^{\circ}\text{C}$ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
BVDSS	Drain- to- source Breakdown Voltage	600	--	--	V	$V_{GS}=0\text{V}, I_D=250\mu\text{A}$
IDSS	Drain- to- Source Leakage Current	--	--	1	μA	$V_{DS}=600\text{V}, V_{GS}=0\text{V}$
IGSS	Gate- to- Source Forward Leakage	--	--	100	nA	$V_{GS}=30\text{V}, V_{DS}=0\text{V}$
	Gate- to- Source Reverse Leakage	--	--	-100		$V_{GS}=-30\text{V}, V_{DS}=0\text{V}$

ON Characteristics $T_J = 25^{\circ}\text{C}$ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
RDS(on)	Static Drain- to- Source On-Resistance(Note*2)	--	0.75	0.9	Ω	$V_{GS}=10\text{V}, I_D=4\text{A}$
VGS(TH)	Gate Threshold Voltage	2	3	4	V	$V_{GS}=V_{DS}, I_D=250\mu\text{A}$

Resistive Switching Characteristics Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
td(ON)	Turn- on Delay Time	--	23	--	nS	$V_{DS}=300\text{V}$ $I_D=8\text{A}$ $R_G=25\Omega$
trise	Rise Time	--	15	--		
td(OFF)	Turn- OFF Delay Time	--	90	--		
tfall	Fall Time	--	30	--		

Dynamic Characteristics Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
Ciss	Input Capacitance	--	1420	--	pF	VGS=0V VDS=25V f=1.0MHz
Coss	Output Capacitance	--	130	--		
Crss	Reverse Transfer Capacitance	--	12	--		
Qg	Total Gate Charge	--	35	--	nC	VDS=400V ID=8A VGS=10V
Qgs	Gate- to- Source Charge	--	7	--		
Qgd	Gate-to-Drain(" Miller") Charge	--	18	--		

Source- Drain Diode Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
IS	Continuous Source Current	--	--	8	A	Integral pn- diode in MOSFET
ISM	Maximum Pulsed Current	--	--	32	A	
VSD	Diode Forward Voltage	--	--	1.4	V	IS=8A,VGS=0V
trr	Reverse Recovery Time	--	310	--	nS	VGS=0V IS=8A di/dt=100A/μs
Qrr	Reverse Recovery Charge	--	4.1	--	μC	

Notes:

- * 1. Repetitive rating, pulse width limited by maximum junction temperature.
- * 2. Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 1\%$

Typical Feature Curve

Figure 1: Output Characteristics

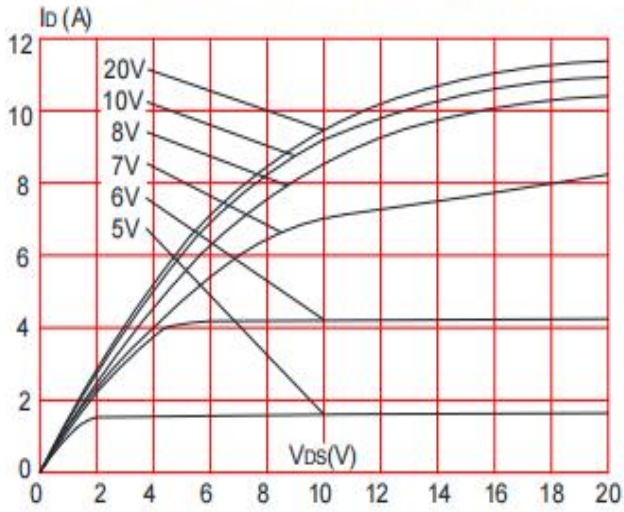


Figure 2: Typical Transfer Characteristics

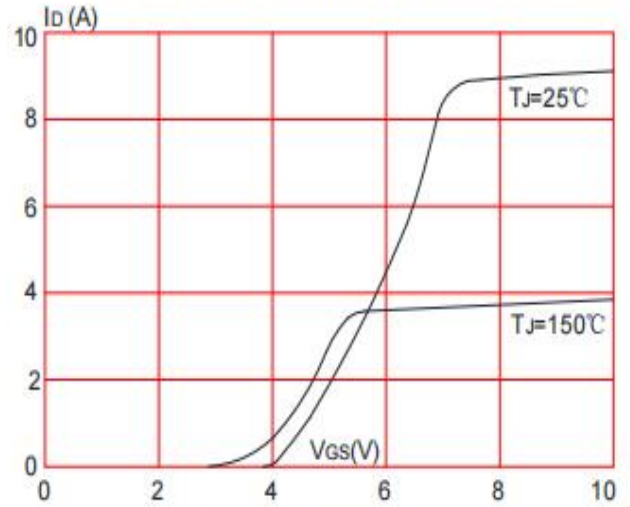


Figure 3: On-resistance vs. Drain Current

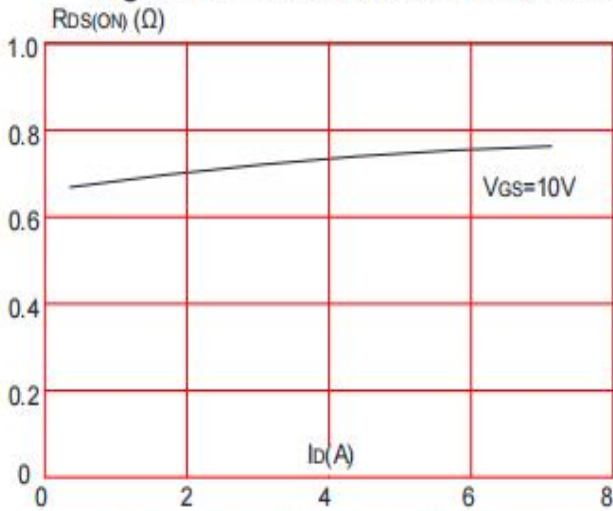


Figure 4: Body Diode Characteristics

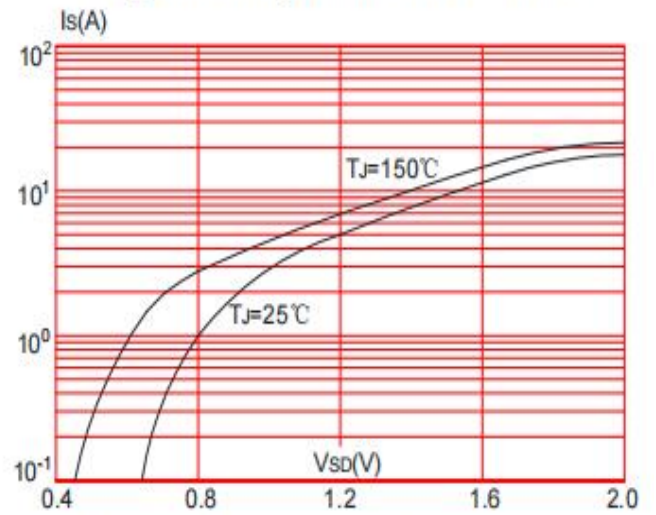


Figure 5: Gate Charge Characteristics

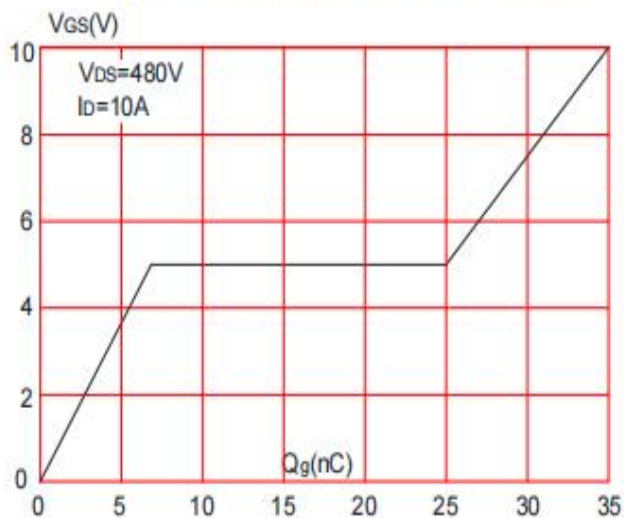


Figure 6: Capacitance Characteristics

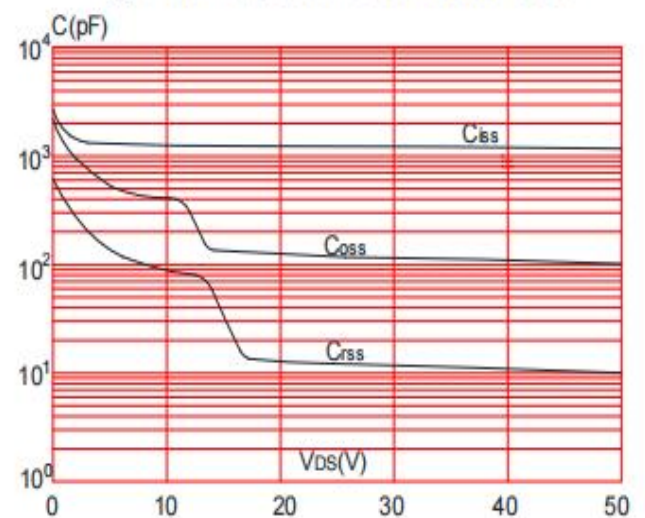


Figure 7: Normalized Breakdown Voltage vs. Junction Temperature

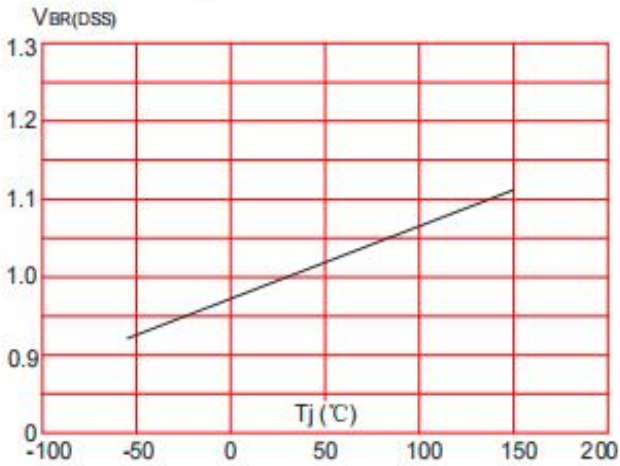


Figure 8: Normalized on Resistance vs. Junction Temperature

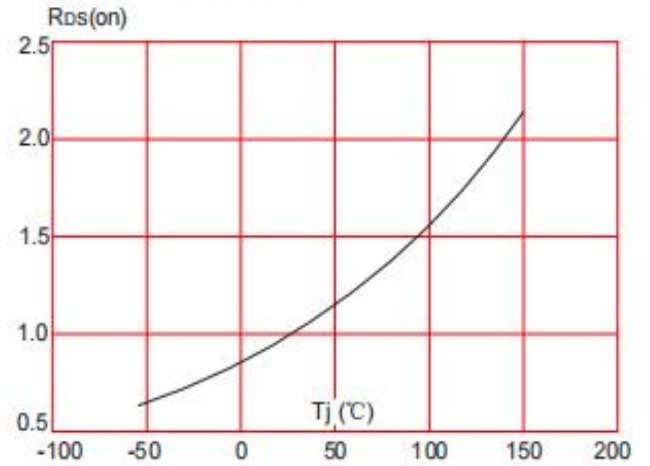


Figure 9: Maximum Safe Operating Area

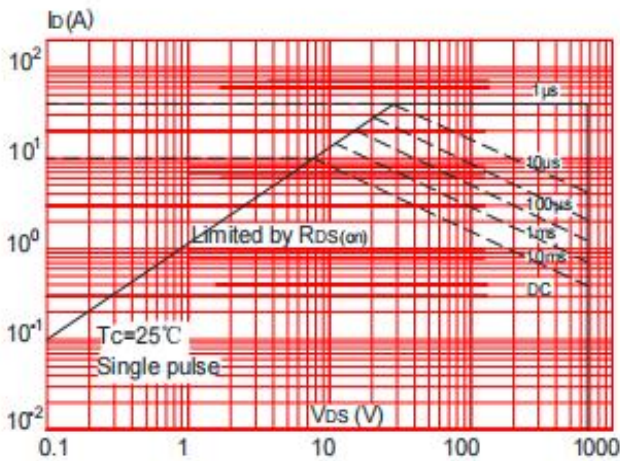


Figure 10: Maximum Continuous Drain Current vs. Case Temperature

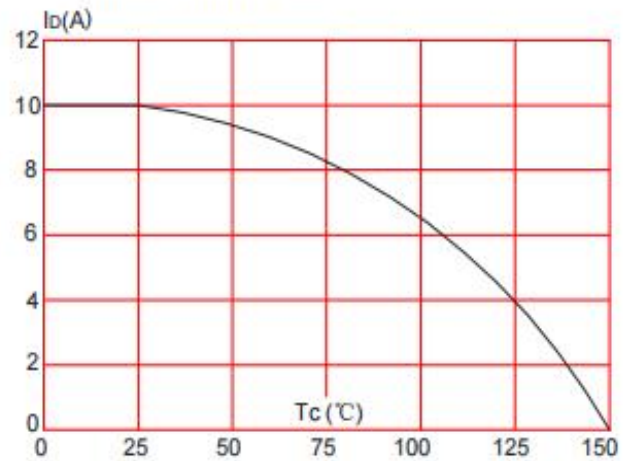
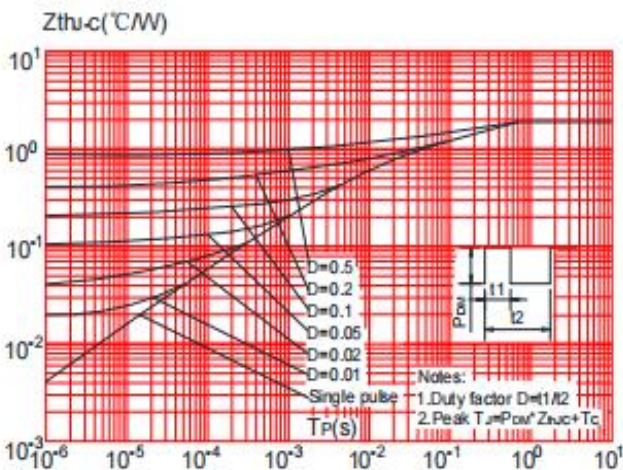


Figure 11: Maximum Effective Transient Thermal Impedance, Junction-to-Case



Test Circuits and Waveforms

Figure A: Gate Charge Test Circuit and Waveform

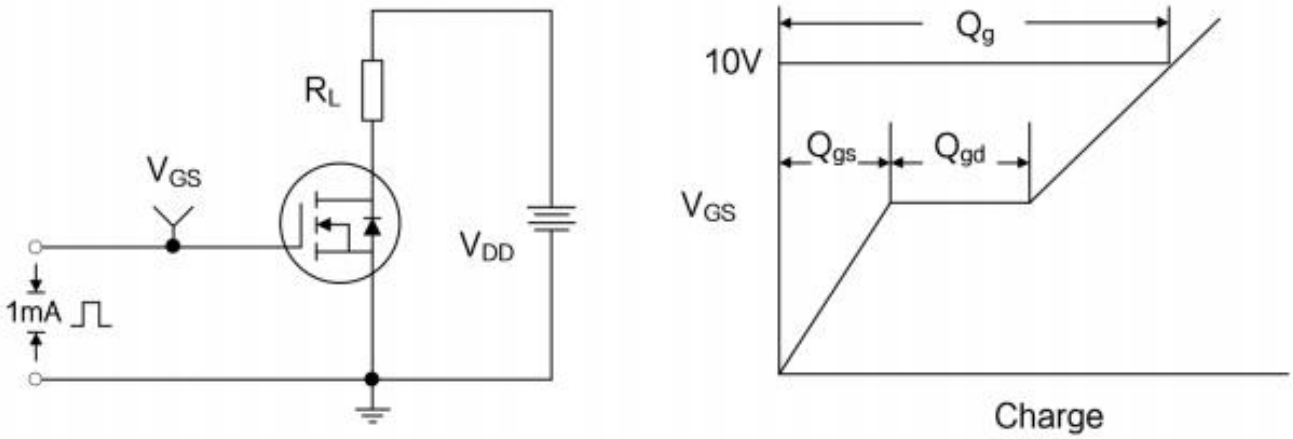


Figure B: Resistive Switching Test Circuit and Waveform

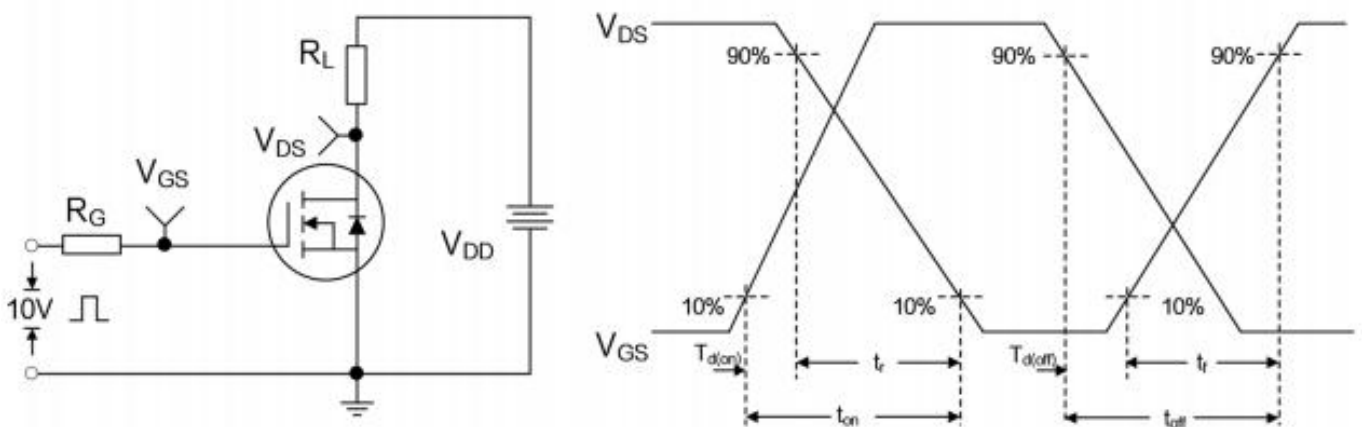
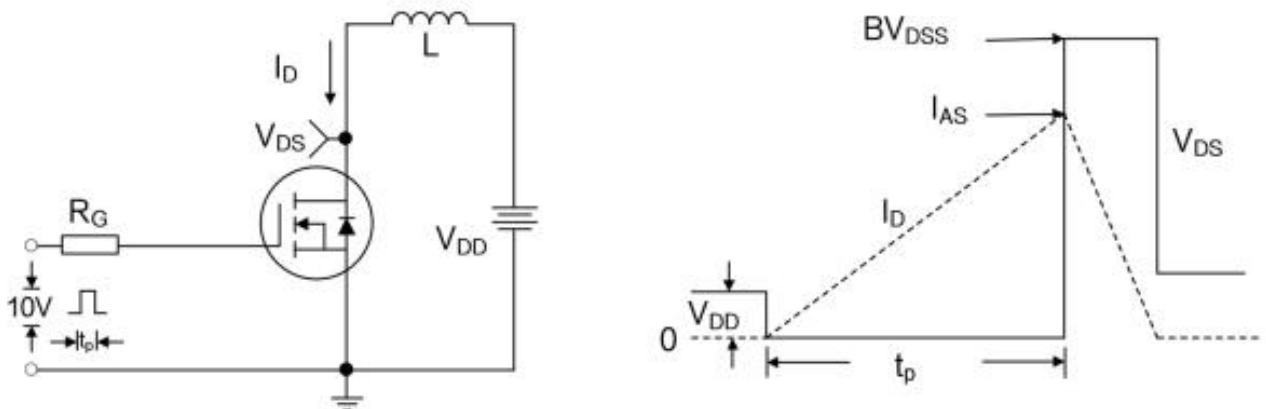
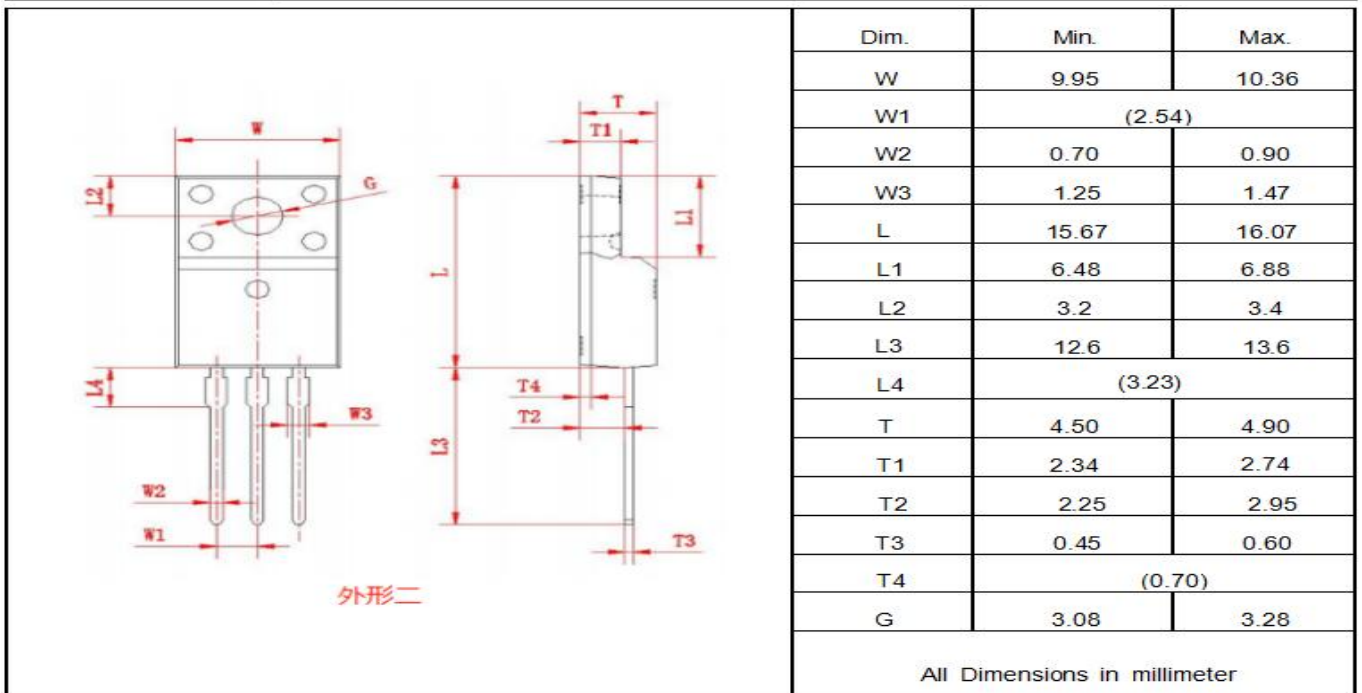
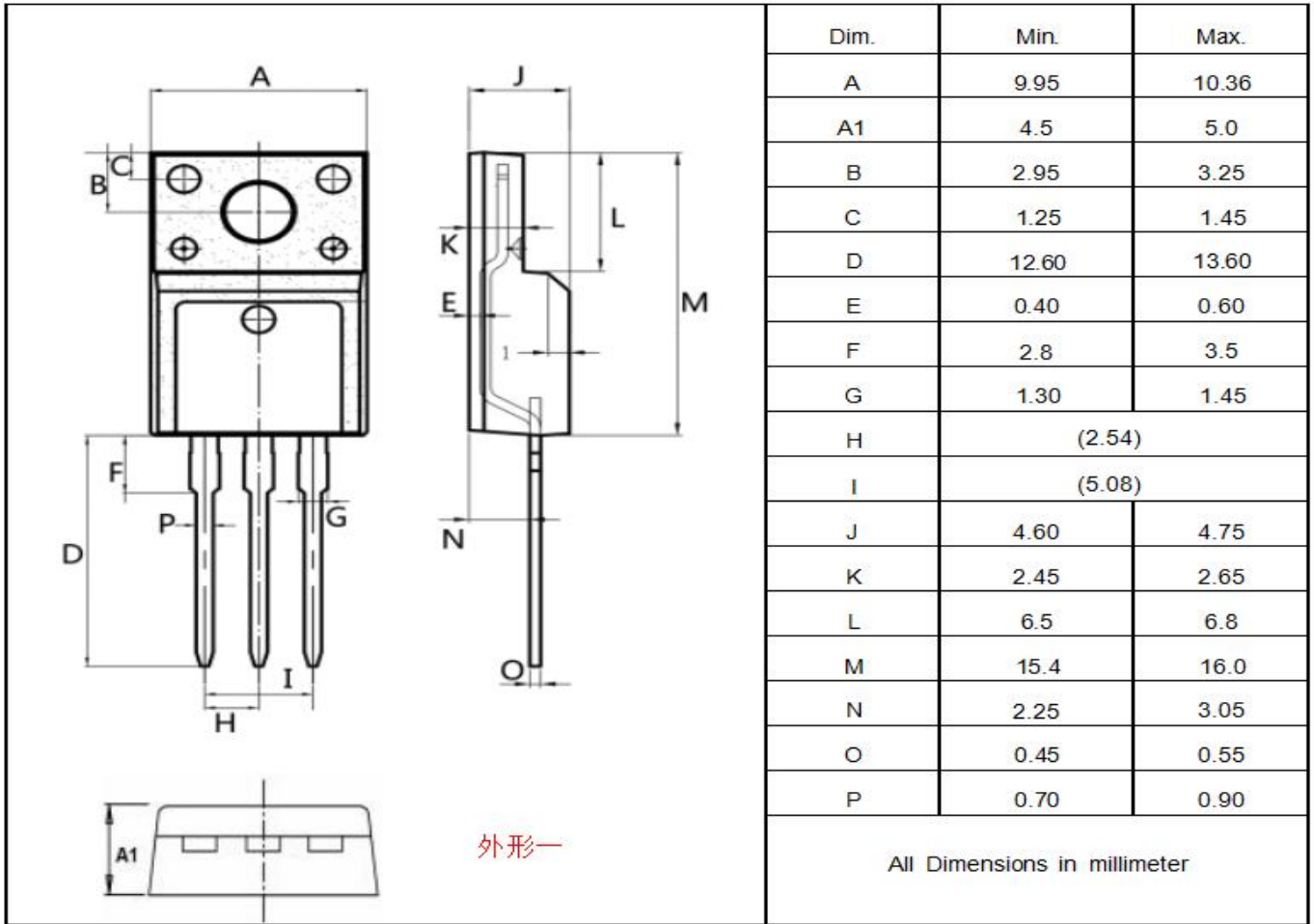


Figure C: Unclamped Inductive Switching Test Circuit and Waveform



Package outline drawing(TO-220F Unit: mm)



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