

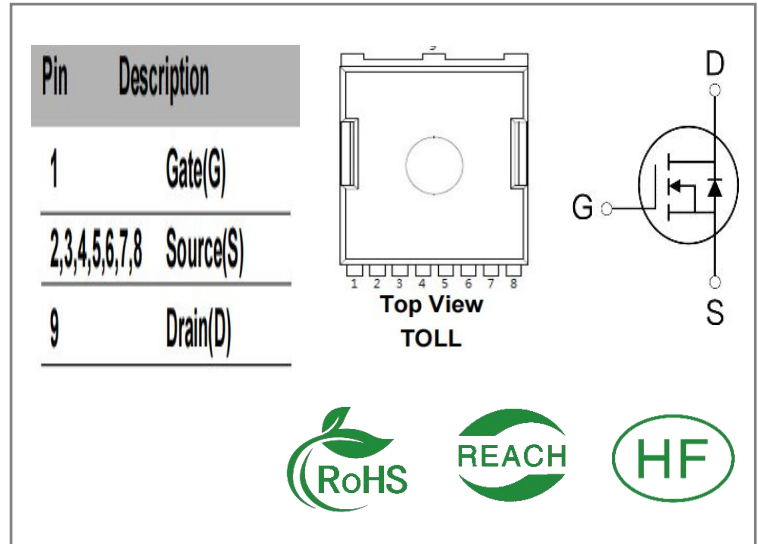
ID	R _{DS(ON)} (Typ)	VDSS
300A	1.7mΩ	100V

Applications:

- Load Switch
- PWM Applications
- Power Managment

Features:

- Fast switching speed
- 100% avalanche tested
- Improved dv/dt capability


Ordering Information

Part Number	Package	Marking	Packing	Qty.
RS100N300I	TOLL-8L	RS100N300I	Tape&reel	2000 PCS

Absolute Maximun Ratings T_c= 25°C unless otherwise specified

Symbol	Parameter	RS100N300I	Units
VDSS	Drain-to-Source Voltage	100	V
ID	Continuous Drain Current TC=25°C	300	A
ID	Continuous Drain Current TC=100°C	180	
IDM	Pulsed Drain Current	1200	
PD	Power Dissipation	300	W
VGS	Gate- to- Source Voltage	±20	V
EAS	Single Pulse Avalanche Engergy L = 0.5mH,VDD =50V, RG = 25Ω, Tj = 25°C	420	mJ
TL TPKG	Maximum Temperature for Soldering	300 260	°C
	Leads at 0.063in(1.6mm)from Case for 10 seconds		
	Package Body for 10 seconds		
TJ and TSTG	Operating Junction and Storage Temperature Range	-55 to 150	

* Drain Current Limited by Maximum Junction Temperature

Caution: Stresses greater than those listed in the“ Absolute Maximum Ratings” Table may cause permanent damage to the device.

Thermal Resistance

Symbol	Parameter	RS100N300I	Units	Test Conditions
R θ JC	Junction-to-Case	0.42	°C / W	Drain lead soldered to water cooled heatsink, PD adjusted for a peak junction temperature of + 150 °C
R θ JA	Junction-to-Ambient	55		1 cubic foot chamber, free air.

OFF Characteristics T_J= 25°C unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
BVDSS	Drain- to- source Breakdown Voltage	100	--	--	V	VGS=0V, ID=250μA
IDSS	Drain- to- Source Leakage Current	--	--	1	μA	VDS=80V, VGS=0V
IGSS	Gate- to- Source Forward Leakage	--	--	100	nA	VGS=20V, VDS=0V
	Gate- to- Source Reverse Leakage	--	--	-100		VGS=-20V, VDS=0V

ON Characteristics T_J=25°C unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
RDS(on)	Static Drain- to- Source On-Resistance	--	1.7	2.2	mΩ	VGS=10V, ID=20A
VGS(TH)	Gate Threshold Voltage	2.0	--	4.0	V	VGS=VDS, ID=250μA

Resistive Switching Characteristics Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
td(ON)	Turn- on Delay Time	--	33	--	nS	VDS=50V ID=50A RG=3Ω VGS=10V
trise	Rise Time	--	28	--		
td(OFF)	Turn- OFF Delay Time	--	102	--		
tfall	Fall Time	--	36	--		

Dynamic Characteristics Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
Ciss	Input Capacitance	--	8397	--	pF	VGS= 0V VDS=50V f=1MHz
Coss	Output Capacitance	--	2783	--		
Crss	Reverse Transfer Capacitance	--	127	--		
Qg	Total Gate Charge	--	112	--	nC	VDS= 50V ID=50A VGS=10V
Qgs	Gate- to- Source Charge	--	31	--		
Qgd	Gate-to-Drain(" Miller") Charge	--	26	--		

Source- Drain Diode Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
IS	Continuous Source Current	--	--	300	A	Integral pn- diode in MOSFET
ISM	Maximum Pulsed Current	--	--	1200	A	
VSD	Diode Forward Voltage	--	--	1.2	V	IS=20A,VGS=0V
trr	Reverse Recovery Time	--	89	--	nS	VGS=0V IS=20A di/dt=100A/μs
Qrr	Reverse Recovery Charge	--	178	--	nC	

Notes:

- * 1. Repetitive rating,pulse width limited by maximum junction temperature.
- * 2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 0.5%

Typical Feature Curve

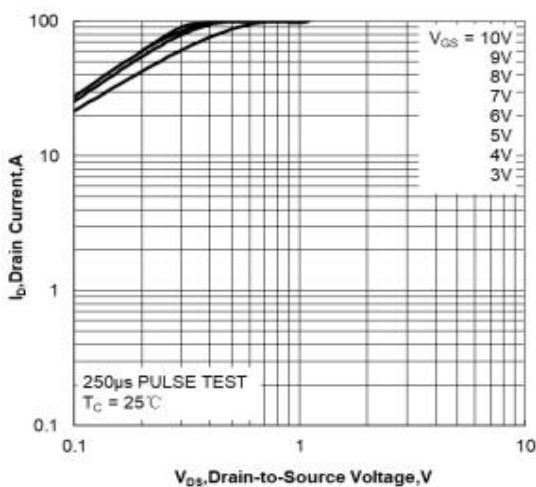


Figure 1. Output Characteristics

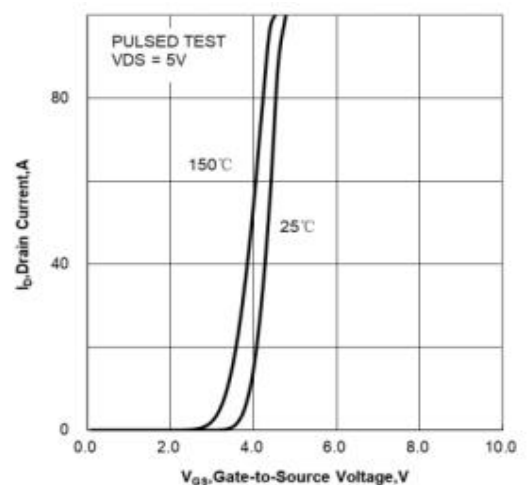


Figure 2. Transfer Characteristics

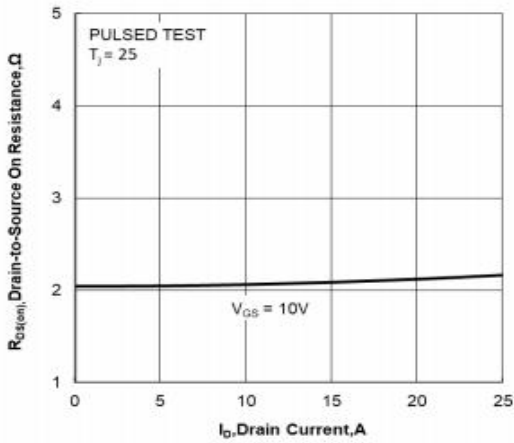


Figure 3. Drain-to-Source On Resistance vs Drain Current

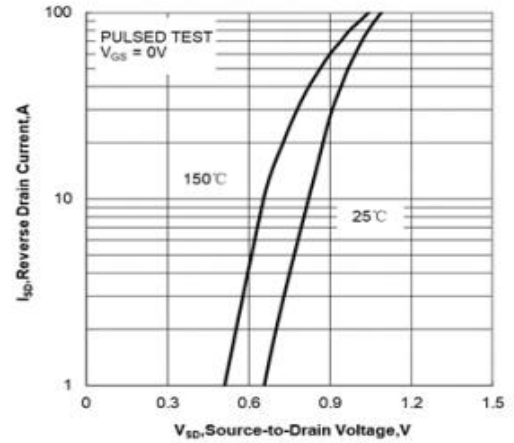


Figure 4. Body Diode Forward Voltage vs Source Current and Temperature

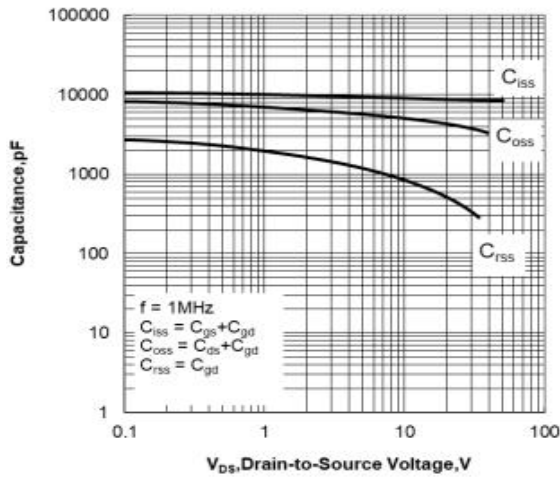


Figure 5. Capacitance Characteristics

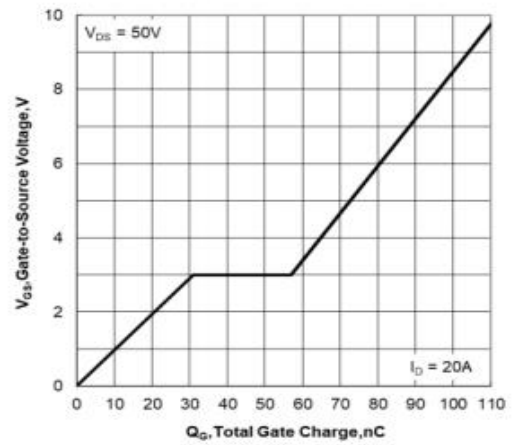


Figure 6. Gate Charge Characteristics

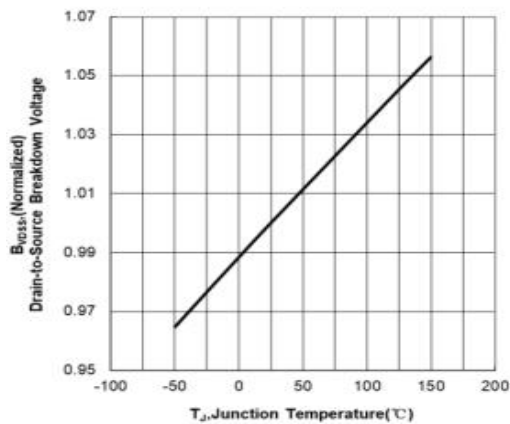


Figure 7. Normalized Breakdown Voltage vs Junction Temperature

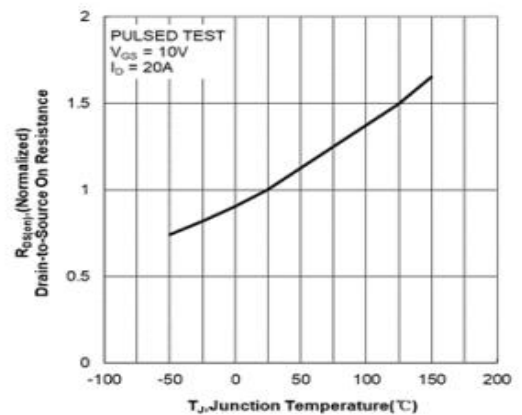


Figure 8. Normalized On Resistance vs Junction Temperature

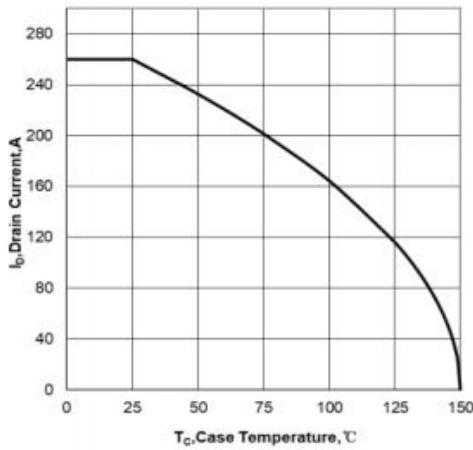


Figure 9. Maximum Continuous Drain Current vs Case Temperature

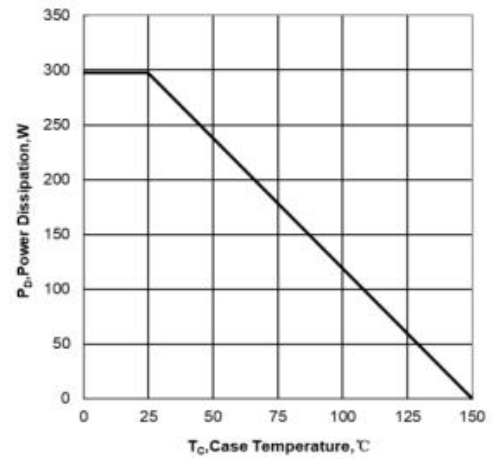


Figure 10. Maximum Power Dissipation vs Case Temperature

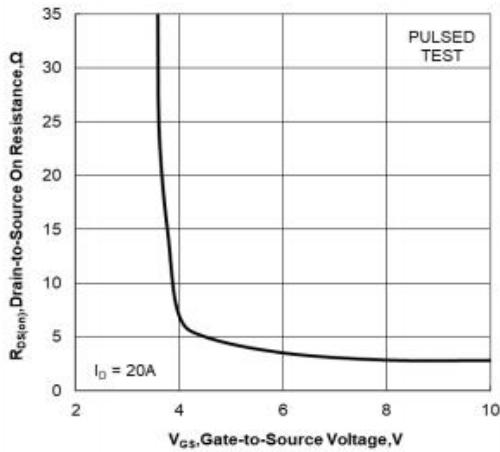


Figure 11. Drain-to-Source On Resistance vs Gate Voltage and Drain Current

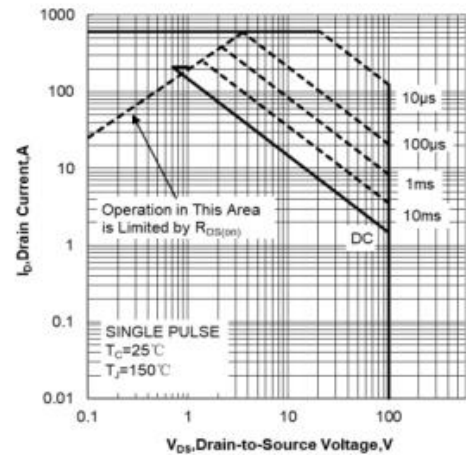


Figure 12. Maximum Safe Operating Area

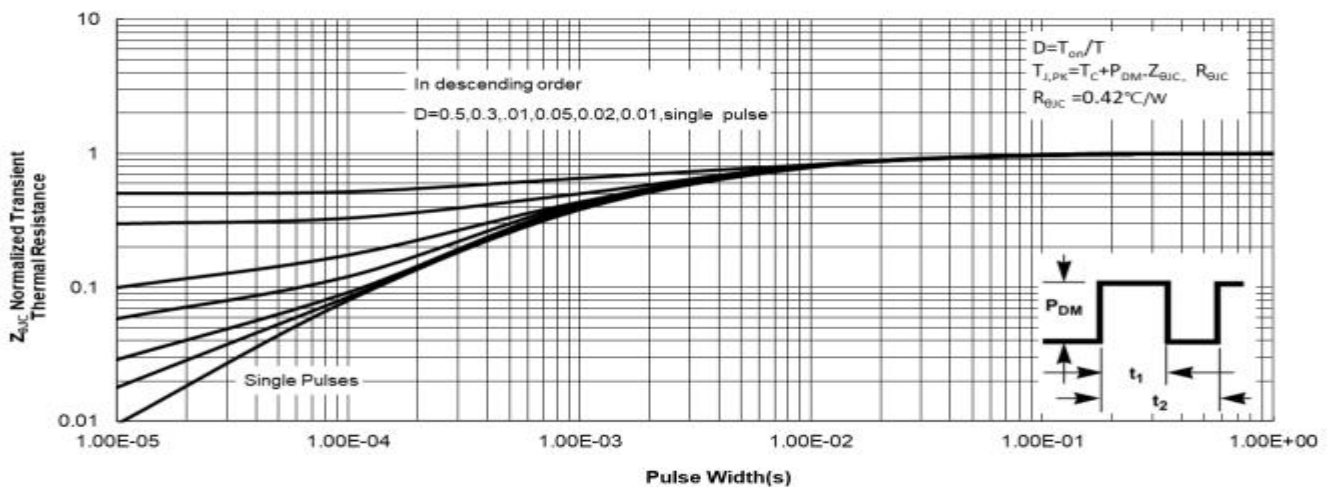


Figure 13. Maximum Effective Transient Thermal Impedance, Junction-to-Case

Test circuits and Waveforms

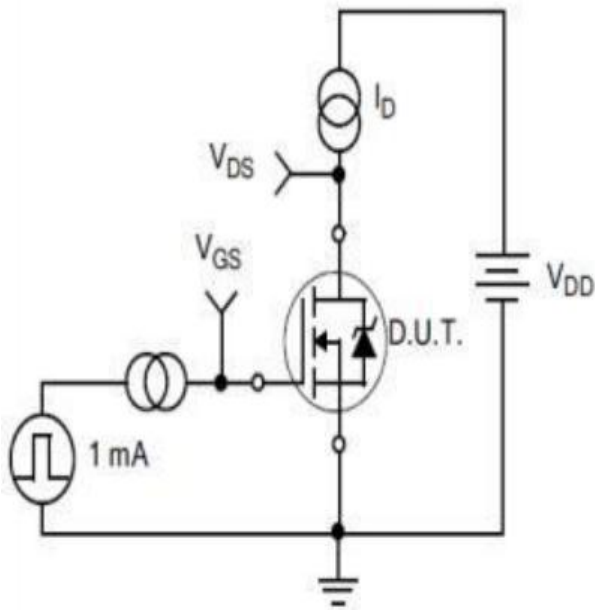


Figure A.
Gate Charge Test Circuit

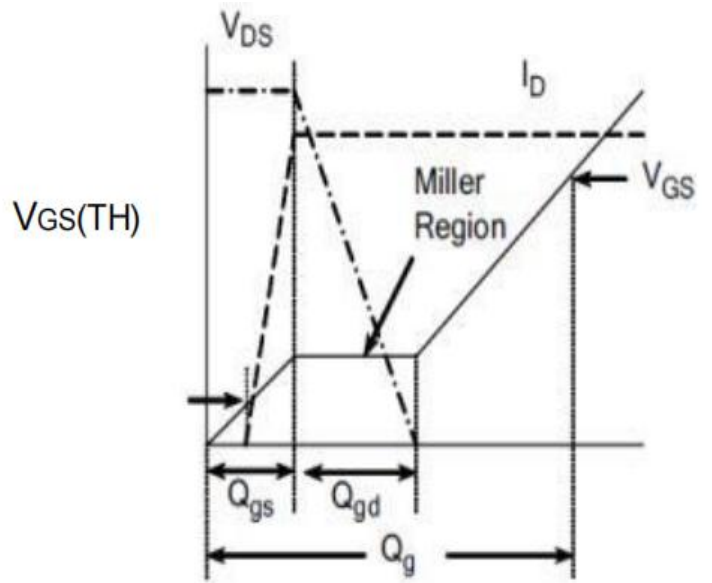


Figure B.
Gate Charge Waveform

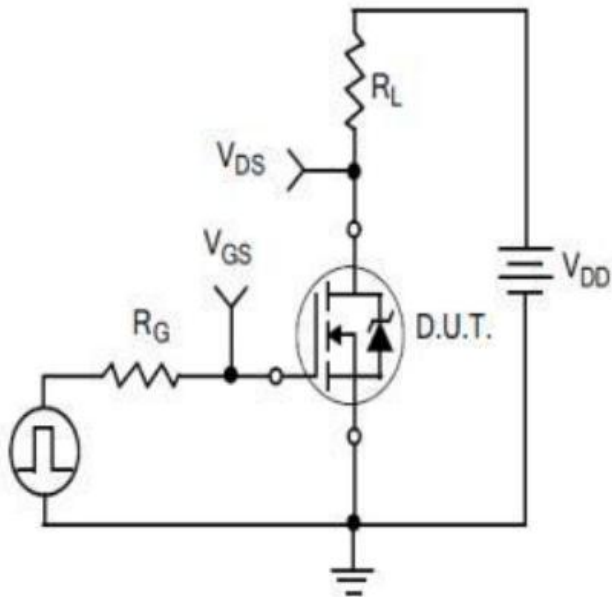


Figure C.
Resistive Switching Test Circuit

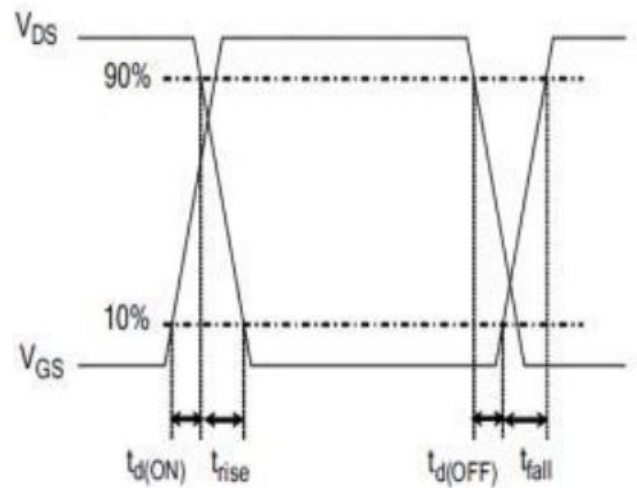


Figure D.
Resistive Switching Waveforms

Test circuits and Waveforms

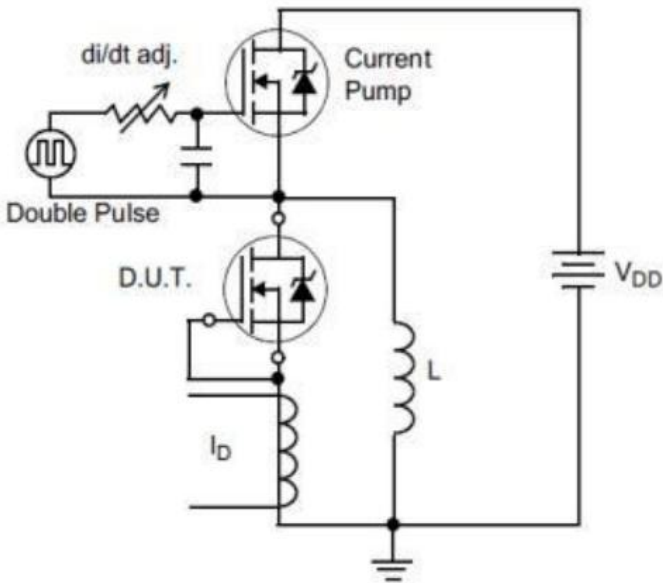


Figure E. Diode Reverse Recovery Test Circuit

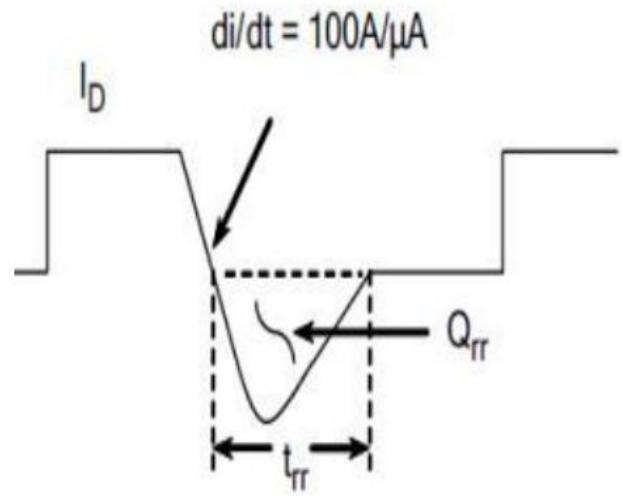


Figure F. Diode Reverse Recovery Waveform

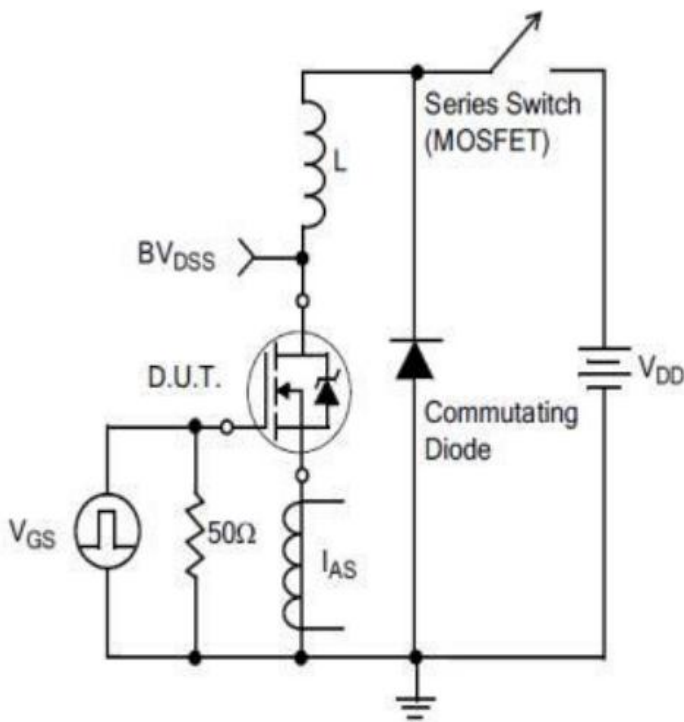
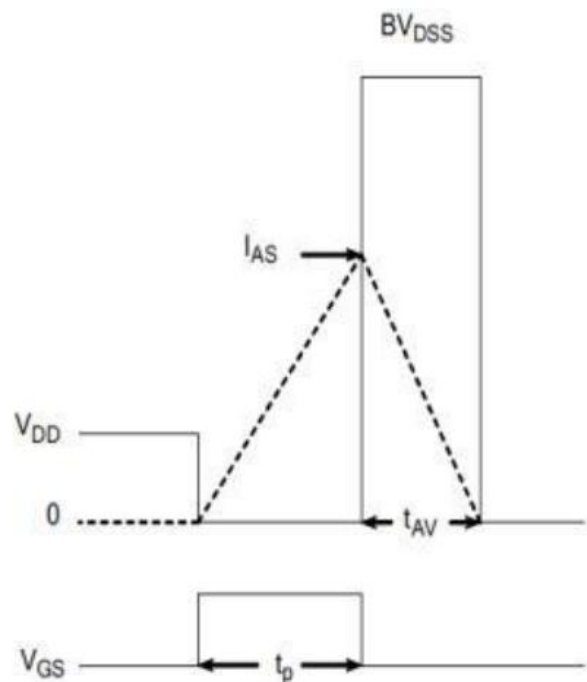
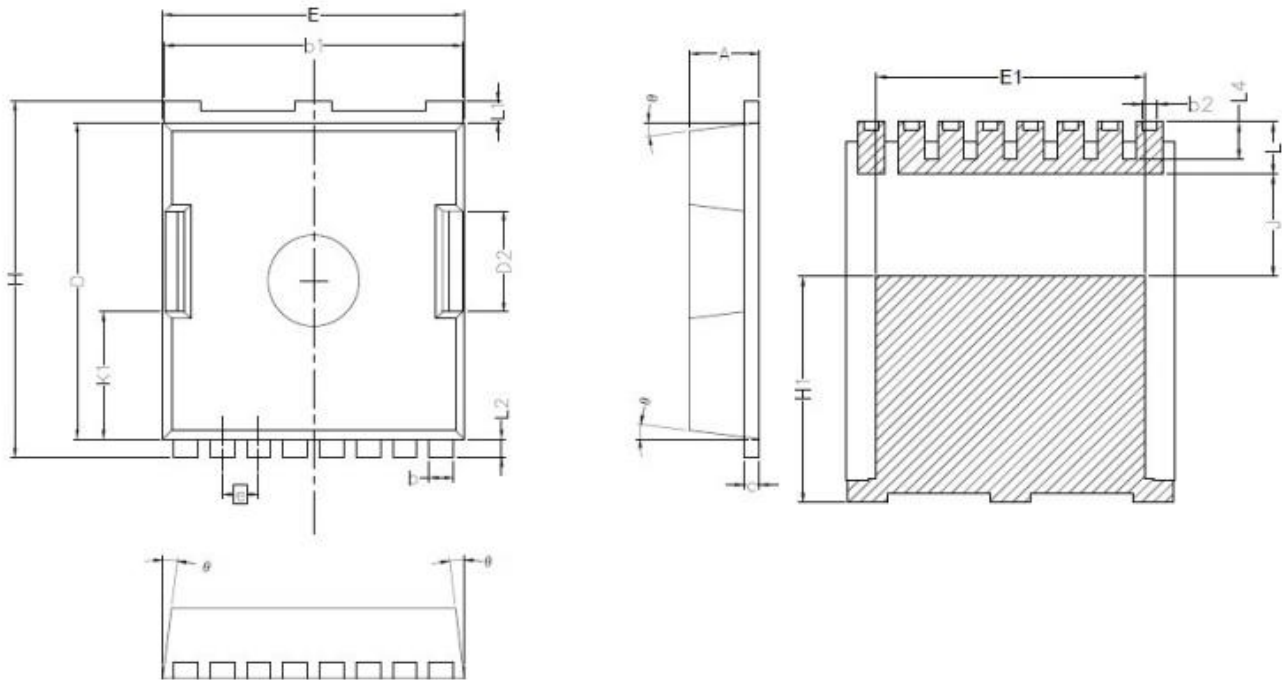


Figure G. Unclamped Inductive Switching Test Circuit



$$EAS = \frac{I_{AS}^2 L}{2}$$

Figure H. Unclamped Inductive Switching Waveforms

Package outline drawing(TOLL-8L Unit: mm)


Symbol	Dimensions In Millimeters	
	MIN.	MAX.
A	2.20	2.40
b	0.90	0.90
b1	9.70	9.90
b2	0.42	0.50
c	0.40	0.60
D	10.28	10.58
D2	3.10	3.50
E	9.70	10.10
E1	7.90	8.30
e	1.20BSC	
H	11.48	11.88
H1	6.75	7.15
N	8	
J	3.00	3.30
K1	3.98	4.38
L	1.40	1.80
L1	0.60	0.80
L2	0.50	0.70
L4	1.00	1.30
θ	4°	10°

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