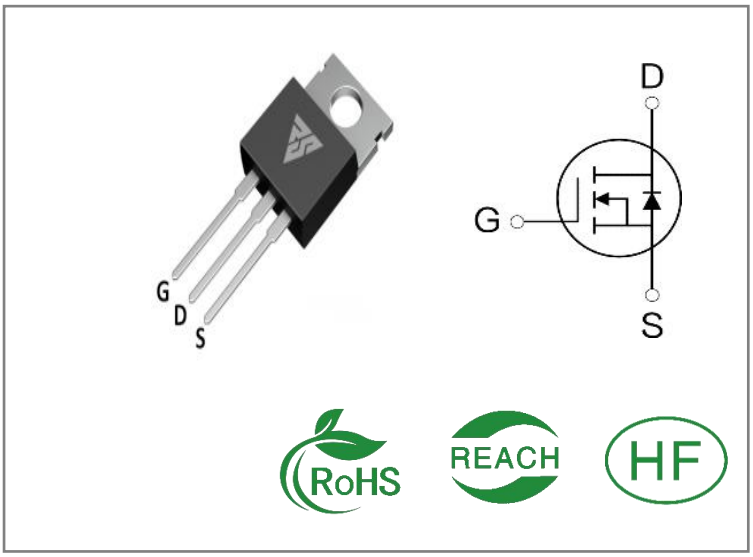
ID	R_{DS}(ON)(Typ)	VDSS
50A	14mΩ	60V



Applications:
- Load Switch
- PWM Applications
- Power Managment

Features:
- Fast switching speed
- 100% avalanche tested
- Improved dv/dt capability

Ordering Information

Part Number	Package	Marking	Packing	Qty.
RS60N50T	T0-220	RS60N50T	Tube	50 PCS

Absolute Maximun Ratings Tc= 2 5℃ unless otherwise specified

Symbol	Parameter	RS60N50T	Units
VDSS	Drain-to-Source Voltage	60	V
ID	Continuous Drain Current TC=25℃	50	A
IDM	Pulsed Drain Current	200	
PD	Power Dissipation	110	W
VGS	Gate- to- Source Voltage	±20	V
EAS	Single Pulse Avalanche Engergy L = 1mH,VDD = 50V, RG = 25Ω, Tj = 25℃	2500	mJ
TL TPKG	Maximum Temperature for Soldering	300 260	℃
	Leads at 0.063in(1.6mm)from Case for 10 seconds Package Body for 10 seconds		
TJ and TSTG	Operating Junction and Storage Temperature Range	-55 to 150	

* Drain Current Limited by Maximum Junction Temperature

Caution: Stresses greater than those listed in the“ Absolute Maximum Ratings” Table may cause permanent damage to the device.

Thermal Resistance

Symbol	Parameter	RS60N50T	Units	Test Conditions
RθJC	Junction-to-Case	1.14	℃/ W	Drain lead soldered to water cooled heatsink, PD adjusted for a peak junction temperature of + 1 5 0 ℃
RθJA	Junction-to-Ambient	60		1 cubic foot chamber,free air.

OFF Characteristics TJ= 25℃ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
BVDSS	Drain- to- source Breakdown Voltage	60	--	--	V	VGS=0V,ID=250μA
IDSS	Drain- to- Source Leakage Current	--	--	5.0	μA	VDS=60V,VGS=0V
IGSS	Gate- to- Source Forward Leakage	--	--	100	nA	VGS=20V ,VDS=0V
	Gate- to- Source Reverse Leakage	--	--	-100		VGS=-20V ,VDS=0V

ON Characteristics TJ=25℃ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
RDS(on)	Static Drain- to- Source On-Resistance	--	14	22	mΩ	VGS=10V,ID=25A
VGS(TH)	Gate Threshold Voltage	2.0	--	4.0	V	VGS=VDS,ID=250μA

Resistive Switching Characteristics Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
td(ON)	Turn- on Delay Time	--	22	--	nS	VDS=30V ID=50A RG=25Ω
trise	Rise Time	--	82	--		
td(OFF)	Turn- OFF Delay Time	--	52	--		
tfall	Fall Time	--	93	--		

Dynamic Characteristics Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
Ciss	Input Capacitance (10V)	--	1489	--	pF	VGS= 0V VDS=25V f=1.0MHz
Coss	Output Capacitance (4.5V)	--	608	--		
Crss	Reverse Transfer Capacitance	--	275	--		
Qg	Total Gate Charge	--	60	--	nC	VDS=48V ID=50A VGS=10V
Qgs	Gate- to- Source Charge	--	6	--		
Qgd	Gate-to-Drain(" Miller") Charge	--	31	--		

Source- Drain Diode Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
IS	Continuous Source Current	--	--	50	A	Integral pn- diode in MOSFET
ISM	Maximum Pulsed Current	--	--	200	A	
VSD	Diode Forward Voltage	--	--	2	V	IS=25A,VGS=0V
trr	Reverse Recovery Time	--	68	--	nS	VGS=0V IS=50A di/dt=100A/μs
Qrr	Reverse Recovery Charge	--	4.2	--	uC	

Notes:

* 1. Repetitive rating,pulse width limited by maximum junction temperature.
* 2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 1%

Typical Feature Curve

Figure 1. Output Characteristics (T_J= 25ºC)

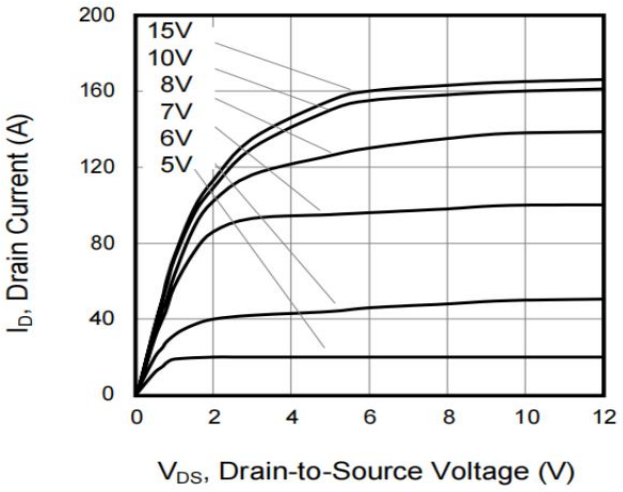


Figure 2. Body Diode Forward Voltage

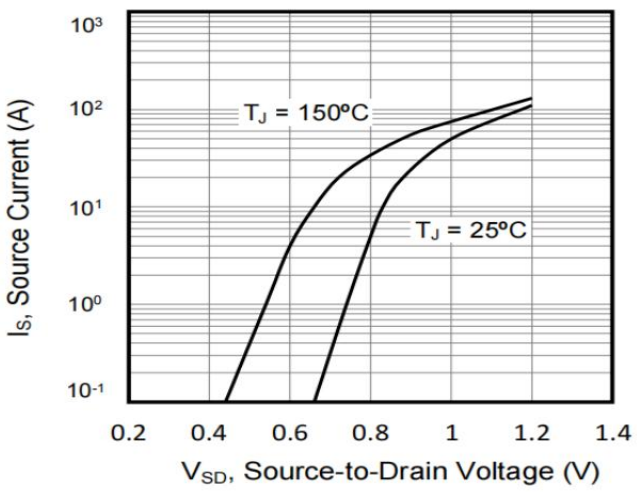


Figure 3. Drain Current vs. Temperature

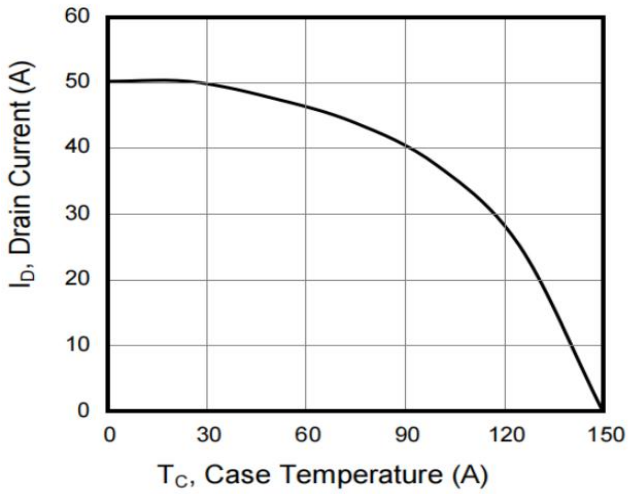


Figure 4. BV_{DSS} Variation vs. Temperature

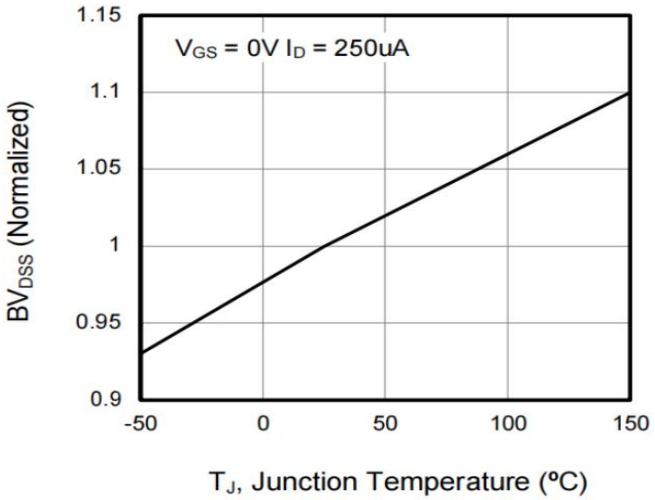


Figure 5. Transfer Characteristics

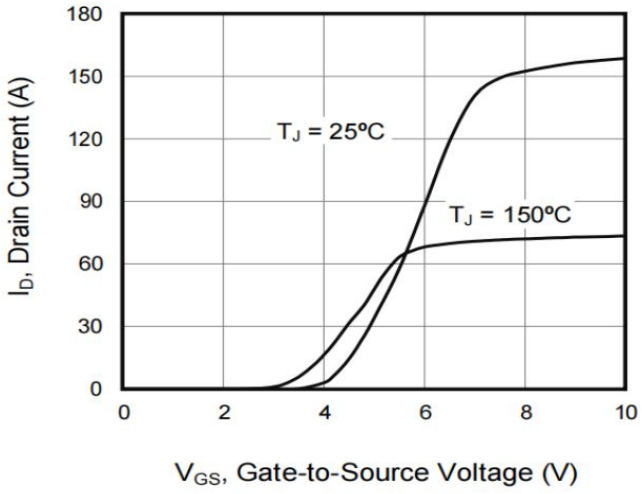


Figure 6. On-Resistance vs. Temperature

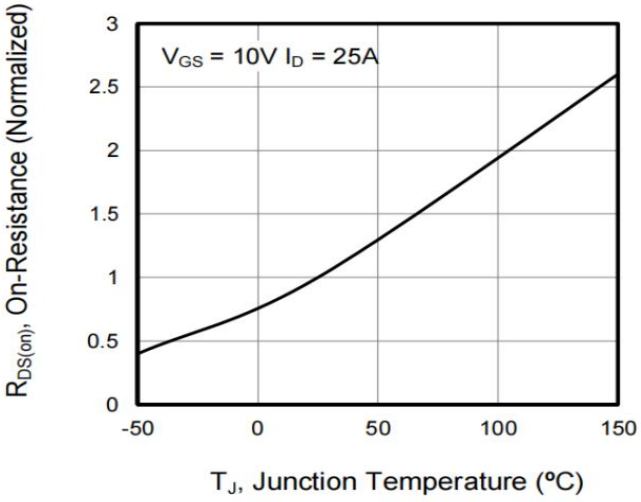


Figure 7. Capacitance

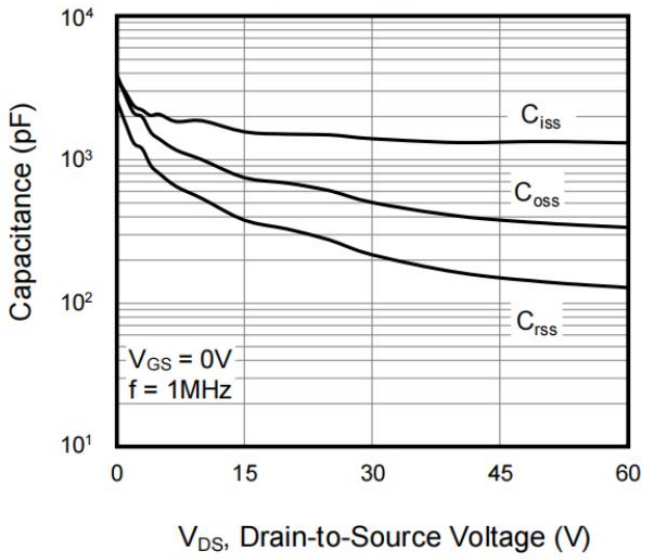


Figure 8. Gate Charge

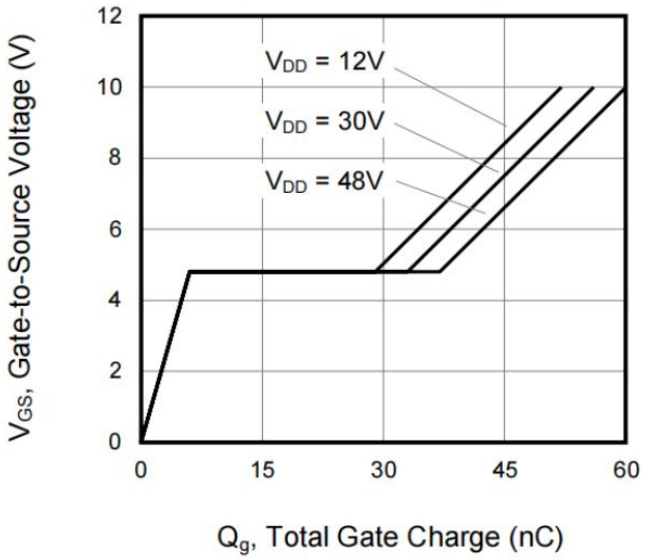
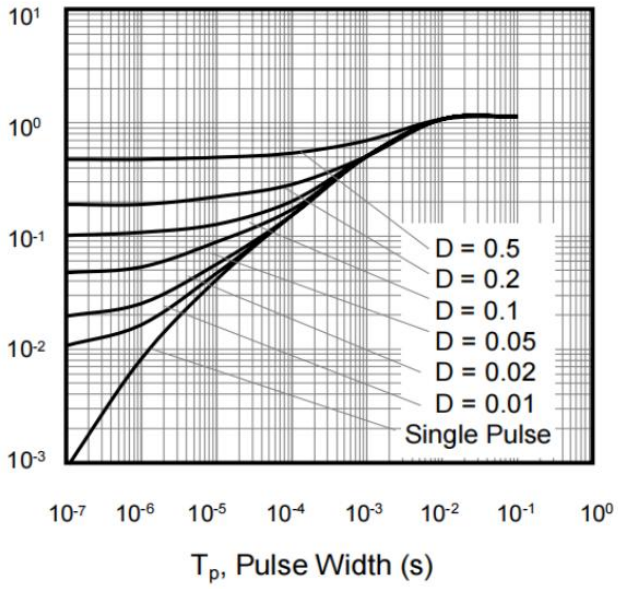


Figure 9. Transient Thermal Impedance



Test ircuits and Waveforms

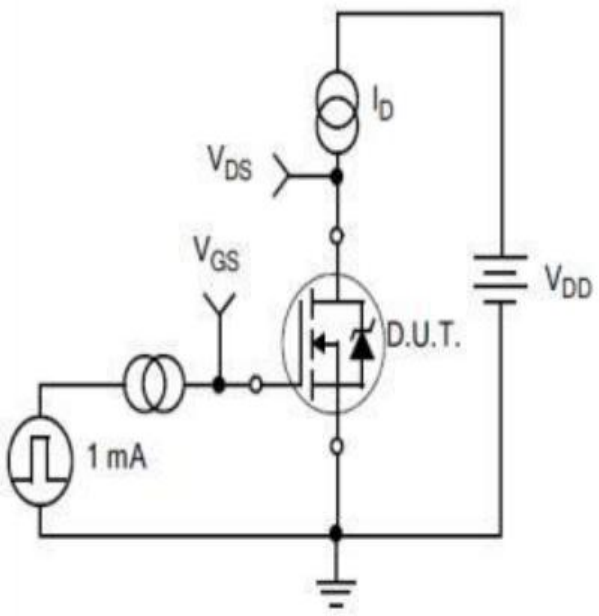


Figure A.
Gate Charge Test Circuit

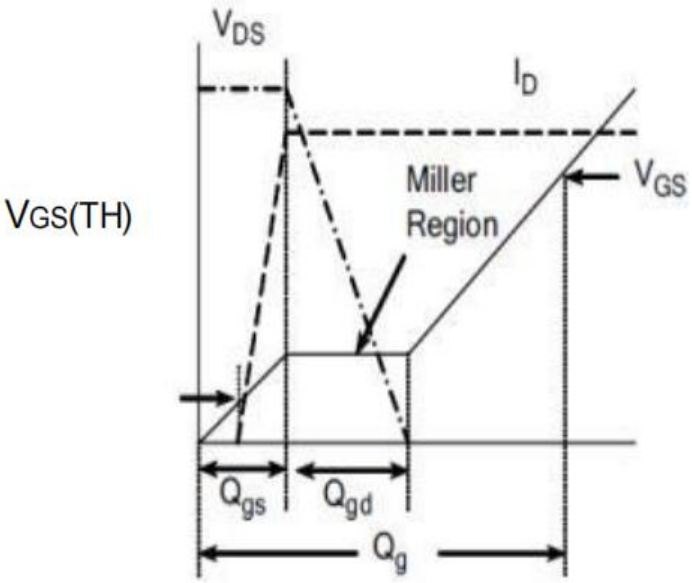


Figure B.
Gate Charge Waveform

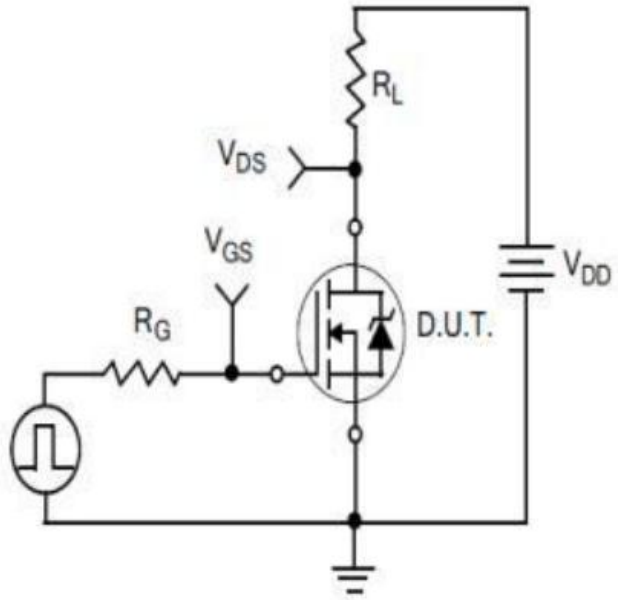


Figure C.
Resistive Switching Test Circuit

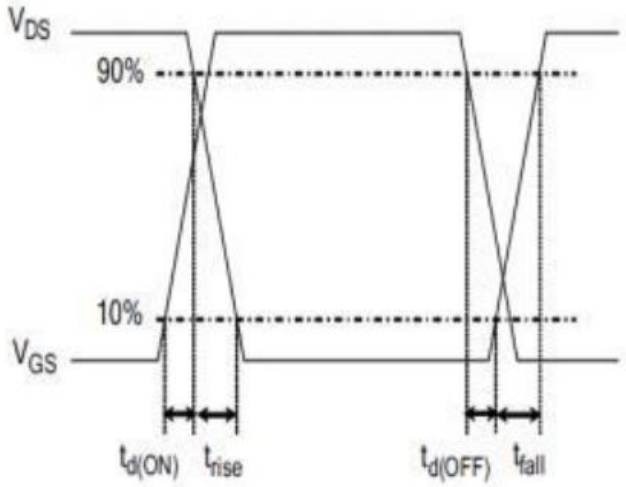


Figure D.
Resistive Switching Waveforms

Test ircuits and Waveforms

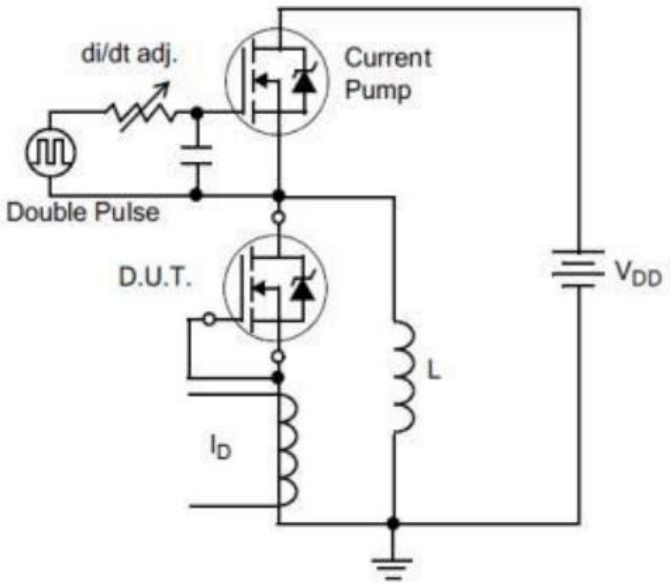


Figure E.Diode Reverse Recovery Test Circuit

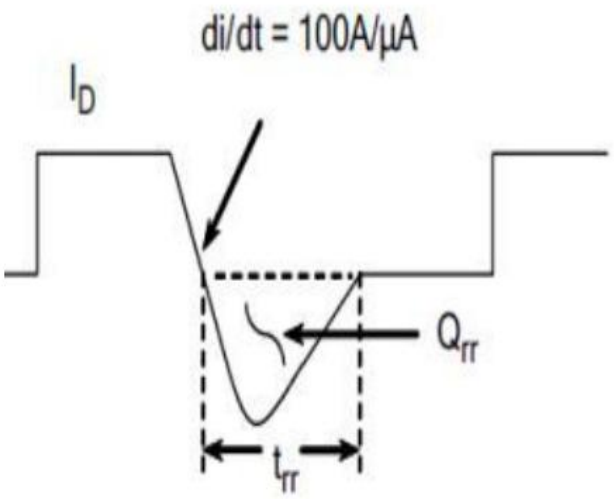


Figure F.Diode Reverse Recovery Waveform

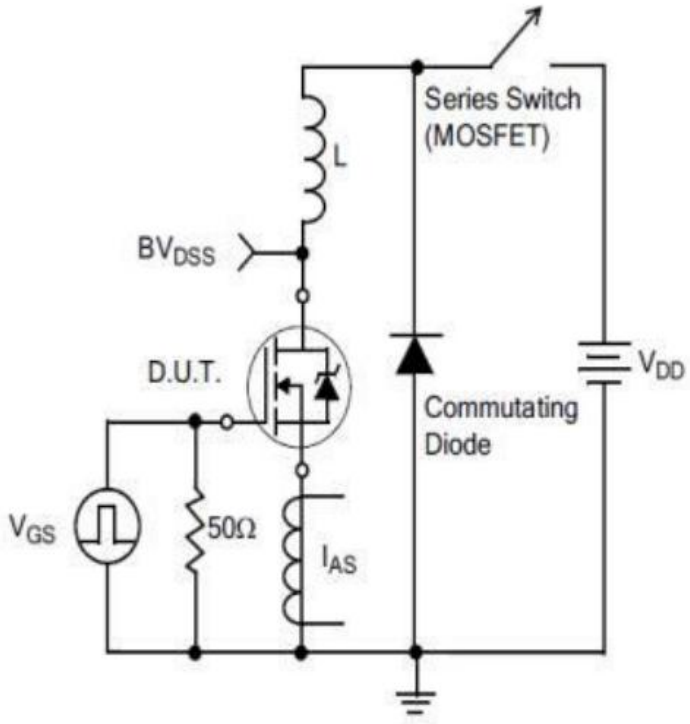
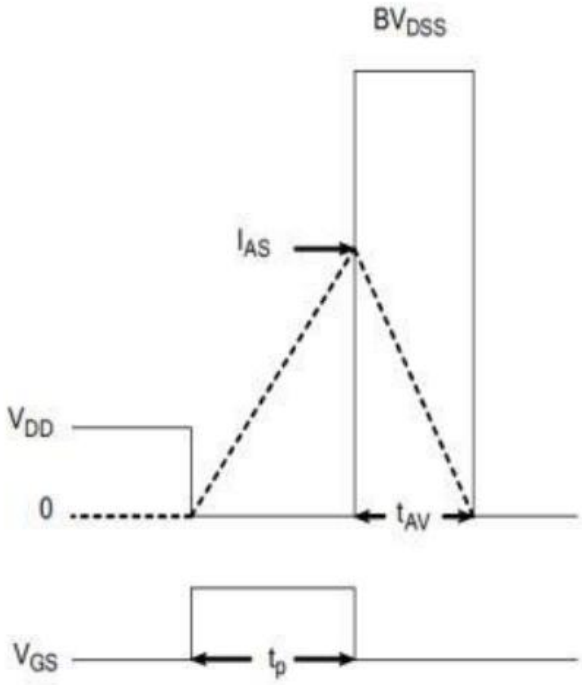


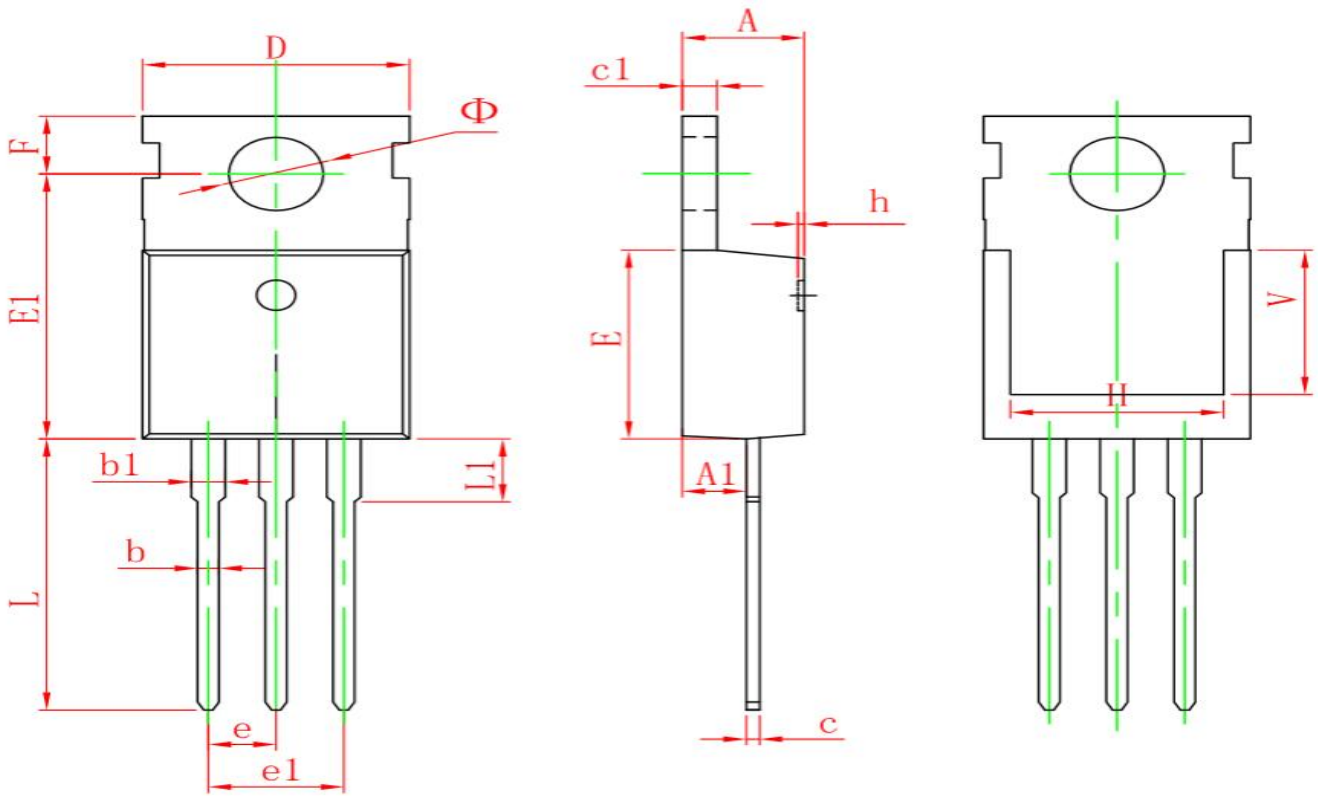
Figure G.Unclamped Inductive Switching Test Circuit



$$E_{AS}=\frac{I_{AS}^2 L}{2}$$

Figure H.Unclamped Inductive Switching Waveforms

Package outline drawing(TO-220 Unit: mm)



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	4.400	4.600	0.173	0.181
A1	2.250	2.550	0.089	0.100
b	0.710	0.910	0.028	0.036
b1	1.170	1.370	0.046	0.054
c	0.330	0.650	0.013	0.026
c1	1.200	1.400	0.047	0.055
D	9.910	10.250	0.390	0.404
E	8.950	9.750	0.352	0.384
E1	12.650	13.050	0.498	0.514
e	2.540 TYP.		0.100 TYP.	
e1	4.980	5.180	0.196	0.204
F	2.650	2.950	0.104	0.116
H	7.900	8.100	0.311	0.319
h	0.000	0.300	0.000	0.012
L	12.900	13.400	0.508	0.528
L1	2.850	3.250	0.112	0.128
V	6.900 REF.		0.276 REF.	
Φ	3.400	3.800	0.134	0.150

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