

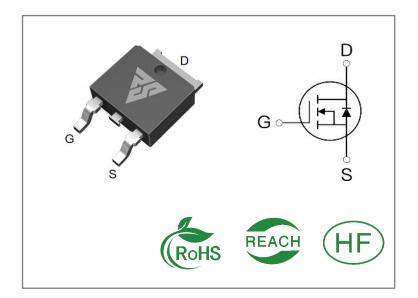
ID	R _{DS} (ON)(Typ)	VDSS
5A	1.25Ω	500V

Applications:

- Switch Mode Power Supply(SMPS)
- Adapter & Charger
- AC-DC Switching Power Supply

Features:

- Fast switching speed
- 100% avalanche tested
- Improved dv/dt capability



Ordering Information

Part Number	Package	Package Marking		Qty.	
RS5N50D	T0-252	RS5N50D	Tape&reel	2500 PCS	

Absolute Maximun Ratings Tc= 25°C unless otherwise specified

Symbol	Parameter	RS5N50D	Units
VDSS	Drain-to-Source Voltage	500	V
ID	Continuous Drain Current TC=25℃	5	
ID	Continuous Drain Current TC=100℃	3	А
IDM	Pulsed Drain Current	20	
PD	Power Dissipation	52	W
VGS	Gate- to- Source Voltage	±30	V
EAS	Single Pulse Avalanche Engergy L = 10mH, VDD = 50V, RG = 25Ω	200	mJ
	Maximum Temperature for Soldering		
TL TPKG	Leads at 0.063in(1.6mm)from Case for 10 seconds Package Body for 10 seconds	300 260	$^{\circ}$
TJ and TSTG	Operating Junction and Storage Temperature Range	-55 to 150	

^{*} Drain Current Limited by Maximum Junction Temperature Caution: Stresses greater than those listed in the "Absolute Maximum Ratings" Table may cause permanent damage to the device.





Thermal Resistance

Symbol	Parameter	RS5N50D	Units	Test Conditions
RθJC	Junction-to-Case	2.6	°C/W	Drain lead soldered to water cooled heatsink, PD adjusted for a peak junction temperature of + 1 5 0 $^{\circ}{\rm C}$
RθJA	Junction-to- Ambient	62		1 cubic foot chamber,free air.

OFF Characteristics TJ= 25 ^oC unless otherwise specified

Symbol	Parameter	Min.	Тур.	Max.	Units	Test Conditions
BVDSS	Drain- to- source Breakdown Voltage	500			٧	VGS=0V,ID=250μ A
IDSS	Drain- to- Source Leakage Current			1	μΑ	VDS=500V,VGS= 0V
ICCC	Gate- to- Source Forward Leakage			100	- A	VGS=30V ,VDS=0 V
IGSS	Gate- to- Source Reverse Leakage			-100	nA	VGS=-30V ,VDS= 0V

ON Characteristics TJ=25°C unless otherwise specified

Symbol	Parameter	Min.	Тур.	Max.	Units	Test Conditions
RDS(on)	Static Drain- to- Source On- Resistance(Note*2)		1.25	1.45	Ω	VGS=10V,ID=2.5 A
VGS(TH	Gate Threshold Voltage	2	3	4	V	VGS=VDS,ID=25 0μA

Resistive Switching Characteristics Essentially independent of operating temperature

Symbol	Parameter		Тур.	Max.	Units	Test Conditions
td(ON)	Turn- on Delay Time		24			
trise	Rise Time		18			VDS=250V
td(OFF)	Turn- OFF Delay Time		52		nS	ID=5A RG=10Ω
tfall	Fall Time		31			



Dynamic Characteristics Essentially independent of operating temperature

Symbol	Parameter	Min.	Тур.	Max.	Units	Test Conditions
Ciss	Input Capacitance		478			VGS=0V
Coss	Output Capacitance		55		рF	VDS=25V
Crss	Reverse Transfer Capacitance		6.7			f=1.0MHz
Qg	Total Gate Charge		16			VDS=400V
Qgs	Gate- to- Source Charge		3.5		nC	ID=5A
Qgd	Gate-to-Drain(" Miller") Charge		5.5			VGS=10V

Source-Drain Diode Characteristics

Symbol	Parameter	Min.	Тур.	Max.	Units	Test Conditions
IS	Continuous Source Current	Continuous Source Current		5	Α	Integral pn- diode
ISM	Maximum Pulsed Current			20	Α	in MOSFET
VSD	Diode Forward Voltage			1.4	V	IS=5A,VGS=0V
trr	Reverse Recovery Time		408		nS	VR=400V
Qrr	Reverse Recovery Charge		1.5		μС	IF=5A,di/dt=100 A/μs

Notes:

^{* 1.} Repetitive rating, pulse width limited by maximum junction temperature.

^{* 2.} Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 1%





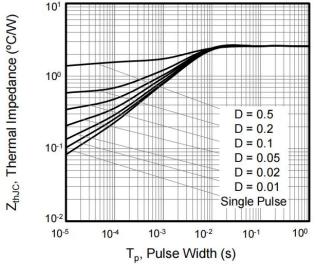


Figure 1. Transient Thermal Impedance

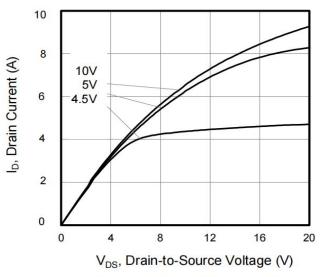


Figure 3. Output Characteristics

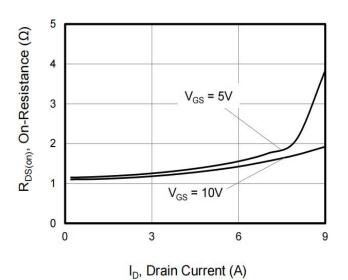


Figure 5. On-Resistance vs Drain Current

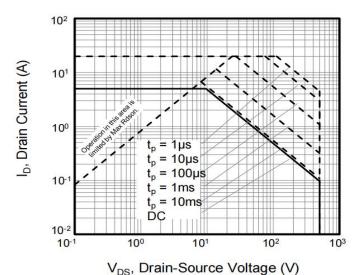


Figure 2. Safe Operation Area

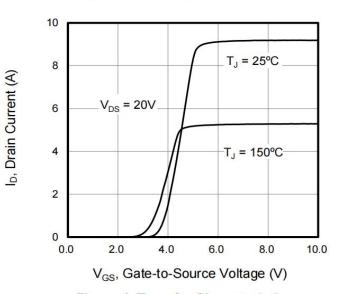
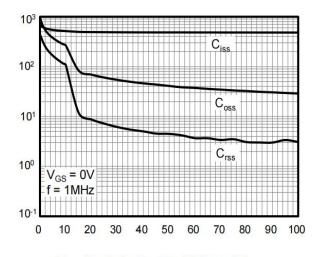


Figure 4. Transfer Characteristics



V_{DS}, Drain-to-Source Voltage (V)

Figure 6. Capacitance

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Capacitance (pF)



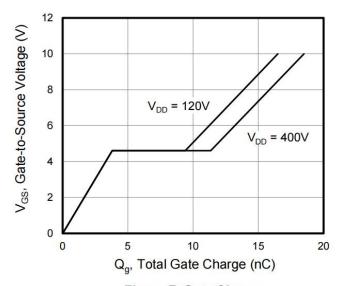


Figure 7. Gate Charge

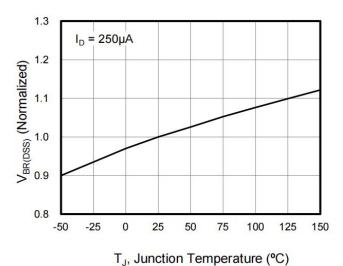
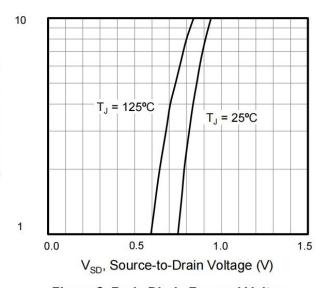


Figure 9. Breakdown Voltage vs Junction Temperature



Is, Source Current (A)

Figure 8. Body Diode Forward Voltage

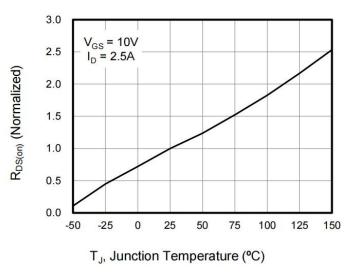


Figure 10. On-Resistance vs Temperature



Test Circuits and Waveforms

Figure A: Gate Charge Test Circuit and Waveform

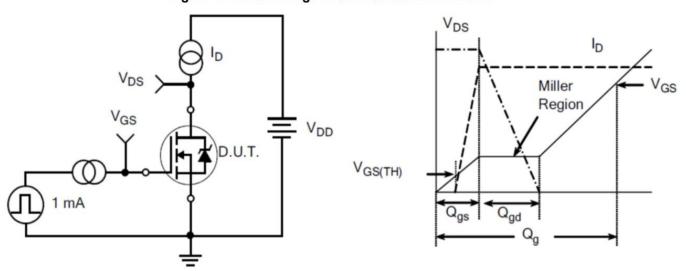


Figure B: Resistive Switching Test Circuit and Waveform

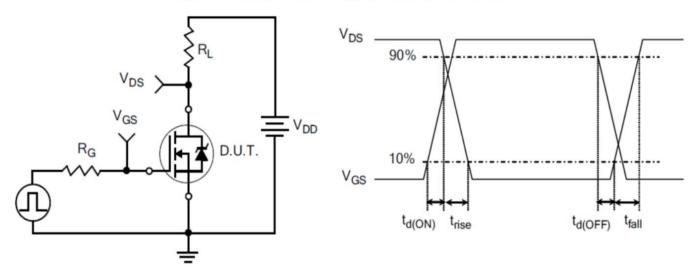
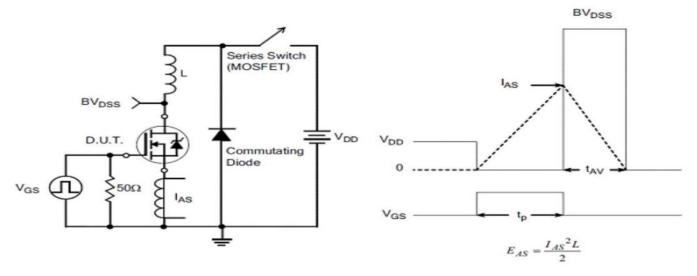


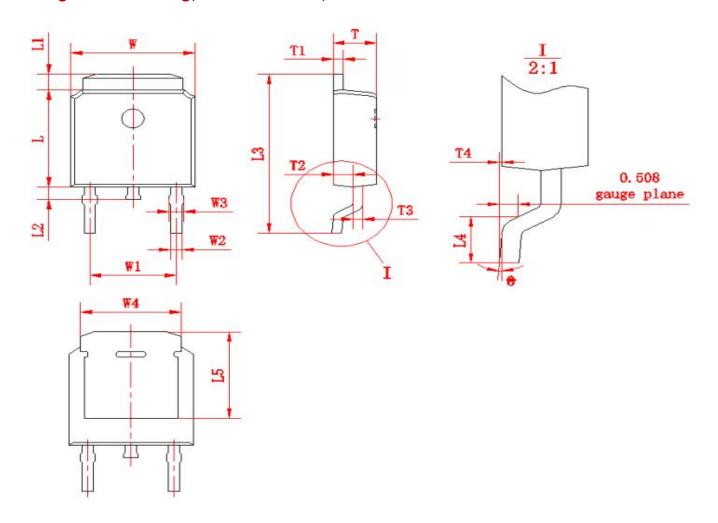
Figure C: Unclamped Inductive Switching Test Circuit and Waveform



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Package outline drawing(TO-252 Unit: mm)



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符号	Min	Max	符号	Min	Max	符号	Min	Max
W	6.50	6.70	L1	0.80	1.20	T1	0.48	0.58
W1	(4.5	572)	L2	0.60 1.00		T2	0.95	1.15
W2	0.6	0.8	L3	9.70	10.30	Т3	0.48	0.58
W3	0.68	0.88	L4	1.30	1.70	T4	0.00	0.12
W4	(5	.3)	L5	(5.20)		0	0	8
L	6.00	6.20	Т	2.20	2.40			



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